

High temperature low power quad voltage comparators

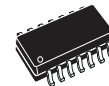
Features

- Wide single supply voltage range or dual supplies for all devices: +2 V to +36 V or ± 1 V to ± 18 V
- Very low supply current (1.1 mA) independent of supply voltage (1.4 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ± 5 nA typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 250 mV typ. ($I_O = 4$ mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

Description

This device consists of four independent precision voltage comparators. All these comparators are designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.

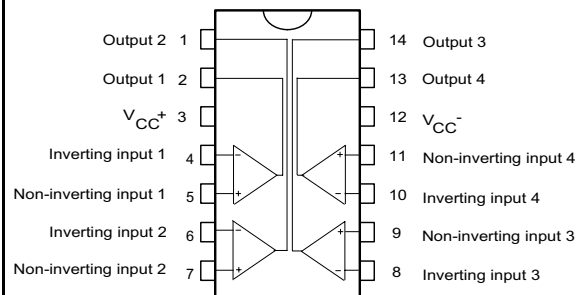


D
SO-14
(Plastic micropackage)



Wafer form

Pin connections (top view)



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	± 18 or 36	V
V_{ID}	Differential input voltage	± 36	V
V_{in}	Input voltage	-0.3 to +36	V
	Output short-circuit to ground ⁽¹⁾	20	mA
R_{thja}	Thermal resistance junction to ambient ⁽²⁾ (SO-14)	105	°C/W
R_{thjc}	Thermal resistance junction to case ⁽²⁾ (SO-14)	31	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽³⁾	500	V
	MM: machine model ⁽⁴⁾	100	
	CDM: charged device model ⁽⁵⁾	1500	
T_{stg}	Storage temperature range	-65 to +150	°C

1. Short-circuit from the output to V_{CC}^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of V_{CC}^+ .
2. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
3. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
4. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
5. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply voltage	2 to 36	V
T_{oper}	Operating free-air temperature range	-40 to +150	°C
V_{icm}	Input common mode voltage range($V_{CC}=30V$) ⁽¹⁾ $T_{amb} = +25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 to $V_{CC}^+ - 1.5$ 0 to $V_{CC}^+ - 2$	V

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5$ V, but either or both inputs can go to +30 V without damage.

2 Circuit schematics

Figure 1. Schematic diagram (1/4 LM2901)

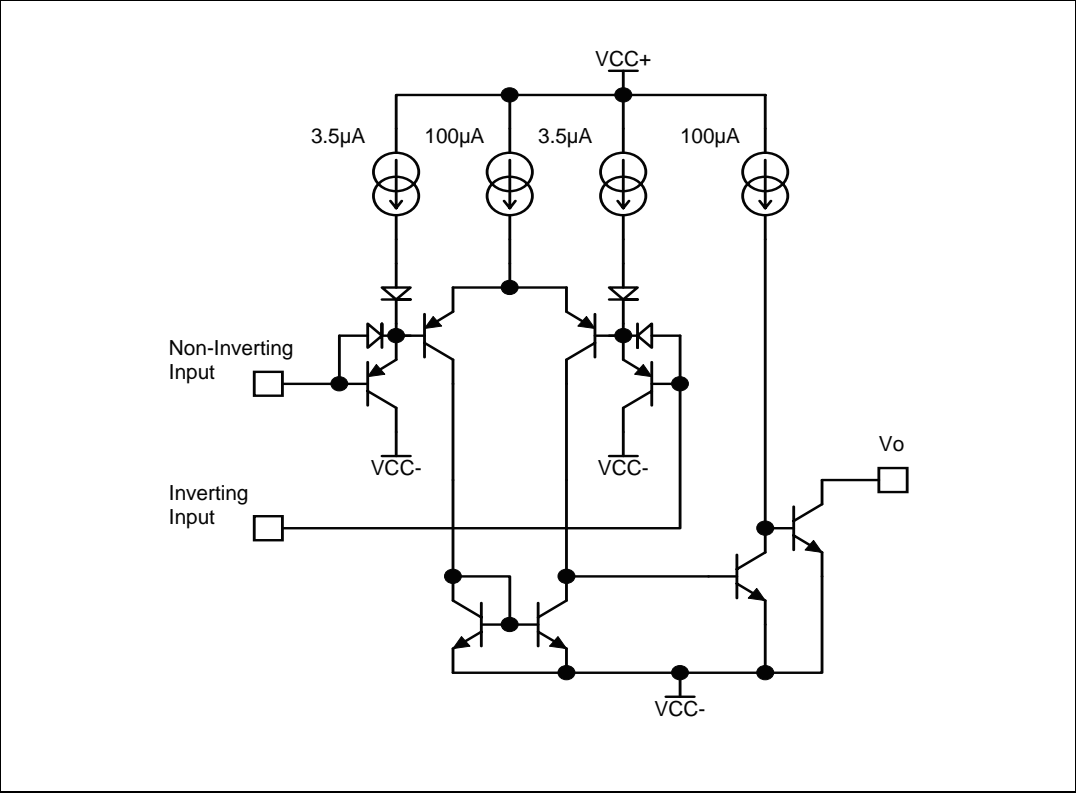
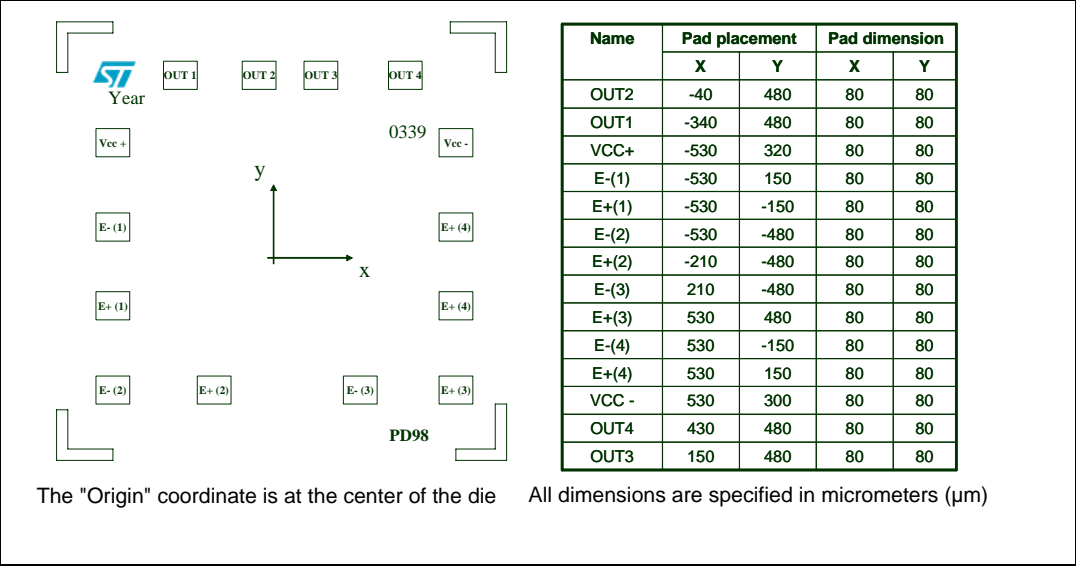


Figure 2. Pad locations



3 Electrical characteristics

Table 3. $V_{CC}^+ = 5V$, $V_{CC}^- = GND$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ⁽¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$		1	7 15	mV
I_{io}	Input offset current $T_{min} \leq T_{amb} \leq T_{max}$		5	50 150	nA
I_{ib}	Input bias current (I_{I^+} or I_{I^-}) ⁽²⁾ $T_{min} \leq T_{amb} \leq T_{max}$		25	250 400	nA
A_{VD}	Large signal voltage gain $V_{CC}=15V$, $R=15k\Omega$, $V_o=1$ to $11V$	25	200		V/mV
I_{CC}	Supply current (all comparators) $V_{CC} = +5V$, no load $V_{CC} = +30V$, no load		1.1 1.3	2 2.5	mA
V_{ID}	Differential input voltage ⁽³⁾			V_{CC}^+	V
V_{OL}	Low level output voltage $V_{id} = -1V$, $I_{sink} = 4mA$ $T_{min} \leq T_{amb} \leq T_{max}$		250	400 700	mV
I_{OH}	High level output current $V_{CC} = V_o = 30V$, $V_{id} = 1V$ $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1	nA μA
I_{sink}	Output sink current $V_{id} = -1V$, $V_o = 1.5V$ $T_{min} \leq T_{amb} \leq T_{max}$	6 2	16		mA
t_{re}	Small signal response time ⁽⁴⁾ $R_L = 5.1k\Omega$ connected to V_{CC}^+		1.3		μs
t_{rel}	Large signal response time ⁽⁵⁾ TTL input, $V_{ref} = +1.4V$, $R_L = 5.1k\Omega$ to V_{CC}^+ – Output signal at 50% of final value – Output signal at 95% of final value			500 1	ns μs

1. At output switch point, $V_o \approx 1.4V$, $R_S = 0$ with V_{CC}^+ from $5V$ to $30V$, and over the full input common-mode range ($0V$ to $V_{CC}^+ - 1.5V$).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so there is no load on the reference of input lines
3. The response time specified is for a $100mV$ input step with $5mV$ overdrive.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or $0.3V$ below the negative power supply, if used).
5. Maximum values are guaranteed by design.

Figure 3. Supply current vs. supply voltage

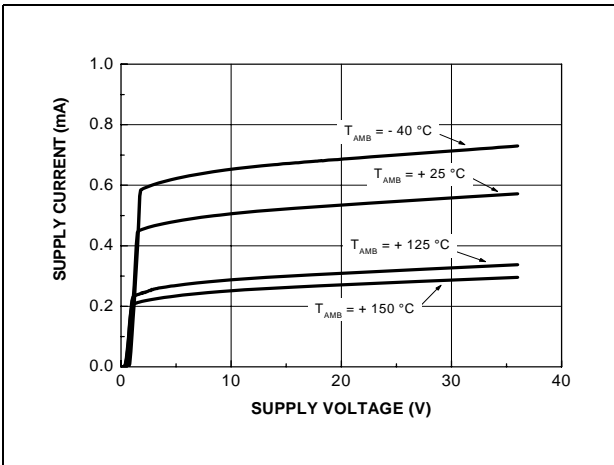


Figure 4. Input current vs. supply voltage

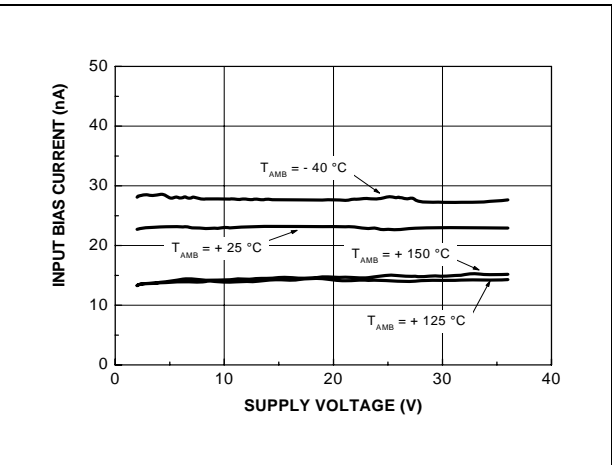


Figure 5. Output saturation voltage vs. output current ($V_{CC}=5V$)

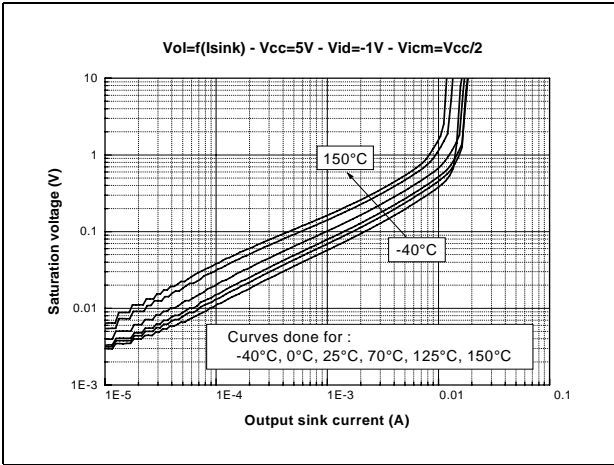


Figure 6. Output saturation voltage vs. output current ($V_{CC}=30V$)

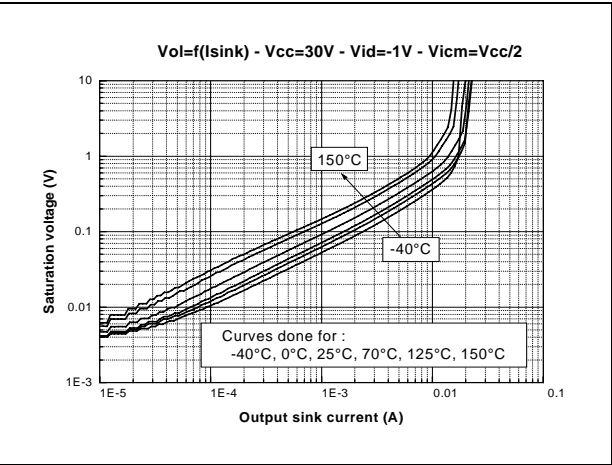


Figure 7. Response time for various input overdrives - positive transition

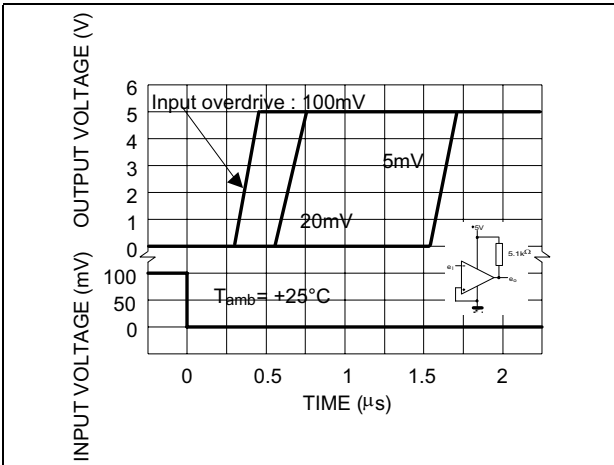
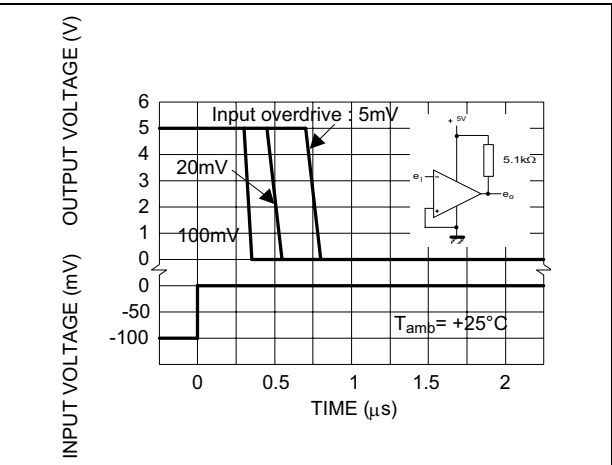


Figure 8. Response time for various input overdrives - negative transition



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 9. SO-14 package mechanical drawing

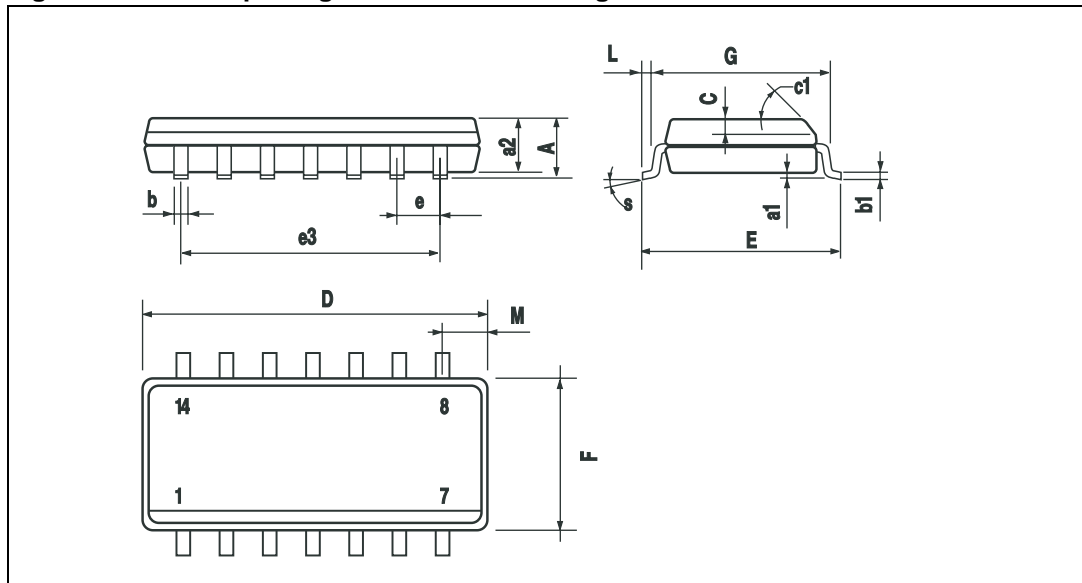


Table 4. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

5 Ordering information

Table 5. Order codes

Order code	Temperature range	Package	Packing	Marking
JLM2901H- I6D1	-40°C, +150°C	Wafer		
LM2901HD LM2901HDT		SO-14	Tube or Tape & reel	2901H
LM2901HYD ⁽¹⁾ LM2901HYDT ⁽¹⁾		SO-14 (Automotive grade)		2901HY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
25-Sep-2003	1	Initial release.
7-Jul-2005	2	PPAP references inserted in the datasheet, see Order codes table.
8-Nov-2005	3	Table data reformatted for easier use in Electrical characteristics . Curves added in Electrical characteristics section.
8-Apr-2008	4	Added ESD parameters in AMR table. Added operating conditions table. Added footnotes for automotive grade order codes in order codes table. Reformatted document.

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