



8K x 8 Registered PROM

Features

- CMOS for optimum speed/power
- High speed (commercial and military)
 - 15 ns address set-up
 - 12 ns clock to output
- Low power
 - 660 mW (commercial)
 - 770 mW (military)
- On-chip edge-triggered registers
 - Ideal for pipelined microprogrammed systems
- EPROM technology
 - 100% programmable
 - Reprogrammable (7C265W)
- 5V $\pm 10\%$ V_{CC} , commercial and military
- Capable of withstanding >2001V static discharge
- Slim 28-pin, 300-mil plastic or hermetic DIP

Functional Description

The CY7C265 is a 8192 x 8 registered PROM. It is organized as 8,192 words by 8 bits wide, and has a pipeline output register. In addition, the device features a programmable initialize byte that may be loaded into the pipeline register with the initialize signal. The programmable initialize byte is the 8,193rd byte in the PROM and its value is programmed at the time of use.

Packaged in 28 pins, the PROM has 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\bar{E}/I$ (enable or initialize), and CLOCK.

CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the pipeline register on each rising edge. The data will appear on the outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the enable or the initialize function.

If the asynchronous enable ($\bar{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

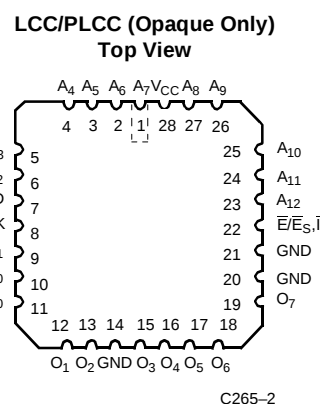
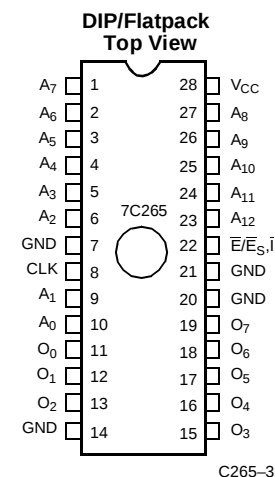
If the synchronous enable ($\bar{ES}$) is being used, the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

If the $\bar{E}/I$ pin is used for $\overline{INIT}$ (asynchronous), then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences, and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated, the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1's and 0's into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register clear (all outputs LOW). If all the bits of the initialize word are programmed to be a 1, activating $\overline{INIT}$ performs a register preset (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The $\overline{INIT}$ LOW disables clock and must return HIGH to enable clock independent of all other inputs, including the clock.



Pin Configurations



		7C265-15	7C265-25	7C265-40	7C265-50
Minimum Address Set-Up Time (ns)		15	25	40	50
Maximum Clock to Output (ns)		12	15	20	25
Maximum Operating Current (mA)	Com'l	120	120	100	80
	Mil	140	140		120

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial ^[1]	−40°C to +85°C	5V ±10%
Military ^[2]	−55°C to +125°C	5V ±10%

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C265-15, 25		7C265-40		7C265-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA	2.4						V
		V _{CC} = Min., I _{OH} = -4.0 mA			2.4		2.4		
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	Com'l	0.4					V
		V _{CC} = Min., I _{OL} = 12.0 mA				0.4		0.4	
		V _{CC} = Min., I _{OL} = 6.0 mA	Mil	0.4					
		V _{CC} = Min., I _{OL} = 8.0 mA						0.4	
V _{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V _{IL}	Input LOW Voltage			0.8		0.8		0.8	V
I _{IX}	Input Load Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-40	+40	-40	+40	-40	+40	μA
I _{OS} ^[4]	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = GND		90		90		90	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	120		100		80	mA
			Mil	140				120	
V _{PP}	Programming Supply Voltage		12	13	12	13	12	13	V
I _{PP}	Programming Supply Current			50		50		50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		3.0		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4		0.4		0.4	V

Capacitance^[5]

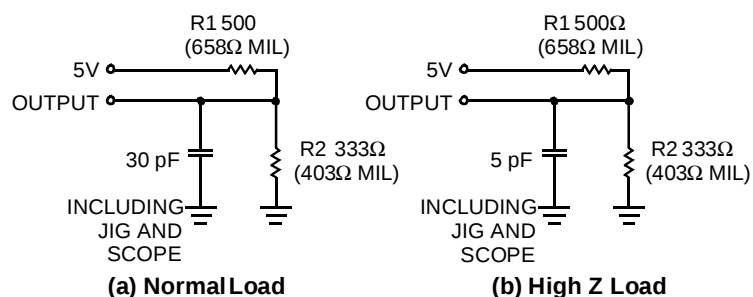
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

- See the last page of this specification for Group A subgroup testing information.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

Test Load for –15 through –25 speeds



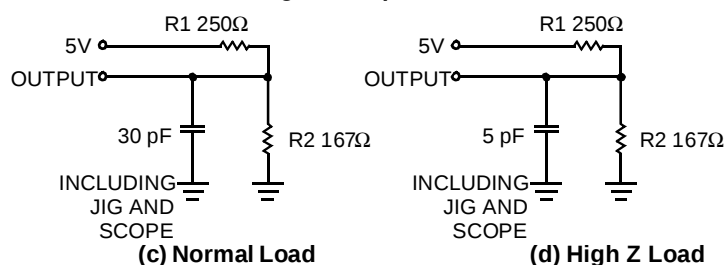
C269-4

C269-5

Equivalent to: THÉVENIN EQUIVALENT



Test Load for –40 through –50 speeds



C269-6

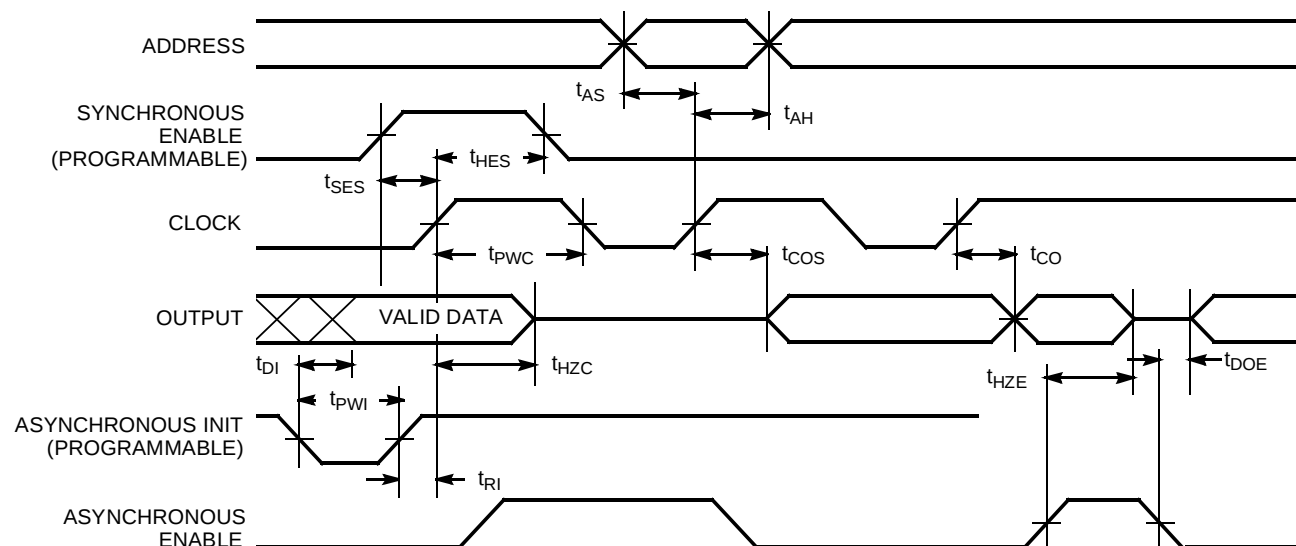
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range^[3, 5]

Parameter	Description	7C265-15		7C265-25		7C265-40		7C265-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	15		25		40		50		ns
t_{HA}	Address Hold from Clock	0		0		0		0		ns
t_{CO}	Clock to Output Valid		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	12		15		15		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync. Enable Only)	12		15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		5		ns
t_{DI}	$\overline{INIT}$ to Output Valid		15		18		25		35	ns
t_{RI}	$\overline{INIT}$ Recovery to Clock	12		15		20		25		ns
t_{PWI}	$\overline{INIT}$ Pulse Width	12		15		25		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		12		15		20		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		12		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$ LOW (Async. Mode)		12		15		20		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ HIGH (Async. Mode)		12		15		20		25	ns

Switching Waveform



C265-7

Erase Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the 7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity • exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 45 minutes. The 7C265 needs to be within one inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Programming Modes

The 7C265 offers a limited selection of programmed architectures. Programming these features should be done with a single 10-ms-wide pulse in place of the intelligent algorithm, mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture, VPP is applied to pins 3, 9, and 22. The choice of a particular mode depends on the states of the other pins during programming,

Bit Map Data

Programmer Address (Hex.)		RAM Data
Decimal	Hex	Contents
0	0	Data
.	.	.
8191	1FFF	Data
8192	2000	INIT Byte
8193	2001	Control Byte

Control Byte

- 00 Asynchronous output enable (default condition)
- 01 Synchronous output enable
- 02 Asynchronous initialize

so it is important that the condition of the other pins be met as set forth in the mode table. The considerations that apply with respect to power-up and power-down during intelligent programming also apply during architecture programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{PGM}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

Table 1. Mode Selection

Mode	Pin Function							
	Read or Output Disable	A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
	Other	A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Asynchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Synchronous Enable Read		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Asynchronous Initialization Read		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Program Memory		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Program Verify		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Program Inhibit		A ₁₂	A ₁₁	A ₁₀ – A ₇	A ₆	A ₅	A ₄ – A ₃	A ₂
Program Synchronous Enable		V _{IHP}	V _{IHP}	A ₁₀ – A ₇	V _{IHP}	V _{PP}	A ₄ – A ₃	V _{IHP}
Program Initialize		V _{ILP}	V _{IHP}	A ₁₀ – A ₇	V _{IHP}	V _{PP}	A ₄ – A ₃	V _{ILP}
Program Initial Byte		A ₁₂	V _{ILP}	A ₁₀ – A ₇	V _{IHP}	V _{PP}	A ₄ – A ₃	V _{ILP}

Mode	Pin Function							
	Read or Output Disable	A ₁	A ₀	GND	CLK	GND	$\bar{E}$, $\bar{I}$	O ₇ – O ₀
	Other	A ₁	A ₀	PGM	CLK	V _{FP}	V _{PP}	D ₇ – D ₀
Asynchronous Enable Read		A ₁	A ₀	GND	V _{IL}	GND	V _{IL}	O ₇ – O ₀
Synchronous Enable Read		A ₁	A ₀	GND	V _{IL} /V _{IH}	GND	V _{IL}	O ₇ – O ₀
Asynchronous Initialization Read		A ₁	A ₀	GND	V _{IL}	GND	V _{IL}	O ₇ – O ₀
Program Memory		A ₁	A ₀	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ – D ₀
Program Verify		A ₁	A ₀	V _{IHP}	V _{ILP}	V _{ILP}	V _{PP}	O ₇ – O ₀
Program Inhibit		A ₁	A ₀	V _{IHP}	V _{ILP}	V _{IHP}	V _{PP}	High Z
Program Synchronous Enable		V _{PP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ – D ₀
Program Initialize		V _{PP}	V _{ILP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ – D ₀
Program Initial Byte		V _{PP}	V _{IHP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{PP}	D ₇ – D ₀

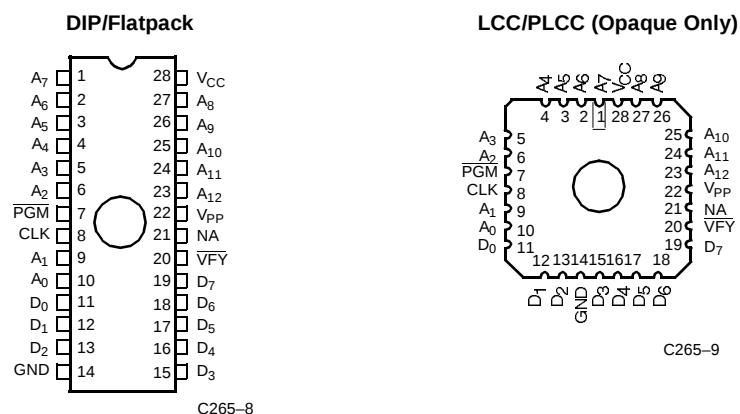
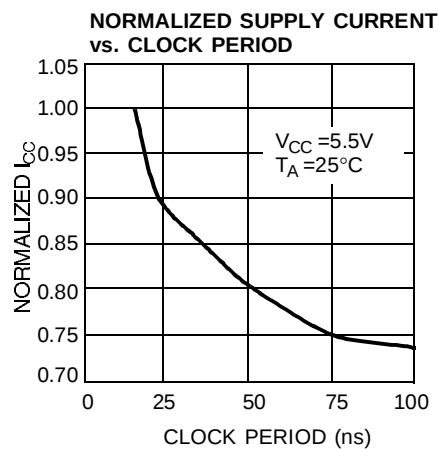
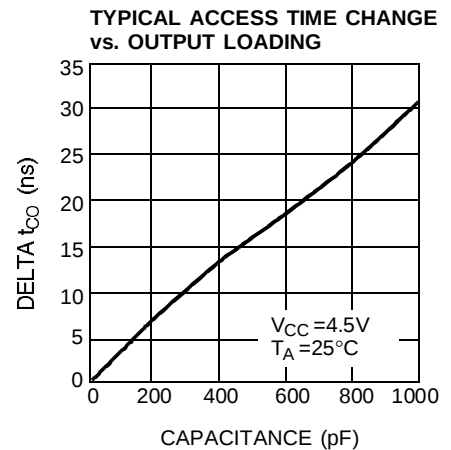
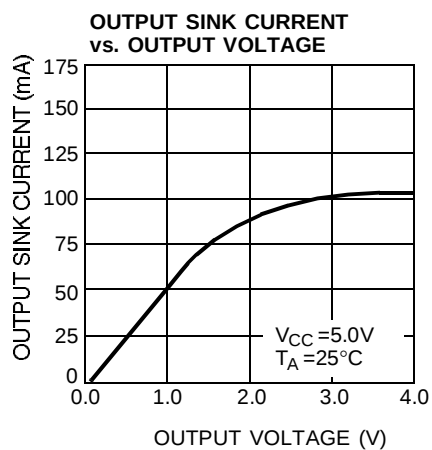
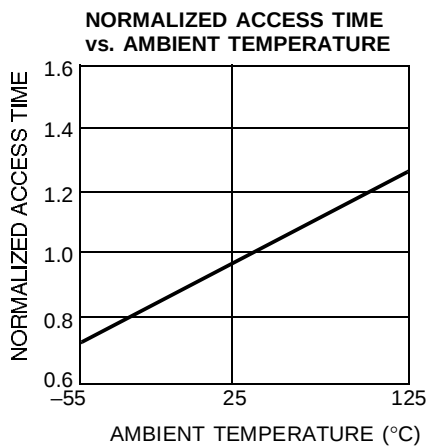
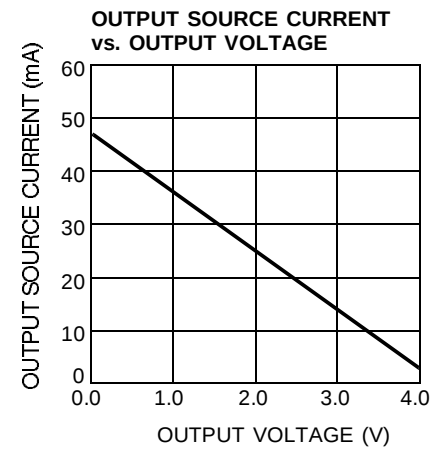
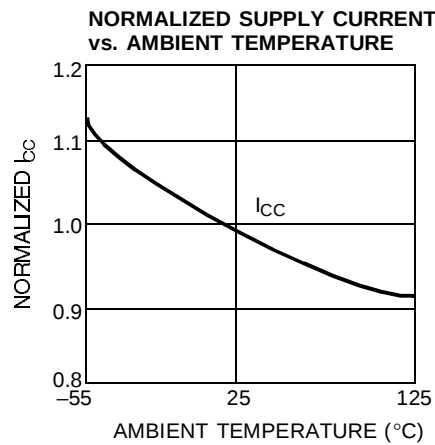
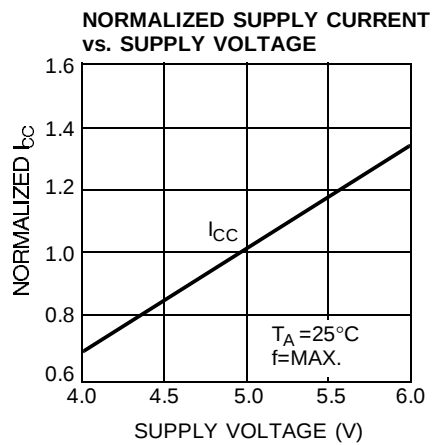


Figure 1. Programming Pinout

Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed

programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Typical DC and AC Characteristics


Ordering Information^[6]

Speed (ns)	I _{CC} (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	120	CY7C265-15JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-15PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-15WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265-15LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265-15QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265-15WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
25	120	CY7C265-25JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-25PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-25WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	140	CY7C265-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265-25LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265-25QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265-25WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	100	CY7C265-40JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-40PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-40WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	80	CY7C265-50JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
		CY7C265-50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C265-50WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	120	CY7C265-50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C265-50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C265-50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C265-50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:

6. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

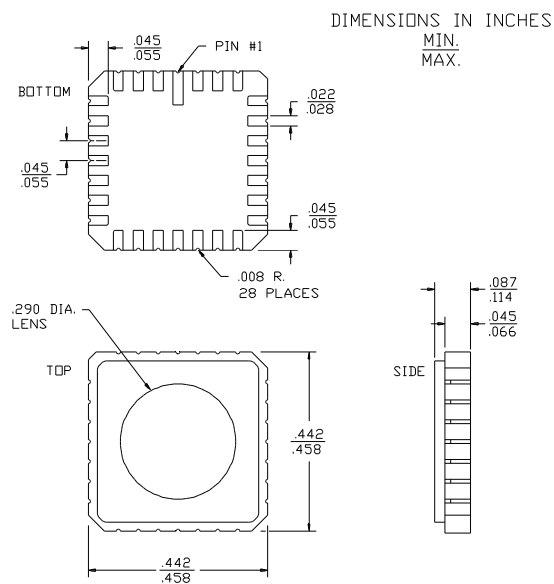
MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

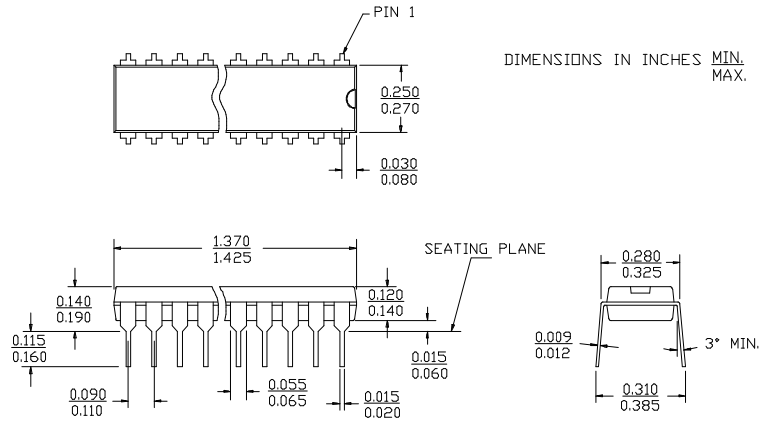
Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{AS}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{PW}	7, 8, 9, 10, 11
t _{SES}	7, 8, 9, 10, 11
t _{HES}	7, 8, 9, 10, 11
t _{COS}	7, 8, 9, 10, 11

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Package Diagrams (continued)
28-Lead (300-Mil) Molded DIP P21

28-Lead (300-Mil) Windowed CerDIP W22

MIL-STD-1835 D-15 Config. A

