



MOTOROLA

MC3440A MC3441A MC3443A

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVERS

The MC3440A, MC3441A, MC3443A are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the device.

The MC3441A differs in that all four drivers are controlled by the common Enable input. Again, the terminations are provided.

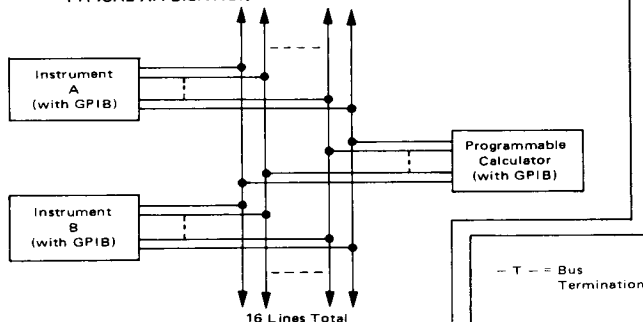
The MC3443A is identical to the MC3441A except that the terminations have been omitted. As such it is pin compatible, and functionally equivalent to the SN75138. It does offer the advantage of receiver input hysteresis.

- Receiver Input Hysteresis Provides Excellent Noise Rejection
- Open-Collector Driver Outputs Permit Wire-OR Connection
- Tailored to Meet the Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations provided (except MC3443A version)
- Provides Electrical Compatibility with General-Purpose Interface Bus

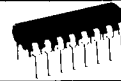
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830	mW
Operating Ambient Temperature Range	T_A	0 to $+70$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to $+150$	$^\circ\text{C}$

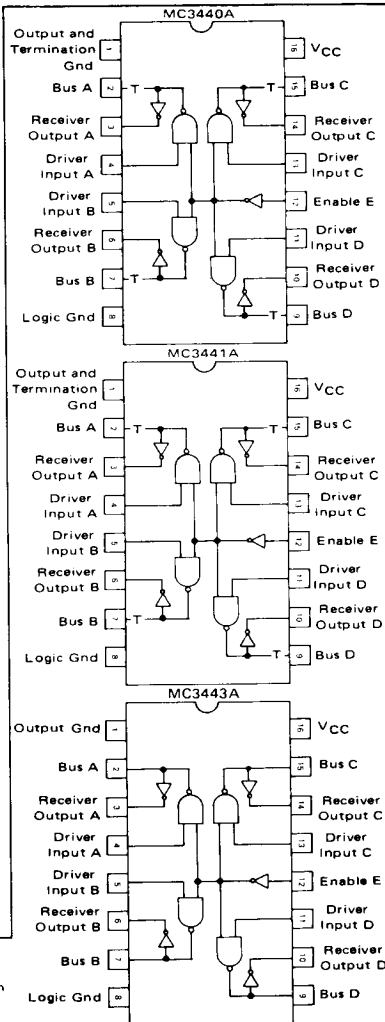
TYPICAL APPLICATION — GPIB MEASUREMENT SYSTEM



QUAD INTERFACE BUS TRANSCEIVERS SILICON MONOLITHIC INTEGRATED CIRCUITS



P SUFFIX
PLASTIC PACKAGE
CASE 648-05



MC3440A, MC3441A, MC3443A

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ and $0 \leq T_A \leq 70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State ($V_{IH} = 2.4\text{ V}$)	$I_{IH(D)}$	–	–	40	μA
Input Current – Low Logic State ($V_{IL} = 0.4\text{ V}$, $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$I_{IL(D)}$	–	–	–1.6 –0.25	mA
Input Clamp Voltage ($I_{IK} = -12\text{ mA}$)	$V_{IK(D)}$	–	–	–1.5	V
Output Voltage – High Logic State (1) ($V_{IH(E)} = 2.4\text{ V}$ or $V_{IL(D)} = 0.8\text{ V}$)	$V_{OH(D)}$	2.5	–	–	V
Output Voltage – Low Logic State ($V_{IH(D)} = 2.0\text{ V}$, $V_{IL(E)} = 0.8\text{ V}$, $I_{OL(D)} = 48\text{ mA}$) ($V_{IH(D)} = 2.0\text{ V}$, $V_{IL(E)} = 0.8\text{ V}$, $I_{OL(D)} = 100\text{ mA}$)	$V_{OL(D)}$	–	–	0.5 0.80	V
Output Leakage Current – MC3443A Only ($V_{IH(E)} = 2.0\text{ V}$ or $V_{IL(D)} = 0.8\text{ V}$)	$I_{OH(D)}$	–	–	250	μA

RECEIVER PORTION					
Input Hysteresis	–	400	580	–	mV
Input Threshold Voltage – Low to High Output Logic State ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$V_{ILH(R)}$	0.8	0.98	–	V
Input Threshold Voltage – High to Low Output Logic State ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)	$V_{IHL(R)}$	–	1.56	2.0	V
Output Voltage – High Logic State ($V_{IL(R)} = 0.8\text{ V}$, $I_{OH(R)} = -400\text{ }\mu\text{A}$)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IH(R)} = 2.0\text{ V}$, $I_{OL(R)} = 16\text{ mA}$)	$V_{OL(R)}$	–	–	0.5	V
Output Short Circuit Current ($V_{IL(R)} = 0.8\text{ V}$) (Only one output may be shorted at a time)	$I_{OS(R)}$	–20	–	–55	mA

BUS TERMINATION PORTION (Does not apply to MC3443A)

Bus Voltage ($V_{IL(D)} = 0.8\text{ V}$) ($I_{BUS} = -12\text{ mA}$) (No Load)	V_{BUS}	– 2.50	–	–1.5 3.70	V
Bus Current ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} \geq 5.0\text{ V}$) ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} \leq 5.5\text{ V}$) ($V_{IL(D)} = 0.8\text{ V}$, $V_{BUS} = 0.5\text{ V}$) ($V_{CC} = 0$, $0 \leq V_{BUS} \leq 2.75\text{ V}$)	I_{BUS}	0.7 – –1.3 –	– – – –	– 2.5 –3.2 +0.04	mA

TOTAL DEVICE POWER CONSUMPTION

Power Supply Current ($V_{IH(D)} = 2.4\text{ V}$, $V_{IL(E)} = 0\text{ V}$)	I_{CC}	30	56	75	mA
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SWITCHING CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	MC3440A, 3441A			MC3443A			Unit
		Min	Typ	Max	Min	Typ	Max	
DRIVER PORTION								
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	—	13	30	—	13	25	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	—	17	30	—	17	25	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	—	25	40	—	25	32	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	—	25	40	—	25	32	ns
RECEIVER PORTION								
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	—	15	30	—	15	22	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	—	15	30	—	15	22	ns

(1) 12 k resistor from the bus terminal to V_{CC} required on the MC3443A version.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

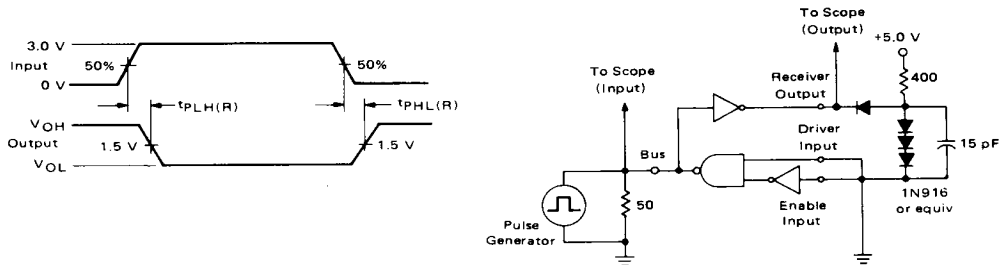


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

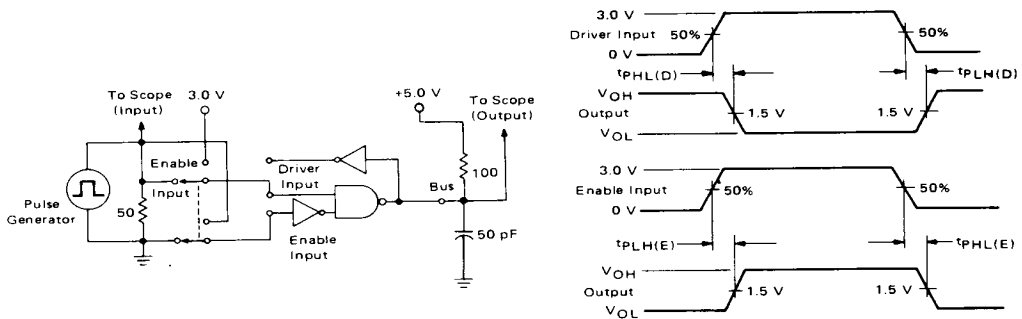
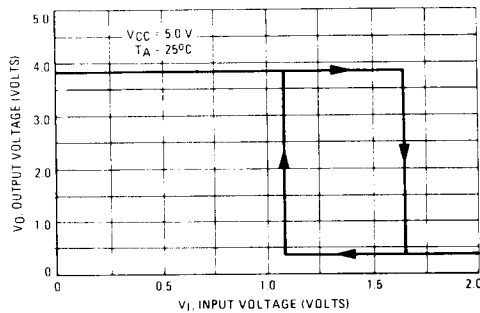
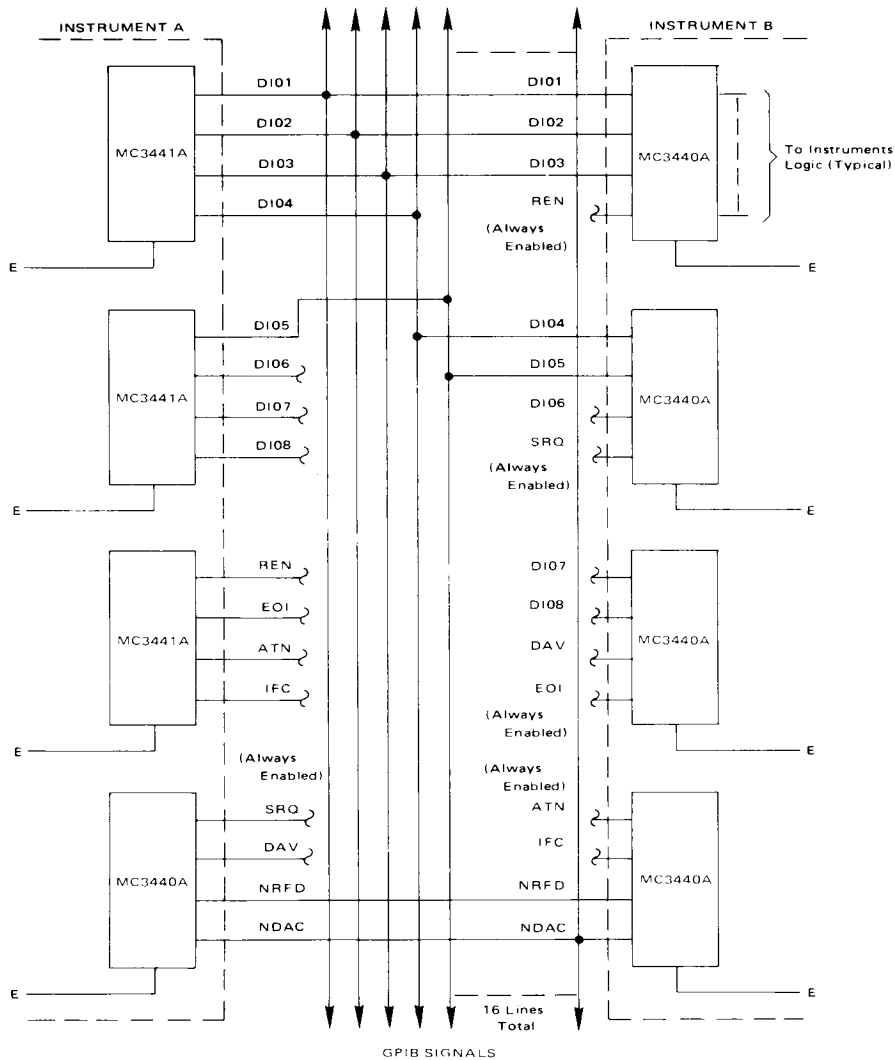


FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS



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GENERAL PURPOSE INTERFACE BUS APPLICATION



8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:

REN – Remote Enable

SRQ – Service Request

EOI – End or Identify

ATN – Attention

IFC – Interface Clear

3 Data Byte Transfer Control Bus

DAV – Data Valid

NRFD – Not Ready for Data

NDAC – Not Data Accepted

16 Total Signal Lines