Document Title

32K x 8 High Speed SRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	March 23,2001	
0B	Revise typo of t_{HA} on page 7	October 18,2001	
0C	Add SOP package type	February 18,2002	
0D	Revise typo of sop size at page 2,9	April 19,2002	

32K x 8 HIGH-SPEED CMOS STATIC RAM

FEATURES

- High-speed access times: 10, 12, 15, 20, 25 ns
- Low active power: 400 mW (typical)
- Low standby power
  -- 250 µW (typical) CMOS standby
  -- 55 mW (typical) TTL standby
- Fully static operation: no clock or refresh required
- TTL compatible interface and outputs
- Single 5V power supply

DESCRIPTION

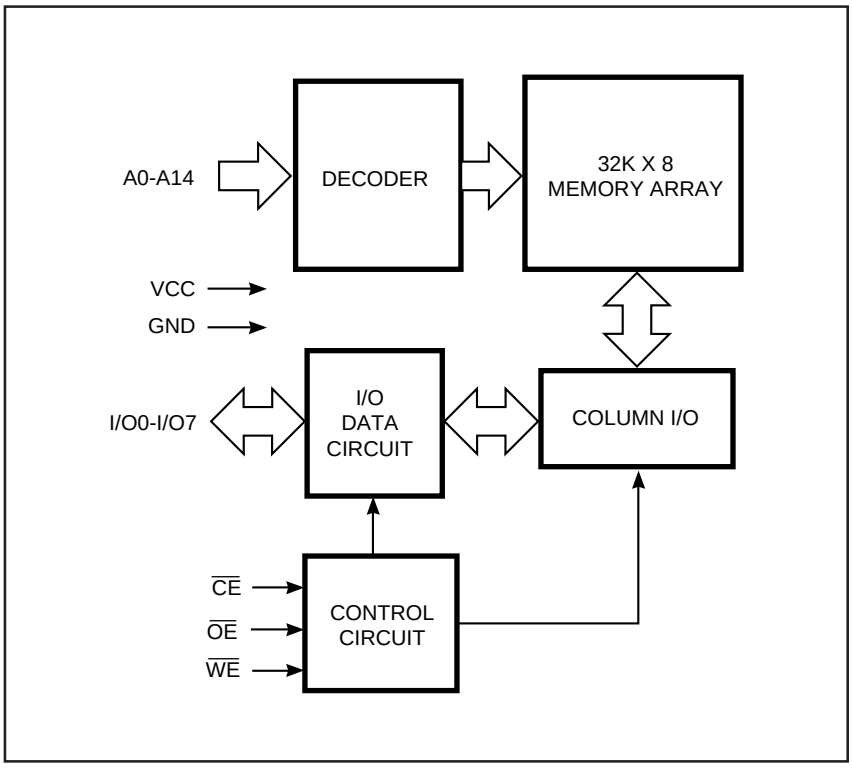
The *ICSI* IC61C256AH is very high-speed, low power, 32,768 word by 8-bit static RAMs. They are fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 50 µW (typical) with CMOS input levels.

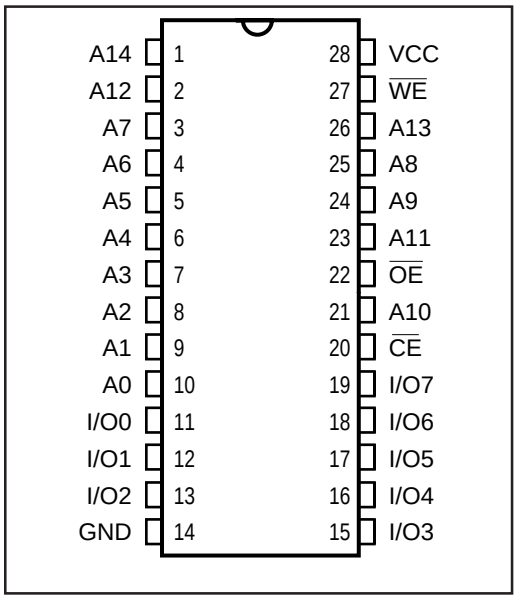
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$). The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IC61C256AH is pin compatible with other 32k x 8 SRAMs and are available in 28-pin 300mil PDIP, 300mil SOJ, and 8*13.4mm TSOP-1 package, 330 mil SOP.

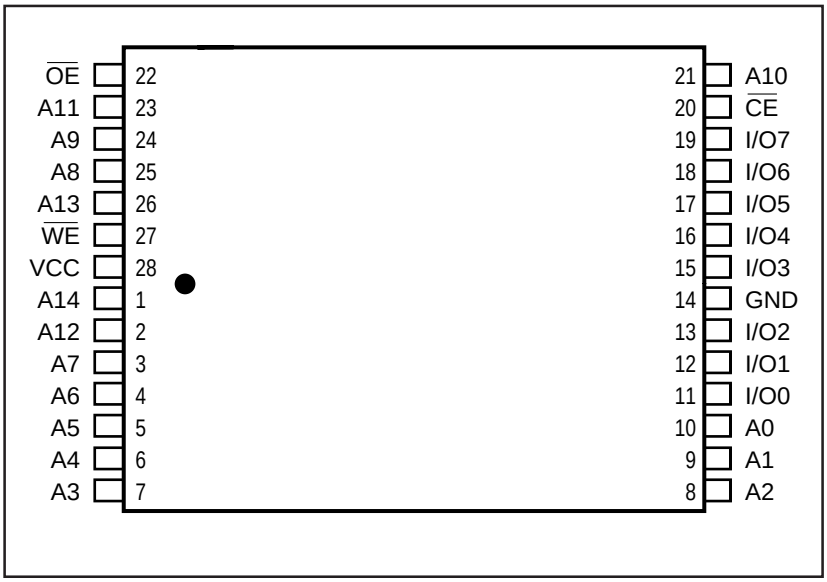
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin DIP and SOJ and SOP



PIN CONFIGURATION
8x13.4mm TSOP-1



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1},I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-10, -12	5V, ± 5%
		-15, -20	5V ± 10%
Industrial	–40°C to +85°C	-12	5V ± 5%
		-15, -20, -25	5V± 10%

Notes:
1. 8 ns is preliminary.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage[1]			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com. Ind.	–5 –10	5 10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com. Ind.	–5 –10	5 10	µA

Notes:
1. V_{IH}=V_{CC} +3.0V for pulse width less than 10ns.
2. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Sym.	Parameter	Test Conditions		-10 Min. Max.	-12 Min. Max.	-15 Min. Max.	-20 Min. Max.	-25 Min. Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind.	— 145 — 180	— 135 — 170	— 125 — 160	— 120 — 150	— 120 — 140	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥V_{IH}, f = 0	Com. Ind.	— 25 — 30	— 25 — 30	— 25 — 30	— 25 — 30	— 25 — 30	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind.	— 2 — 10	— 2 — 10	— 2 — 10	— 2 — 10	— 2 — 10	mA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	—	15	—	20	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	7	—	8	—	9	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	6	—	7	—	9	—	10	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	3	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	7	—	8	—	9	—	10	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	10	—	12	—	15	—	18	—	20	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

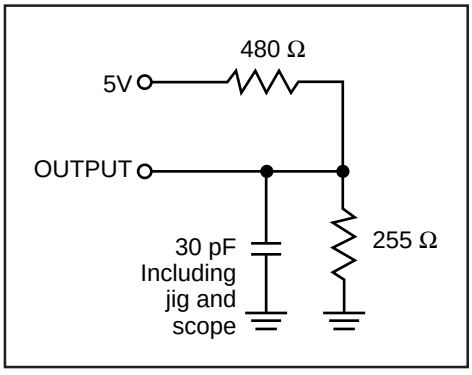


Figure 1.

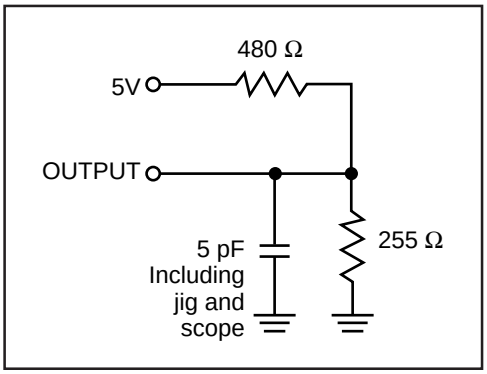
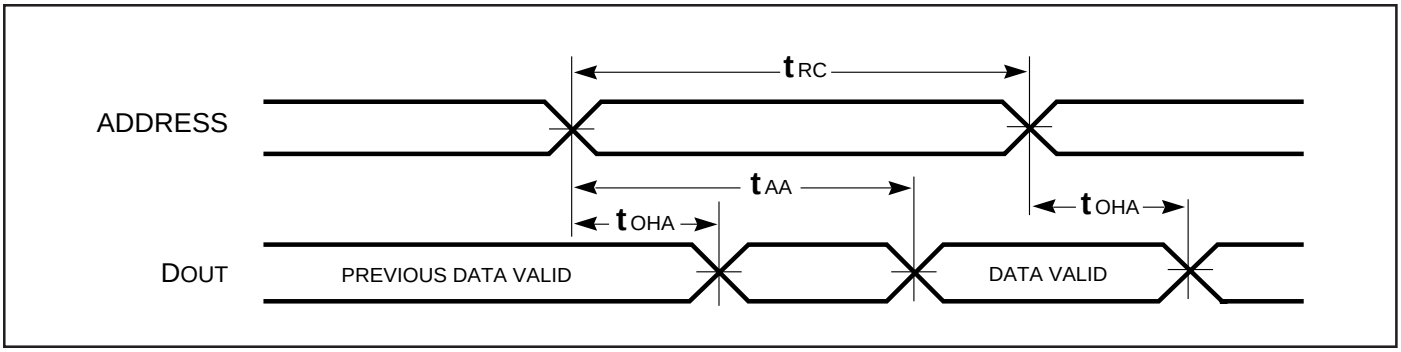


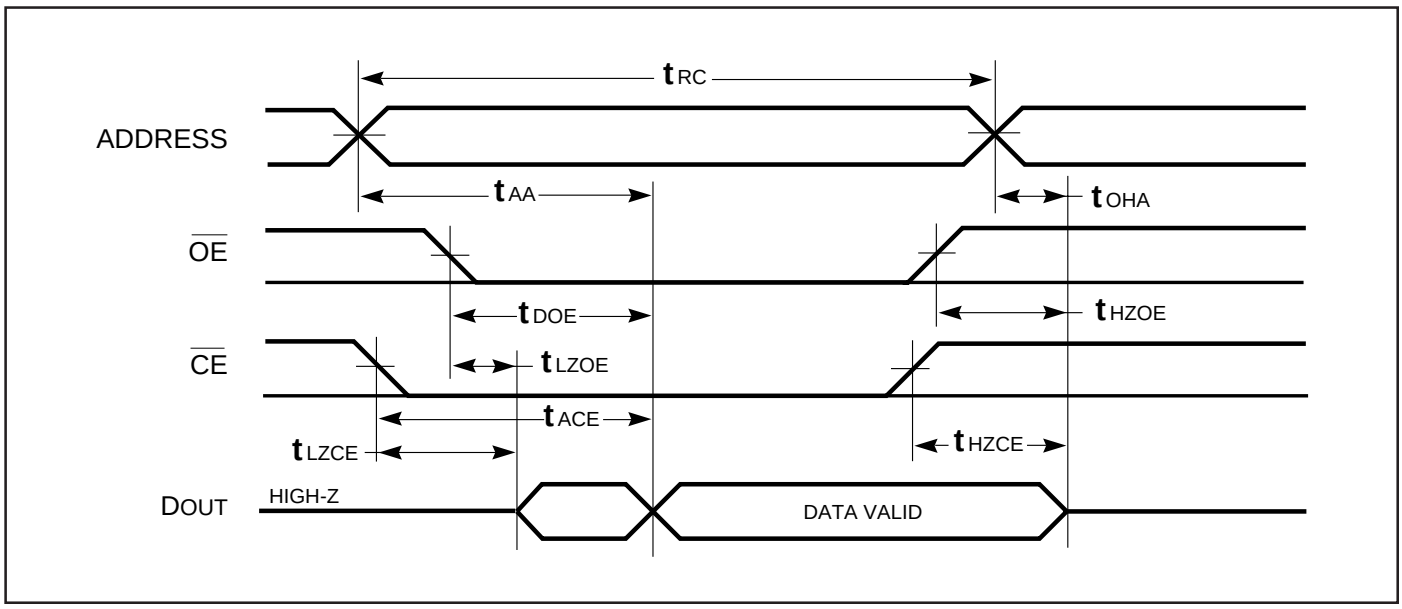
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

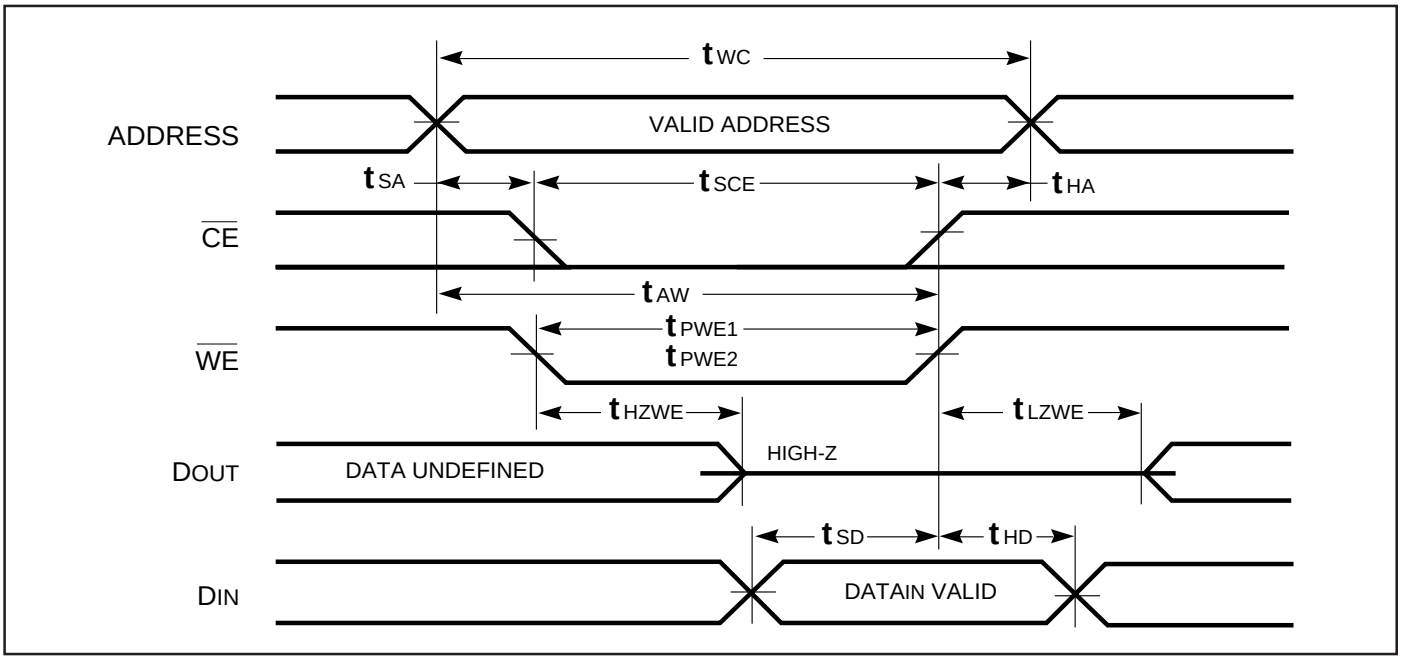
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	9	—	10	—	10	—	13	—	15	—	ns
t_{AW}	Address Setup Time to Write End	9	—	10	—	12	—	15	—	20	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	8	—	8	—	10	—	13	—	15	—	ns
t_{SD}	Data Setup to Write End	7	—	7	—	9	—	10	—	12	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	7	—	8	—	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	0	—	ns

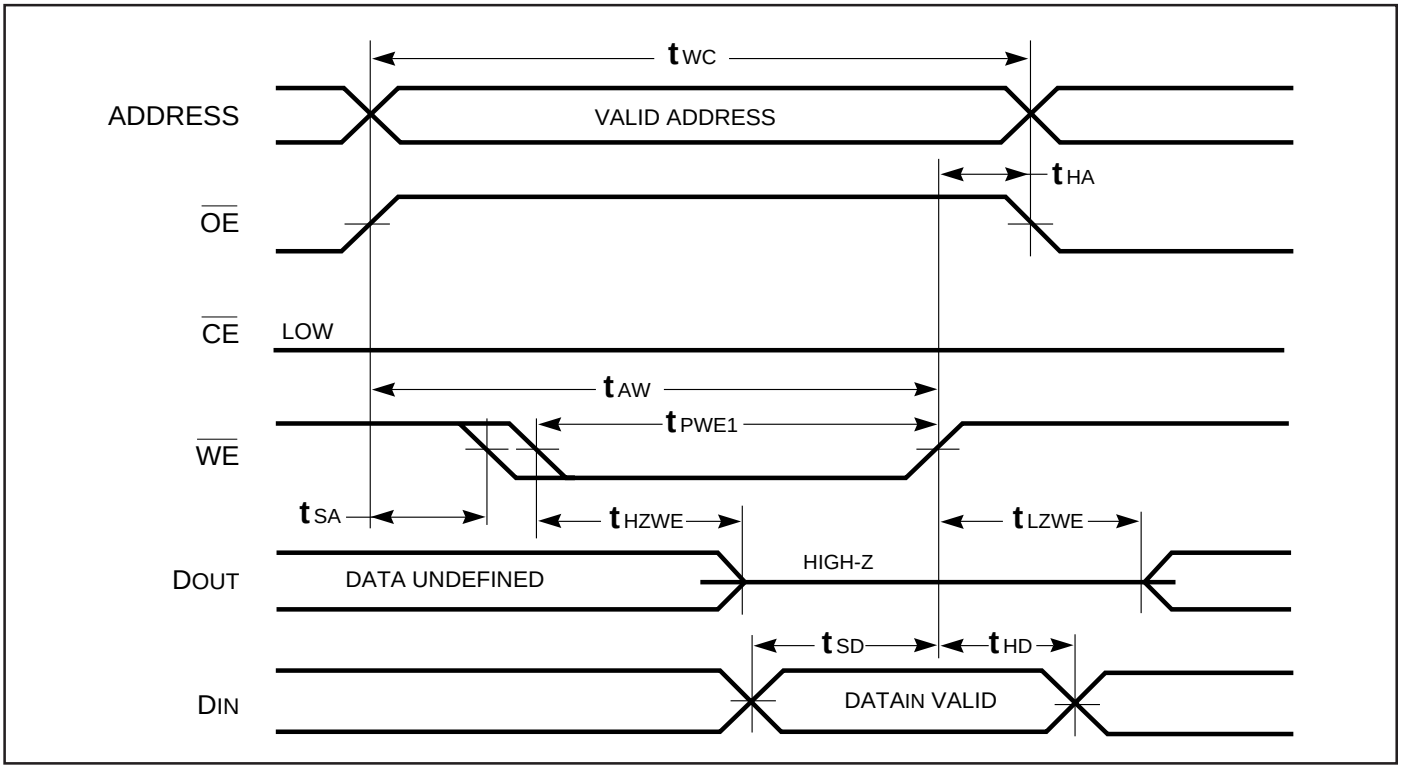
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) [1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled) (1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

ORDERING INFORMATION:
IC61C256AH
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IC61C256AH-10N	300mil DIP
10	IC61C256AH-10J	300mil SOJ
10	IC61C256AH-10T	8*13.4mm TSOP-1
10	IC61C256AH-10U	330mil SOP
12	IC61C256AH-12N	300mil DIP
12	IC61C256AH-12J	300mil SOJ
12	IC61C256AH-12T	8*13.4mm TSOP-1
12	IC61C256AH-12U	330mil SOP
15	IC61C256AH-15N	300mil DIP
15	IC61C256AH-15J	300mil SOJ
15	IC61C256AH-15T	8*13.4mm TSOP-1
15	IC61C256AH-15U	330mil SOP
20	IC61C256AH-20N	300mil DIP
20	IC61C256AH-20J	300mil SOJ
20	IC61C256AH-20T	8*13.4mm TSOP-1
20	IC61C256AH-20U	330mil SOP

ORDERING INFORMATION:
IC61C256AH
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IC61C256AH-12NI	300mil DIP
12	IC61C256AH-12JI	300mil SOJ
12	IC61C256AH-12TI	8*13.4mm TSOP-1
12	IC61C256AH-12UI	330mil SOP
15	IC61C256AH-15NI	300mil DIP
15	IC61C256AH-15JI	300mil SOJ
15	IC61C256AH-15TI	8*13.4mm TSOP-1
15	IC61C256AH-15UI	330mil SOP
20	IC61C256AH-20NI	300mil DIP
20	IC61C256AH-20JI	300mil SOJ
20	IC61C256AH-20TI	8*13.4mm TSOP-1
20	IC61C256AH-20UI	330mil SOP
25	IC61C256AH-25NI	300mil DIP
25	IC61C256AH-25JI	300mil SOJ
25	IC61C256AH-25TI	8*13.4mm TSOP-1
25	IC61C256AH-25UI	330mil SOP

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