Low Power Stereo Audio Codec for Portable Audio/Telephony

FEATURES

- **STEREO AUDIO DAC**
  - **103dB-A SIGNAL-TO-NOISE RATIO**
  - **16/20/24/32-BIT DATA**
  - **SUPPORTS RATES FROM 8-kHz to 96-kHz**
  - **3D/BASS/TREBLE/EQ/DE-EMPHASIS EFFECTS**
- **STEREO AUDIO ADC**
  - **92dB-A SIGNAL-TO-NOISE RATIO**
  - **SUPPORTS RATES FROM 8-kHz TO 96-kHz**
- **TEN AUDIO INPUT PINS**
  - **PROGRAMMABLE IN SINGLE-ENDED OR FULLY DIFFERENTIAL CONFIGURATIONS**
  - **TRI-STATE CAPABILITY FOR FLOATING INPUT CONFIGURATIONS**
- **SEVEN AUDIO OUTPUT DRIVERS**
  - **STEREO 8-OHM 325mW/CHANNEL SPEAKER DRIVE CAPABILITY**
  - **STEREO FULLY-DIFFERENTIAL OR SINGLE-ENDED HEADPHONE DRIVERS**
  - **FULLY DIFFERENTIAL STEREO LINE OUTPUTS**
  - **FULLY DIFFERENTIAL MONO OUTPUT**
- **LOW POWER: 14mW STEREO 48-kHz PLAYBACK WITH 3.3V ANALOG SUPPLY**
- **PROGRAMMABLE INPUT/OUTPUT ANALOG GAINS**
- **AUTOMATIC GAIN CONTROL (AGC) FOR RECORD**
- **PROGRAMMABLE MICROPHONE BIAS LEVEL**
- **PROGRAMMABLE PLL FOR FLEXIBLE CLOCK GENERATION**
- **CONTROL BUS SELECTABLE SPI OR I2C**
- **AUDIO SERIAL DATA BUS SUPPORTS I2S, LEFT/RIGHT-JUSTIFIED, DSP, AND TDM MODES**
- **ALTERNATE SERIAL PCM/I2S DATA BUS FOR EASY CONNECTION TO BLUETOOTH MODULE**
- **DIGITAL MICROPHONE INPUT SUPPORT**
- **EXTENSIVE MODULAR POWER CONTROL**
- **POWER SUPPLIES:**
  - **ANALOG: 2.7V – 3.6V**
  - **DIGITAL CORE: 1.525V – 1.95V**
  - **DIGITAL I/O: 1.1V – 3.6V**
- **PACKAGES: 5X5MM 80-BGA**
  7X7MM 48-QFN

DESCRIPTION

The TLV320AIC33 is a low power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single-ended or fully-differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz DAC playback as low as 15mW(TBD) from a 3.3V analog supply, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC33 contains integrated microphone bias, digitally controlled stereo microphone pre-amp, and automatic gain control (AGC), with mix/mux capability among the multiple analog inputs. The playback path includes mix/mux capability from the stereo DAC and selected inputs, through programmable volume controls, to the various outputs.

The TLV320AIC33 contains four high-power output drivers as well as three fully differential output drivers. The high-power output drivers are capable of driving a variety of load configurations, including up to four channels of single-ended 16-Ω headphones using ac-coupling capacitors, or stereo 16-Ω headphones in a cap-less output configuration. In addition, pairs of drivers can be used to drive 8-Ω speakers in a BTL configuration at 325mW per channel.

The stereo audio DAC supports sampling rates from 8-kHz to 96-kHz and includes programmable digital filtering in the DAC path for 3D, bass, treble, midrange effects, speaker equalization, and de-emphasis for 32-kHz, 44.1-kHz, and 48-kHz rates. The stereo audio ADC supports sampling rates from 8-kHz to 96-kHz and is preceded by programmable gain amplifiers providing up to +59.5-dB analog gain for low-level microphone inputs.

The serial control bus supports SPI or I2C protocols, while the serial audio data bus is programmable for I2S, left/right-justified, DSP, or TDM modes. A highly programmable PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 2-MHz to 50-MHz, with special attention paid to the most popular cases of 12-MHz, 13-MHz, 16-MHz, 19.2-MHz, and 19.68-MHz system clocks.

The TLV320AIC33 operates from an analog supply of 2.7V – 3.6V, a digital core supply of 1.525V – 1.95V, and a digital I/O supply of 1.1V – 3.6V. The device is available in 5x5mm 80-ball u*jr BGA and 7x7mm 48-lead QFN.

SIMPLIFIED BLOCK DIAGRAM

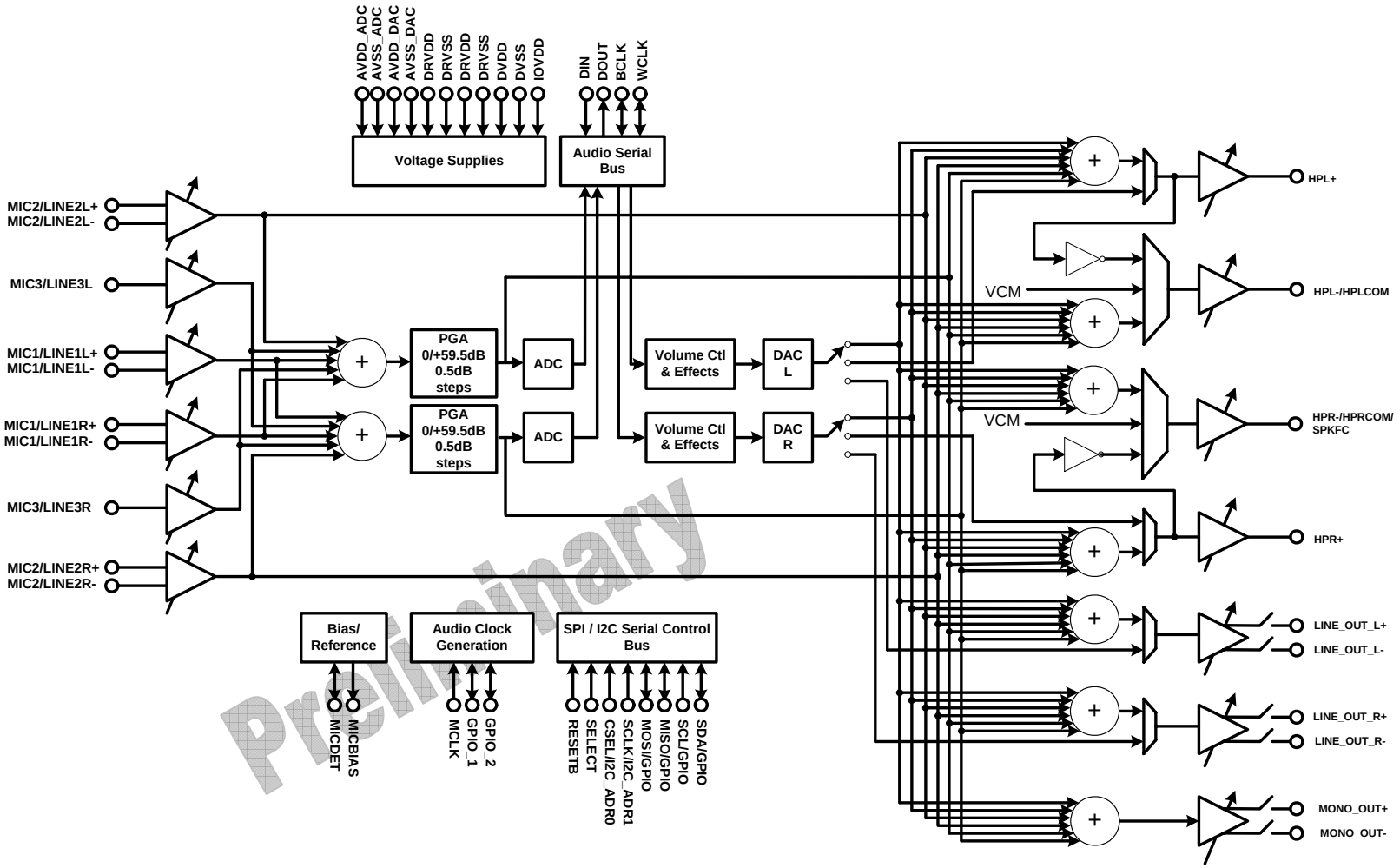
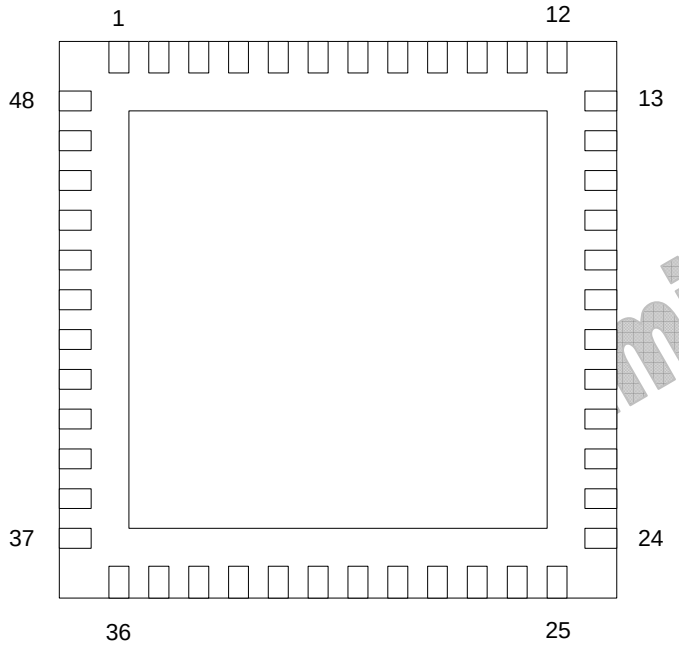


Figure 1. Simplified codec block diagram

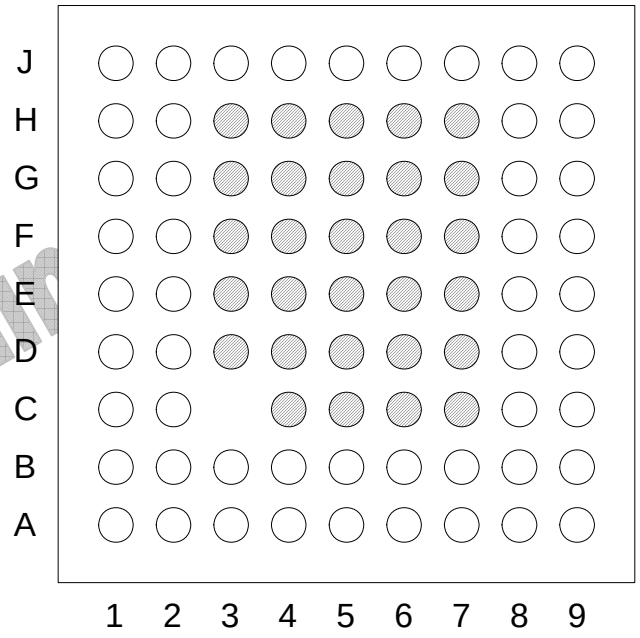
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC33	BGA-80	ZQE	-40C to 85C	TLV320AIC33IZQE	Trays??, xx
				TLV320AIC33IZQER	Tape and Reel, 2000
	QFN-48	RGZ		TLV320AIC33IRGZ	Rails, 52
				TLV320AIC33IRGZR	Tape and Reel, 2000

PIN ASSIGNMENTS



48-lead QFN Package (Bottom view)



5x5mm 80-Ball BGA Package (Bottom View)

(Not to scale)

(Note: Shaded balls on BGA package are not connected to the die, but are electrically connected to each other.)

PIN DESCRIPTION

BGA BALL	QFN PIN NUMBER	PIN NAME	DESCRIPTION
A2	13	MICBIAS	Microphone Bias Voltage Output
A1	14	MIC3R	MIC3 Input (Right or Multifunction)
C2,D2	15	AVSS_ADC	Analog ADC Ground Supply, 0V
B1,C1	16,17	VDDA1	ADC Analog and Output Driver Voltage Supply, 2.7V – 3.6V
D1	18	HPLOUT	High Power Output Driver (Left Plus)
E1	19	HPLCOM	High Power Output Driver (Left Minus or Multifunctional)
E2,F2	20,21	DRVSS	Analog Output Driver Ground Supply, 0V
F1	22	HPRCOM	High Power Output Driver (Right Minus or Multifunctional)
G1	23	HPROUT	High Power Output Driver (Right Plus)
H1	24	VDDA1	ADC Analog and Output Driver Voltage Supply, 2.7V – 3.6V
J1	25	AVDDA2	Analog DAC Voltage Supply, 2.7V – 3.6V
G2,H2	26	AVSS_DAC	Analog DAC Ground Supply, 0V
J2	27	MONO_LOP	Mono Line Output (Plus)
J3	28	MONO_LOM	Mono Line Output (Minus)
J4	29	LEFT_LOP	Left Line Output (Plus)
J5	30	LEFT_LOM	Left Line Output (Minus)
J6	31	RIGHT_LOP	Right Line Output (Plus)
J7	32	RIGHT_LOM	Right Line Output (Minus)
H8	33	/RESET	Reset
J8	34	GPIO2	General Purpose Input/Output #2 (Input/Output) / Digital Microphone Data Input / PLL Clock Input / Audio Serial Data Bus Bit Clock Input/Output
J9	35	GPIO1	General Purpose Input/Output #1 (Input/Output) / PLL/Clock Mux Output / Short Circuit Interrupt / AGC Noise Flag / Digital Microphone Clock / Audio Serial Data Bus Word Clock Input/Output
H9	36	DVDD	Digital Core Voltage Supply, 1.525V – 1.95V
G8	37	MCLK	Master Clock Input
G9	38	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)
F9	39	WCLK	Audio Serial Data Bus Word Clock (Input/Output)
E9	40	DIN	Audio Serial Data Bus Data Input (Input)
F8	41	DOUT	Audio Serial Data Bus Data Output (Output)
D9	42	DVSS	Digital Core / I/O Ground Supply, 0V
E8	43	SELECT	Select Pin (SPI vs I2C Control Mode)
C9	44	IOVDD	I/O Voltage Supply, 1.1V – 3.6V
B8	45	MFP0	Multifunction pin #0 - SPI Chip Select / GPI / I2C Address Pin #0
B9	46	MFP1	Multifunction pin #1 - SPI Serial Clock / GPI / I2C Address Pin #1
A8	47	MFP2	Multifunction pin #2 - SPI MISO Slave Serial Data Output / GPO
A9	48	MFP3	Multifunction pin #3 - SPI MOSI Slave Serial Data Input / GPI / Audio Serial Data Bus Data Input
C8	1	SCL	I2C Serial Clock / GPIO
D8	2	SDA	I2C Serial Data Input/Output / GPIO
A7		NC	No Connect
A6	3	LINE1LP	MIC1 or Line1 Analog Input (Left Plus or Multifunction)

A5	4	LINE1LM	MIC1 or Line1 Analog Input (Left Minus or Multifunction)
B7	5	LINE1RP	MIC1 or Line1 Analog Input (Right Plus or Multifunction)
B6	6	LINE1RM	MIC1 or Line1 Analog Input (Right Minus or Multifunction)
A4	7	LINE2LP	MIC2 or Line2 Analog Input (Left Plus or Multifunction)
B5	8	LINE2LM	MIC2 or Line2 Analog Input (Left Minus or Multifunction)
B4	9	LINE2RP	MIC2 or Line2 Analog Input (Right Plus or Multifunction)
A3	10	LINE2RM	MIC2 or Line2 Analog Input (Right Minus or Multifunction)
B3	11	MIC3L	MIC3 Input (Left or Multifunction)
B2	12	MICDET	Microphone Detect

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

		RATINGS
VDDA1 to VSS, VDDA2 to AVSS_DAC		-0.3V to 3.9V
VDDA1 to DRVSS		-0.3V to 3.9V
IOVDD to DVSS		-0.3V to 3.9V
DVDD to DVSS		-0.3V to 2.5V
VDDA2 to VDDA1		-0.1V to 0.1V
Digital Input Voltage to DVSS		-0.3V to IOVDD+0.3V
Analog Input Voltage to AVSS		-0.3V to AVDD+0.3V
Operating temperature range		-40°C to +85°C
Storage temperature range		-65°C to +105°C
Junction temperature (T_J Max)		+105°C
BGA package	Power dissipation	(T_J Max – T_A) / θ_{JA}
	θ_{JA} Thermal impedance	**TBD**
Lead temperature	Soldering vapor phase (60 sec)	**TBD**
	Infrared (15 sec)	**TBD**

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	**NOM**	**MAX**	**UNIT**
Analog supply voltage VDDA2, VDDA1(2)	2.7	3.3	3.6	V
Digital core supply voltage DVDD(2)	1.525	1.8	1.95	V
Digital I/O supply voltage IOVDD(2)	1.1	1.8	3.6	V
Analog full-scale 0dB input voltage (VDDA2, VDDA1 = 3.3V)		0.707		V_{RMS}
Stereo line output load resistance	10			kΩ
Stereo headphone output load resistance	TBD	16		Ω
Digital output load capacitance		10		pF
Operating free-air temperature, T_A	-40		+85	°C

(2) Analog voltage values are with respect to AVSS_ADC, AVSS_DAC, DRVSS; digital voltage values are with respect to DVSS.

ELECTRICAL CHARACTERISTICS

At 25°C, VDDA1, VDDA2, IOVDD = 3.3V, DVDD = 1.8V, Fs=48-kHz, 24-bit audio data, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
AUDIO ADC					
Input signal level (0-dB)	Single-ended input configuration		0.707		V_{RMS}
Signal-to-noise ratio, A-weighted[3][4]	Fs=48-kHz, 0-dB PGA gain, MIC1/LINE1 inputs selected and AC-shorted together		92		dB
Dynamic range, A-weighted[3][4]	Fs=48-kHz, 1-kHz -60-dB full-scale input applied at MIC1/LINE1 inputs, 0-dB PGA gain		92		dB
Total harmonic distortion	Fs=48-kHz, 1-kHz -1-dB full-scale input applied at MIC1/LINE1 inputs, 0-dB PGA gain		-80		dB
Power supply rejection ratio	1-kHz, 100mVpp on AVDD, DRVDD		TBD		dB
ADC channel separation	1-kHz, -1-dB		TBD		dB
ADC programmable gain amplifier maximum gain	1-kHz input tone, R_{SOURCE}<50Ω		+59.5		dB
ADC programmable gain amplifier step size			0.5		dB
Input resistance	MIC1/LINE1 inputs, Input Mix Attenuation = 0-dB		20		kΩ
Input capacitance	MIC1/LINE1 inputs		10		pF
Input level control minimum attenuation setting			0		dB
Input level control maximum attenuation setting			12		dB
Input level control attenuation step size			1.5		dB
ADC DIGITAL DECIMATION FILTER	**Fs=48kHz**				
FILTER GAIN FROM 0 TO 0.39FS			±0.1		dB
Filter gain at 0.4125Fs			-0.25		dB
Filter gain at 0.45Fs			-3		dB
Filter gain at 0.5Fs			-17.5		dB
Filter gain from 0.55Fs to 64Fs			-75		dB
FILTER GROUP DELAY			17/Fs		Sec
MICROPHONE BIAS 1					
Bias voltage	Programmable settings		2.0 2.5 VDDA1		V
Current sourcing	2.5V setting			4	mA
Output noise voltage	2.5V setting		TBD		nV/√Hz
AUDIO DAC	**Line output, Load = 10kΩ, 50pF**				

0-dB full-scale output voltage	0-dB gain to line outputs. DAC output common-mode setting = 1.35V, output level control gain = 0-dB		1.414		V_{RMS}
Signal-to-noise ratio, A-weighted(5)	Fs=48-kHz, 0-dB gain to line outputs, zero signal applied, referenced to full-scale input level		103		dB
Dynamic range, A-weighted	Fs=48-kHz, 0-dB gain to line outputs, 1-kHz -60-dB signal applied		103		dB
Total harmonic distortion	Fs=48-kHz, 1-kHz -1-dB full-scale signal applied		-80		dB
Power supply rejection ratio	1-kHz, 100mVpp on AVDD_DAC, AVDD_ADC, DRVDD1/2		TBD		dB
DAC channel separation (left to right)	1-kHz, 0-dB		TBD		dB
DAC Digital Interpolation Filter	**Fs = 48-kHz**				
Passband	High-pass filter disabled			0.45*Fs	Hz
Passband ripple	High-pass filter disabled		TBD		dB
Transition band		0.45*Fs		0.55*Fs	Hz
Stopband		0.55*Fs		7.5*Fs	Hz
Stopband attenuation			65		dB
Group delay			21/Fs		Sec
Stereo Headphone Driver	**Pseudo-differential output configuration (5)**				
0-dB full-scale output voltage	0-dB gain to high power outputs. Output common-mode voltage setting = 1.35V		0.707		V_{RMS}
Programmable Output Common Mode Voltage	First option		1.35		V
	Second option		1.50		V
	Third option		1.65		V
	Fourth option		1.8		V
Maximum Programmable Output Level Control Gain			9		dB
Programmable Output Level Control Gain Step Size			1		dB
Maximum output power, P_O	R_L = 32Ω		15		mW
	R_L = 16Ω		30		
Signal-to-noise ratio, A-weighted(6)			95		dB
Total harmonic distortion	1-kHz output, P_O = 10mW		TBD		dB
	1-kHz output, P_O = 20mW		TBD		
Power supply rejection ratio	1-kHz, 100mVpp on AVDD_ADC, AVDD_DAC, DRVDD1/2		TBD		dB
Mute attenuation	1-kHz output		TBD		dB
Digital I/O					

V_{IL} Input low level	I_{IL} = +5-uA		-0.3	0.3 x IOVDD	V
V_{IH} Input high level	I_{IH} = +5-uA		0.7 x IOVDD		V
V_{OL} Output low level	I_{IH} = 2 TTL loads			0.1 x IOVDD	V
V_{OH} Output high level	I_{OH} = 2 TTL loads		0.8 x IOVDD		V
Supply Current	**Fs = 48-kHz**				
Stereo line playback	VDDA1 VDDA2 DVDD	Fs=48-kHz, PLL off, headphone drivers off	TBD TBD TBD		mA
Mono record	VDDA1 VDDA2 DVDD	Fs=48-kHz, PLL and AGC off	TBD TBD TBD		
Stereo record	VDDA1 VDDA2 DVDD	Fs=48-kHz, PLL and AGC off	TBD TBD TBD		
PLL	VDDA1 VDDA2 DVDD	Additional power consumed when PLL is powered	TBD TBD TBD		
Headphone amplifier	VDDA1 VDDA2 DVDD	LINE2LP/RP only routed to single-ended headphones, DAC and PLL off, no signal applied	TBD TBD TBD		
Power down	VDDA1 VDDA2 DVDD	All supply voltages applied, all blocks programmed in lowest power state	TBD TBD TBD		

(3) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(4) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

(5) Unless otherwise noted, all measurements use output common-mode voltage setting of 1.35V, 0-dB output level control gain, 16-ohm single-ended load.

(6) Ratio of output level with a 1-kHz full-scale input, to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

PACKAGING INFORMATION

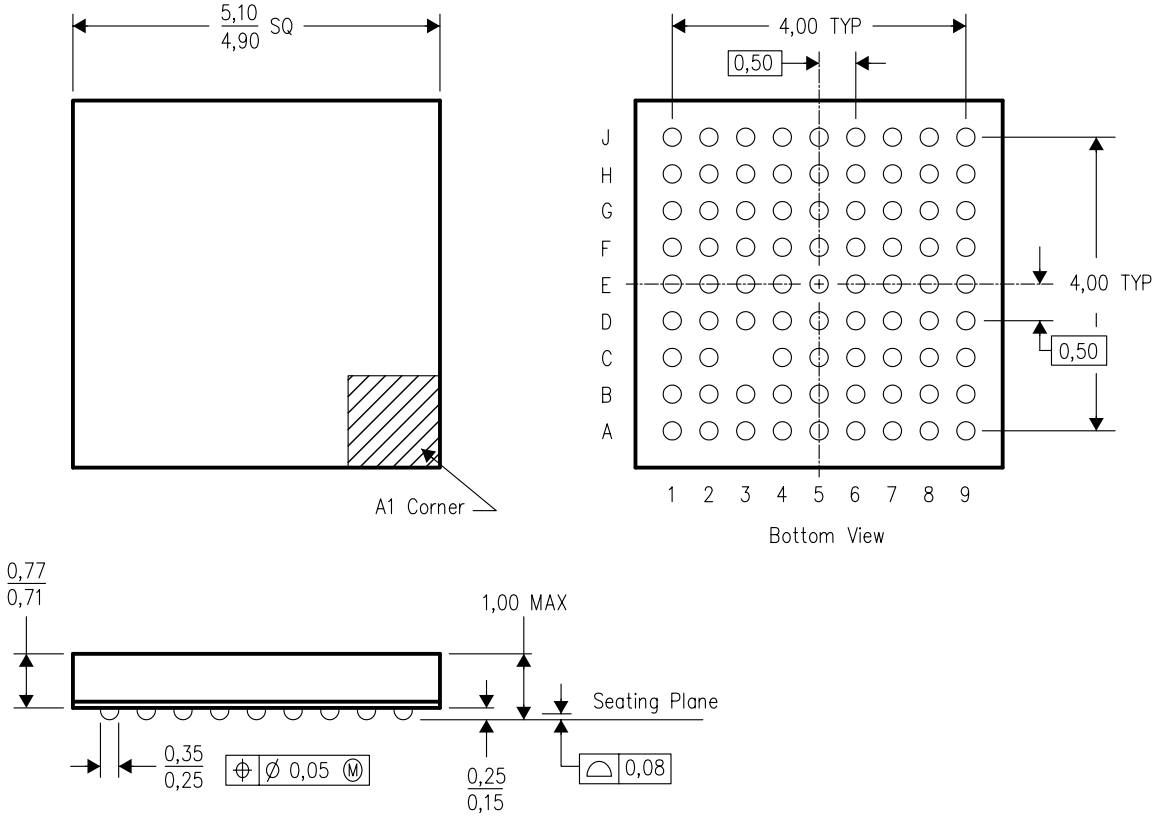
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV320AIC33IGQE	PREVIEW	VFBGA	GQE	80	360	TBD	Call TI	Call TI
TLV320AIC33IGQER	PREVIEW	VFBGA	GQE	80	2500	TBD	Call TI	Call TI
TLV320AIC33IRGZ	PREVIEW	QFN	RGZ	48	250	TBD	Call TI	Call TI
TLV320AIC33IRGZR	PREVIEW	QFN	RGZ	48	2000	TBD	Call TI	Call TI
TLV320AIC33IZQE	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80	360	TBD	Call TI	Call TI
TLV320AIC33IZQER	PREVIEW	BGA MICROSTAR JUNIOR	ZQE	80	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

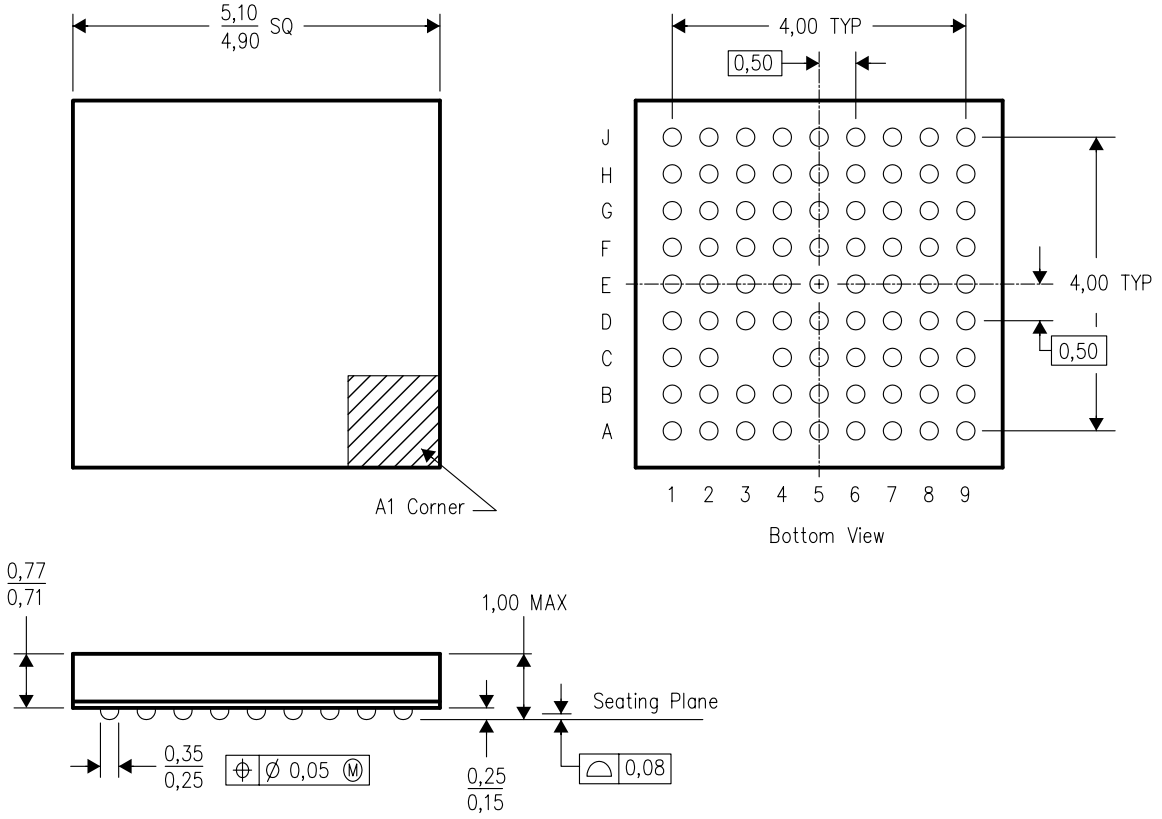
ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–4/D 10/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

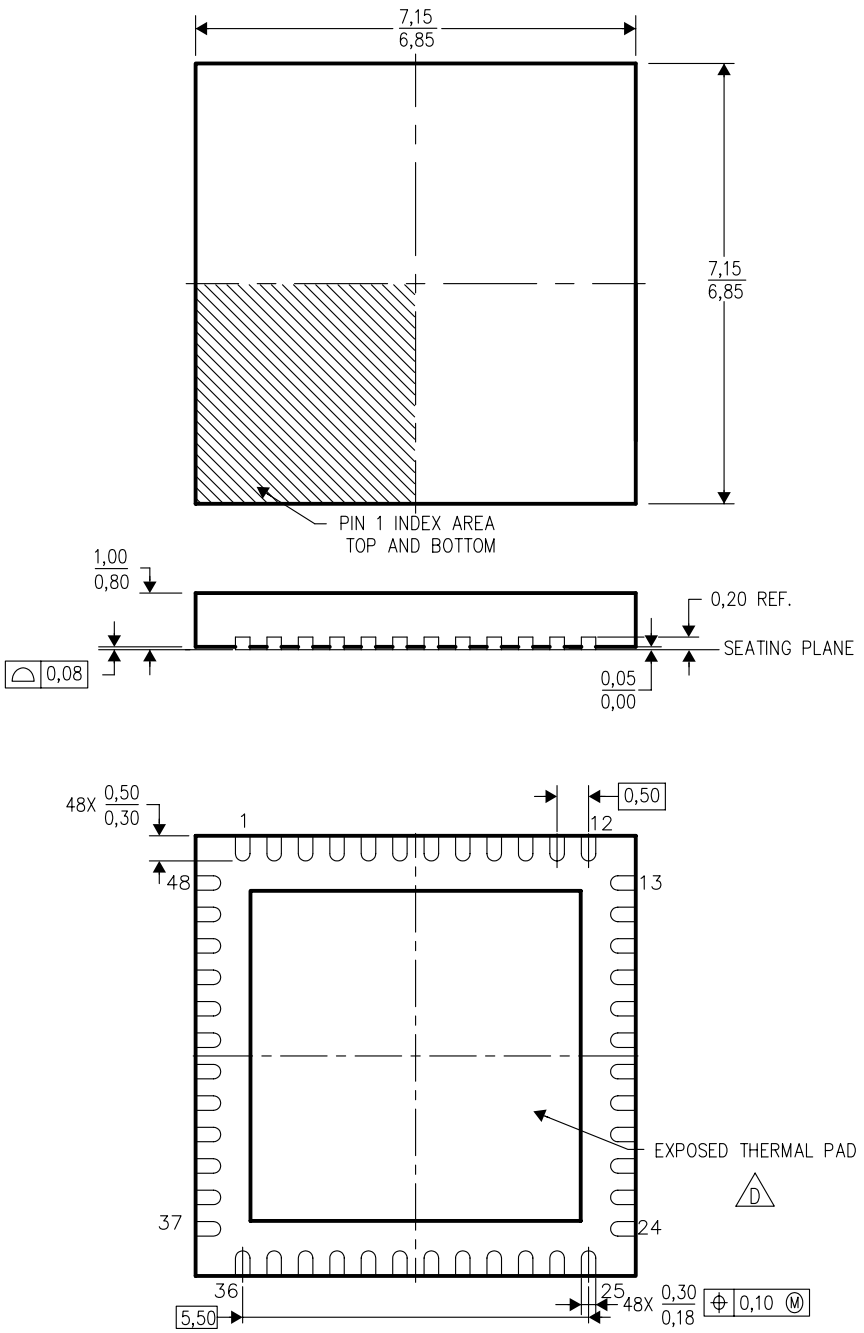
GQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4200461–4/G 10/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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