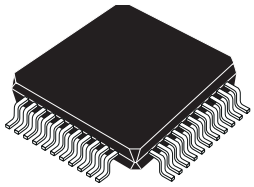
STA001

RF FRONT-END FOR DIGITAL RADIO

PRODUCT PREVIEW

- SINGLE CHIP RECEIVER FOR SATELLITE DIGITAL TRANSMISSION
- SUPERHETERODYNE RECEIVER WITH IF OUTPUT
- HIGH INPUT INTERCEPT POINT, LOW MIXER NOISE
- 54dB IF VGA GAIN RANGE
- ADJUSTABLE RF GAIN
- ADJUSTABLE IF GAIN
- INTEGRATED RF VCO
- INTEGRATED IF VCO
- INTEGRATED SYNTHESIZER
- I^2CBUS COMPATIBLE PROGRAMMING INTERFACE
- UNREGULATED 2.7 V TO 3.3V VOLTAGE SUPPLY
- LOW COST EXTERNAL COMPONENTS



TQFP44
ORDERING NUMBER: STA001

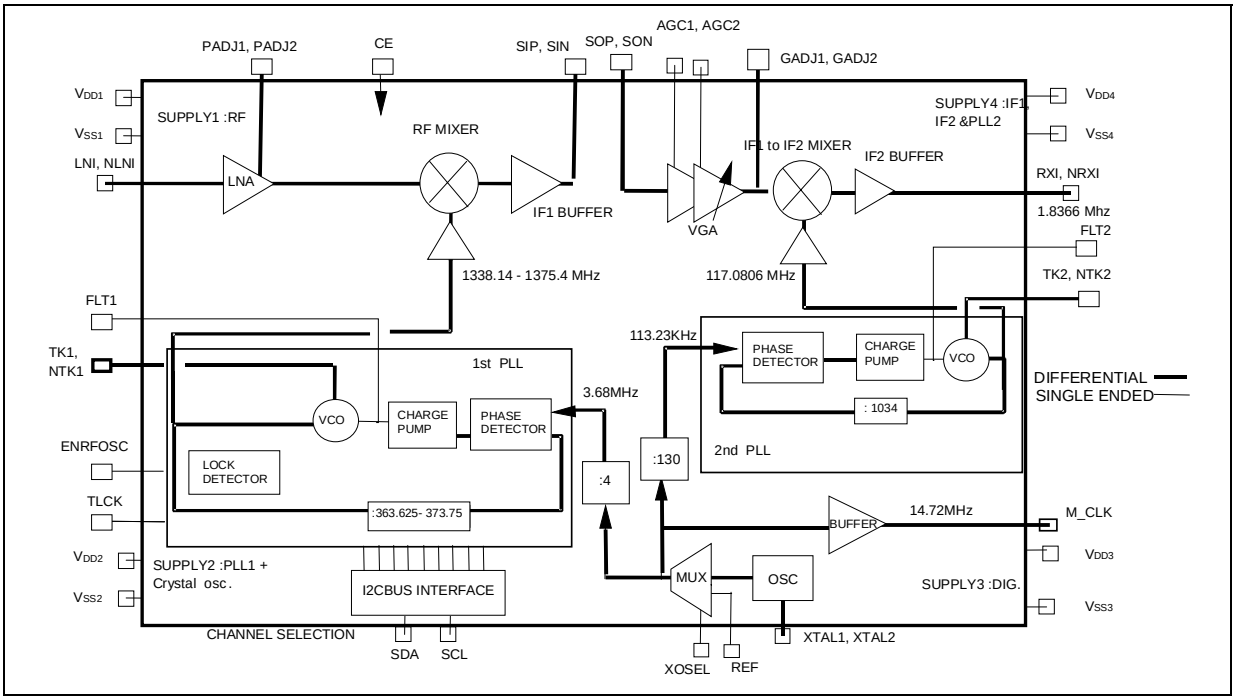
DESCRIPTION

The STA001 is an RF IC using STMicroelectronics HSB2 High Speed Bipolar Technology for one chip solution for the Starman digital satellite radio receiver.

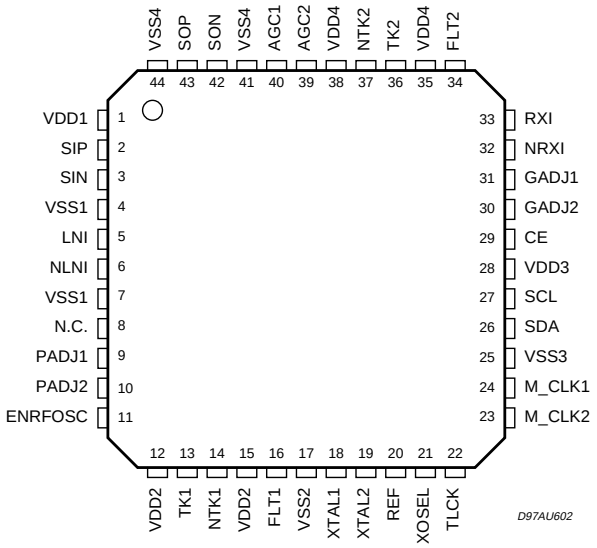
The STA001 is assembled in a TQFP44 package. The frontend architecture is a double conversion receiver (see block diagram) .

The chip includes all the RF functions up to low IF and manages the signals to and from the baseband.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN FUNCTION

N°	Pin	Function
1	VDD1	Positive supply 1
2	SIP	SAW filter input connection
3	SIN	SAW filter input connection
4	VSS1	Negative supply 1
5	LNI	RF input
6	NLNI	RF input
7	VSS1	Negative supply 1
8	NC	Not connected
9	PADJ1	RF gain adjust connection 1
10	PADJ2	RF gain adjust connection 2
11	ENRFOSC	RF Oscillator enable
12	VDD2	Positive supply 2
13	TK1	1st PLL tank connection 1
14	NTK1	1st PLL tank connection 2
15	VDD2	Positive supply 2
16	FLT1	1st PLL loop filter connection
17	VSS2	Negative supply 2
18	XTAL1	Quartz oscillator connection 1
19	XTAL2	Quartz oscillator connection 2
20	REF	External optional TCXO input
21	XOSEL	Internal/external XO selection
22	TLCK	Lock detector output

PIN FUNCTION (continued)

N°	Pin	Function
23	M_CLK2	Master clock differential output 1
24	M_CLK1	Master clock differential output 2
25	VSS3	Negative supply 3
26	SDA	Data serial input
27	SCL	Clock input
28	VDD3	Positive supply 3
29	CE	Chip Enable
30	GADJ2	IF gain adjust connection 2
31	GADJ1	IF gain adjust connection 1
32	NRXI	Low IF Signal output 2
33	RXI	Low IF Signal output 1
34	FLT2	2nd PLL loop filter connection
35	VDD4	Positive supply 4
36	TK2	2nd PLL tank connection
37	NTK2	2nd PLL tank connection
38	VDD4	Positive supply 4
39	AGC2	VGA control pin 2
40	AGC1	VGA control pin 1
41	VSS4	Negative supply 4
42	SON	SAW filter output connection
43	SOP	SAW filter output connection
44	VSS4	Negative supply 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{stg}	Storage temperature	-40 , +125	°C
T_{oper}	Operative ambient temperature	-20 , +85	°C
V_{max}	Maximum voltage on any pin (with the exception of CE, SDA, SDL)	VDD+0.3	V
V_{min}	Minimum voltage on any pin	GND-0.3	V
V_{maxi}	Maximum voltage on pins CE, SDA, SDL	VDD+0.6	V
VDD_{max}	Minimum/Maximum power supply between $VDD_{1,2,3,4}$ and $VSS_{1,2,3,4}$	-0.3/5.5	V
V_{esd}	Electrostatic Discharge Voltage (ESD)	2	KV

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VDD	Operating voltage	2.7, 3.3	V
T_{jun}	Junction temperature	-30, +95	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{Th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient (1)	45	°C/W

(1) According to JEDEC specification on a 4 layers board

ELECTRICAL CHARACTERISTCS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENTS (T_{amb} = 25°, VDD = 3V)						
I_{CC1}	Current supplied by VDD1	Powered circuits: LNA, RF mixer, IF buffer	9.5	14	17	mA
I_{CC2}	Current supplied by VDD2	Powered circuits: RF pll, Crystal Oscillator. ENRFOSC=high (IC RF Osc. Enabled), XOSEL=high (IC XO Enabled)	8.5	10	12	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=high (IC XO Enabled)	3	5	6	mA
		ENRFOSC=high (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)	7.5	9	11	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=low (IC XO Disabled)	2	4	5	mA
I_{CC3}	Current supplied by VDD3	Powered circuits: Digital cells	12	15	18	mA
I_{CC4}	Current supplied by VDD4	Powered circuits: VGA, IF mixer, output buffer, IF pll. V(AGC1)=V(AGC2)=1.2 (IF_{gain}=75dB)	7	11	14	mA
I_{TOT}	I_{CC1}+ I_{CC2}+ I_{CC3}+ I_{CC4}	ENRFOSC=high (IC RF Osc. Enabled), XOSEL=high (IC XO Enabled)	40	50	61	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=high (IC XO Enabled)	34	45	55	mA
		ENRFOSC=high (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)	39	49	60	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=low (IC XO Disabled)	34	44	54	mA
I_{TOTSB}	Standby I_{CC1}+ I_{CC2}+ I_{CC3}+ I_{CC4}	CE=GND			100	µA
LNA, RF MIXER AND IF1 BUFFER (T = 25°, VDD-VSS = 3V)						
BW_i	Input signal BW		1452		1492	MHz
BW_o	Output signal BW		114		116.5	MHz
G_V	Voltage Gain	Input LNI, NLNI pins; output SIP, NIP pins. R_L = 200Ω, PADJ1, PADJ2 floating	28	30	33	dB

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{Vtrim}	Minimum Voltage Gain	Input LNI, NLNI pins; output SIP, NIP pins. R_L = 200Ω, R_{ext}=0	22	25	28	dB
Z_i	Input impedance R || C	Balanced, LNI, NLNI pins		75 0.2		Ω pF
Z_o	Output impedance	Balanced, SIP, SIN pins		50		Ω
R_l	Input Return Loss	LNI, NLNI pins		14		dB
IIP3	Input IP3	Input LNI, NLNI pins; output SIP, NIP pins, R_l=200Ω, PADJ1, PADJ2 floating	-20		-15	dBm
$IIP3_{trim}$	Input IP3 minimum gain	Input LNI, NLNI pins; output SIP, NIP pins, R_l=200Ω, R_{ext}=0 on PADJ1, PADJ2	-19.5		-11.5	dBm
1dBcp	Input 1 dB compression point	Input LNI, NLNI pins; output SIP, NIP pins, R_l=200Ω, PADJ1, PADJ2 floating		-26		dBm
$1dBcp_{trim}$	Input 1 dB compression point	Input LNI, NLNI pins; output SIP, NIP pins, R_l=200Ω, PADJ1, PADJ2 R_{ext}=0 on PADJ1, PADJ2		-24		dBm
NF	Noise figure contribution	Measurement conditions: Input LNI, NLNI pins; output SIP, NIP pins. R_S=50Ω, R_l=200Ω, DSB, PADJ1, PADJ2 floating		5		dB
NF_{trim}	Noise figure contribution minimum gain	Measurement conditions: Input LNI, NLNI pins; output SIP, NIP pins. R_S=50Ω, R_l=200Ω, DSB, R_{ext}=0 on PADJ1, PADJ2		6.5		dB
$IF1_{leak}$	LO1 to IF1 leakage		-100		-25	dBm
RF_{leak}	LO1 to RF leakage		-100		-30	dBm
V_{DC}	LNI, NLNI common mode DC voltage	AC coupled to the Balun	V_{DD}-1.2	V_{DD}-1	V_{DD}-0.8	V
V_{DC}	SIP, SIN common mode DC voltage	AC coupled to the SAW filter	V_{DD}-1.3	V_{DD}-1.1	V_{DD}-0.9	V

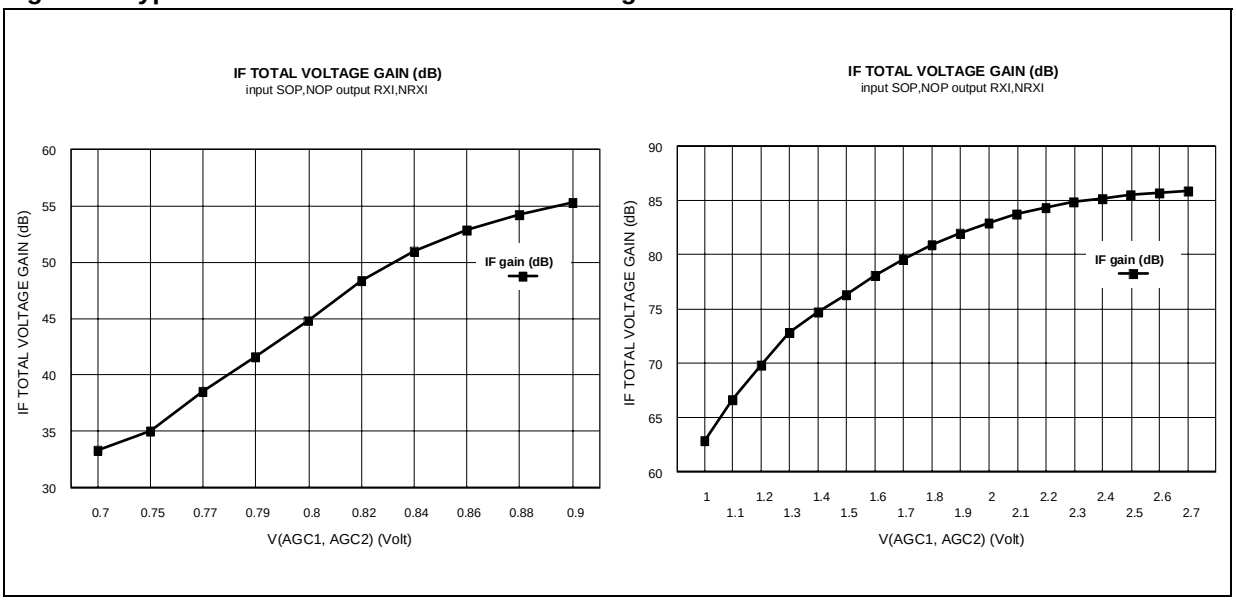
IF VGA AMPLIFIER, IF MIXER AND OUTPUT BUFFER (T = 25°, VDD-VSS = 3V)

BW_i	Input signal BW		114		116.5	MHz
BW_o	Output signal BW		0.6		3.1	MHz
G_{min}	Minimum gain	Input LNI, NLNI pins; output SIP, NIP pins. Rl=high impedance V($AGC_{1,2}$)=0V		32	37	dB
G_{max}	Maximum gain	Input LNI, NLNI pins; output SIP, NIP pins. Rl=high impedance V($AGC_{1,2}$)=3V	71	86		dB
I_{AGC}	Input current in AGC control pin			10		µA
Z_{AGC}	AGC pin input impedance			600		KΩ

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NF	Noise figure contribution	Measurement conditions: Input SIP, NIP pins; output SOP, NOP pins. R_S=50Ω, R_l=200Ω, DSB, Gain = 65dB		9		dB
1dBcp	Input 1 dB compression point	Gain = 65dB		-50		dBm
$1dBcp_{fg}$	Input 1 dB compression point full gain	Gain = 81dB		-66		dBm
IIP3	Input IP3	Gain = 65dB		-41		dBm
$IIP3_{fg}$	Input IP3 full gain	Gain = 81dB		-57		dBm
Z_{in}	Input impedance	Balanced, SOP, SON pins		50		Ω
Z_{out}	Output impedance	Balanced, RXI, NRXI pins (see fig. 9)		200		Ω
V_{DC}	SOP, SON common mode DC voltage	AC coupled to the SAW filter	V_{DD}-1.2	V_{DD}-1	V_{DD}-0.8	V
V_{DC}	RXI, NRXI common mode DC voltage		V_{DD}-2.1		V_{DD}-1.36	V
V_{DC}	GADJ1, GADJ2 common mode DC voltage		V_{DD}-0.15	V_{DD}-0.12	V_{DD}	V
Z_{adj}	Gain adjustment pins impedance	Balanced, GADJ1, GADJ2 pins		800		Ω
BB_{leak}	LO2 to BB leakage	Obtained using low pass filter at the output		-45		dBm
$IF2_{leak}$	LO2 to IF2 leakage	Obtained with SAW filter connected to IF port	-100		-30	dBm
IM3	Third order IM product	V_{out}=1V_{DDp}		-30		dBc

Figure 1. Typical IF Overall Gain vs Control Voltage



ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CRYSTAL OSCILLATOR (T = 25°, VDD-VSS = 3V)						
V_{DC}	XTAL1, XTAL2 common mode DC voltage	XOSEL high	V_{DD}-1.1		V_{DD}-0.68	V
PLLs, SYNTHESIZERS (T = 25°, VDD-VSS = 3V)						
t_s	RF pll loop settling time	within 1 KHz final freq. Offset, by using the loop filter of Application board		1		ms
P_n	Total phase noise contribution	100Hz < Δf < 1.84Mhz, $Q_{rf\_tank} \geq 20$, $Q_{if\_tank} \geq 20$		1.6		deg_{rms}
f_{REF1}	RF pll comparation frequency			3.68		MHz
f_{REF2}	IF pll comparation frequency			113.23		KHz
P_{SP}	Spurious power level***	RF pll, Δf_C=n*460KHz n=1,2.. IF pll, Δf_C=113.23KHz	 -100	-50	 -45	dBc dBc
N_{prog1}	RF PLL selectable division ratios	from REF1 to LO1, range covered by a 0.5 step, using a 14.72MHz quartz	1443 (first used 1454.5)		1506.5 (last used 1495)	
N_{prog2}	RF PLL selectable division ratios	from REF1 to LO1, range covered by a 0.5 step, using a 14.725MHz quartz	1443 (first used 1454)		1506.5 (last used 1494.5)	
N_{fix}	IF PLL fixed division ratios	from REF2 to LO2, 1 fixed +2 testing values	987	1034	1081	
N_{REF1}	REF1 division ratio	from Crystal oscillator to REF1		4		
N_{REF2}	REF2 division ratio	from Crystal oscillator to REF2		130		

*** Using loop filter as suggested in application board schematics

RF VCO (T = 25°, VDD-VSS = 3V)

f_{LO1_1}	LO Freq. range	Using 14.72Mhz quartz	1338.14		1375.4	MHz
f_{LO1_2}	LO Freq. range	Using 14.725Mhz quartz	1338.134375 to 1375.407031			MHz
V_{FLT1}	Freq. control voltage range	Pin FLT1	V_{SS} + 0.2		V_{DD} - 0.2	V
V_{DC}	TK1, NTK1 DC voltage	ENRFOSC high	V_{DD}-1.3	V_{DD}-1.1	V_{DD}-0.65	V
Z_i	Input impedance R || C	Balanced, TK1, NTK1 pins		300 0.2		Ω pF

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IF VCO (T = 25°, VDD-VSS = 3V)						
f_{LO2_1}	LO Freq.	Using a 14.72MHz quartz, Min. and Max. Values are optional fixed frequency usable for testing purposes.	111.76	117.08	122.4	MHz
f_{LO2_2}	LO Freq.	Using a 14.725MHz quartz, Min. and Max. Values are optional fixed frequency usable for testing purposes.	111.8	117.12	122.44	MHz
V_{FLT2}	Freq. control voltage range	FLT2 pin	V_{SS} + 0.2		V_{DD} - 0.2	V
DIGITAL INTERFACE TO MP (SCL, SDA, TLCK) AND XOSEL INTERFACE (T = 25°, VDD-VSS = 3V)						
INPUT PARAMETERS (SCL, SDA)						
V_{IH}	digital input signals	high	V_{DD}-1		V_{DD}	V
V_{IL}		low	V_{SS}		V_{SS}+0.7	V
I_{IH}	Input current High			10		µA
I_{IL}	Input current Low			-40		µA
T_t	Input edge transition			0.1		µs/V
R_{in}	Input resistance			190K		Ω
OUTPUT PARAMETERS (TLCK)						
V_{OH}	digital output signals	high	V_{DD}-0.5		V_{DD}	V
V_{OL}		low	V_{SS}		V_{SS}+0.5	V
t_r	Rise time	Cl=5pF		0.4		µs/V
t_f	Fall time	Cl=5pF		0.4		µs/V
DIFFERENTIAL DIGITAL INTERFACE (M_CLK1, M_CLK2) (T = 25°, VDD-VSS = 3V)						
V_{OH}	digital output signals, V(M_CLK1) - V(M_CLK2)	high		0.2		V
V_{OL}		low		-0.2		V
V_{DC}	M_CLK1, M_CLK2 common mode DC voltage		V_{DD}-1.12		V_{DD}-0.7	V
t_r	Rise time	Cl=5pF each pin		10		ns
t_f	Fall time	Cl=5pF each pin		10		ns
Z_{out}	Output impedance	balanced		500		Ω

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{M_CLK1}	M_CLK frequency	Using a 14.72MHz quartz		14.72		MHz
f_{M_CLK2}	M_CLK frequency	Using a 14.725MHz quartz		14.725		MHz

ADDITIONAL DIGITAL INTERFACE (CE) (T = 25°, VDD-VSS = 3V)
(LOW=GND, HIGH=VDD)

V_{IH}	digital input signals	high	V_{SS}+1.8			V
V_{IL}		low			V_{SS}+1.3	V
t_r	CE power up time			2		µs
t_f	CE power down time			6		µs

XOSEL, CE, TLCK, ENRFOSC TRUTH TABLE (LOW = GND, HIGH = VDD)

Pin	Type	Level	Result
CE	input	high	Chip enabled
		low	Chip disabled
XOSEL	input	high	Internal Crystal oscillator selected
		low	External TCXO connected on REF selected
ENRFOSC	input	high	Internal RF oscillator selected
		low	External RF oscillator connected on TK1, NTK1 pins
TLCK	output	high	Synth. locked
		low	Synth. unlocked

ADDITIONAL OPTIONAL INTERFACE INFORMATION (REF)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DC}	REF DC voltage	XOSEL low	V_{DD}-1.1	V_{DD}-0.9	V_{DD}-0.7	V
R_{in}	Input resistance	XOSEL low		70K		Ω

FUNCTIONAL DESCRIPTION

Receiver chain

The receiver chain transforms the RF frequency signals to an IF signal at 1.84 MHz Carrier directly usable by the Channel decoder.
In front of the STA001 IC it can be placed an external LNA and a bandpass filter; the bandpass filter limitates the input bandwidth and guarantees a suitable rejection to the image frequency.
The STA001 input stage is a LNA working in the 1452-1492 MHz band. The RF signal is downconverted, using an active mixer, to a first IF of 115.244 MHz. The first LO is tunable with a frequency step of 460 KHz.
The RF can be reduced 5dB by an external trimmer/resistor connected between PADJ1 and PADJ2 pins.

An IF variable gain amplifier guarantees 54 dB typical of gain range.

Using pins GADJ1, GADJ2, the output RX signal level can be decreased to the desired value by an external trimmer/resistor.

Moreover, the IF chain can be configured to have a fixed gain by fixing statically control voltages on AGC1 and AGC2 pins (i.e. V(AGC1)=VCC and V(AGC2)=GND), and by trimming the gain through connecting an external resistor between GADJ1 and GADJ2.

By using an 800 Ohm resistor connected between GADJ1 and GADJ2, for example, a typical 56 dBs IF static gain is obtained.

The first IF signal, having a bandwidth of 2.5 MHz, shaped by an external SAW filter, is downconverted to a second IF of 1.84 MHz.

A differential clock output at 14.72 MHz is available to be used from the baseband.

Synthesizers, PLL, charge pump and VCOs

The first Voltage controlled Oscillator is controlled by an integrated PLL and it's able to cover a frequency range of 37MHz with a step size of 460 KHz.

The second Voltage controlled oscillator produces a fixed 117.08MHz frequency controlled by a second integrated PLL. Moreover, the 2nd PLL is able to select 2 other fixed frequencies, i.e. 111.76MHz and 122.4MHz, suitable for application test.

The other components of the first PLL synthesizer are a low frequency programmable divider and a dual modulus prescaler; a fixed dividers is instead used to synthesize the second VCO frequency. Other fixed internal dividers are used to get the comparation frequencies of both loops.
Channel selection is made through the I^2CBUS interface , directly from the µP.

POWER SUPPLIES

The chip operates from an unregulated power supply of 2.7 to 3.3 Volts. All interface circuits to the baseband chips are operating between these supplies unless otherwise specified.

INTERFACE SPECIFICATION

All the interface voltage levels to the micro controller are referenced to the supply voltage of the interface power supply (GND) . The interface voltage levels are therefore fully compatible with the base band circuits.
The digital levels are all CMOS threshold compatible with the exception of M_CLK1, M_CLK2 pins (ECL type).
For completeness all other interface signals are also included.

I^2C BUS INTERFACE

Data transmission from microprocessor to the STA001 takes place through the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected to SDA and SCL).

Data Validity

The data on the SDA line must be stable during the high period of the clock. The HIGH to LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte format

Every byte transferred on the SDA line must contains bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The peripheral (STA001) that acknowledges has to pull-down (LOW) the SDA line during the clock pulse.

The STA001 which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at at the HIGH level during the ninth clock pulse time. In this case the µP can generate the STOP information in order to abort the transfer.

Transmission without acknwoledge

Avoiding to detect the acknowlegde of the STA001, the µP can use a simpler transmission: simply it waits one clock period without checking the STA001 acknowledging, and sends the new data.
This approach of course is less protected from misworking.

Figure 2. Validity on the I^2CBUS

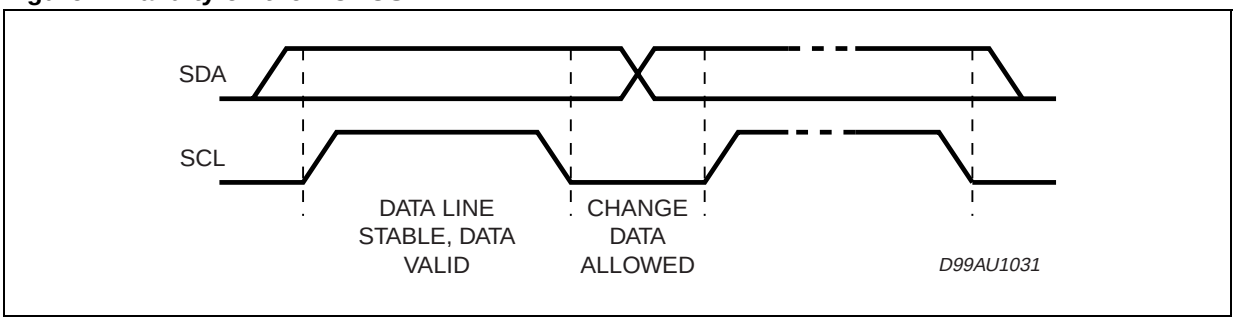


Figure 3. Timing Diagram of the I^2CBUS

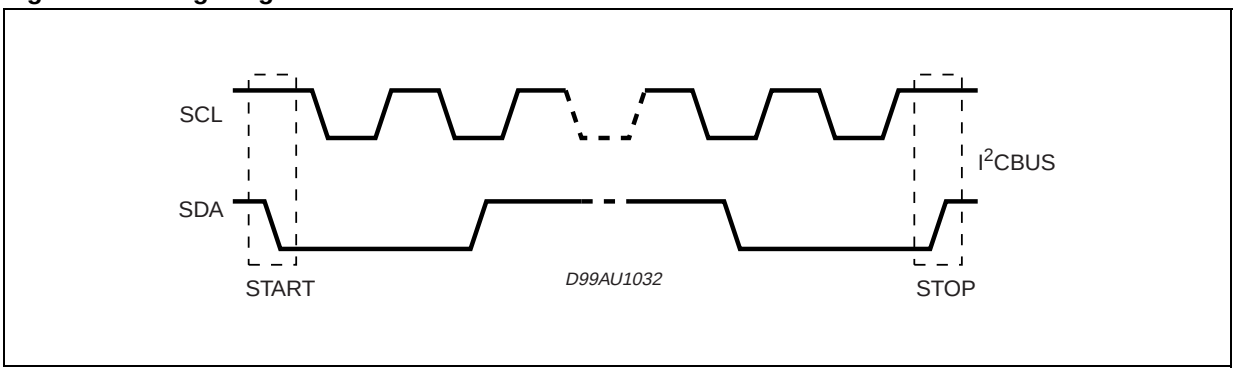
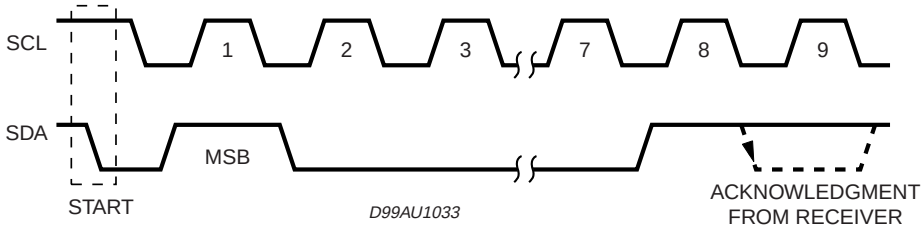
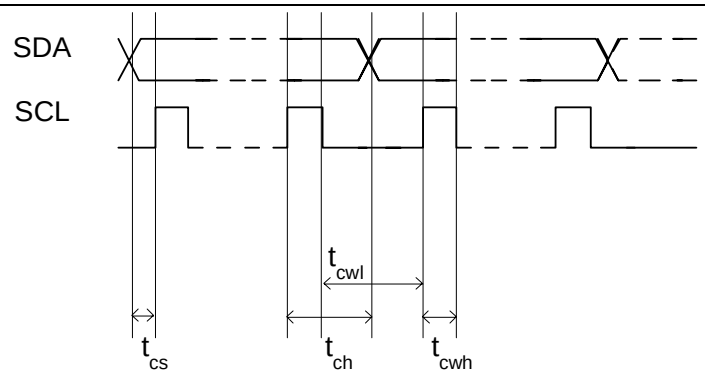


Figure 4. Acknowledge on the I²CBUS



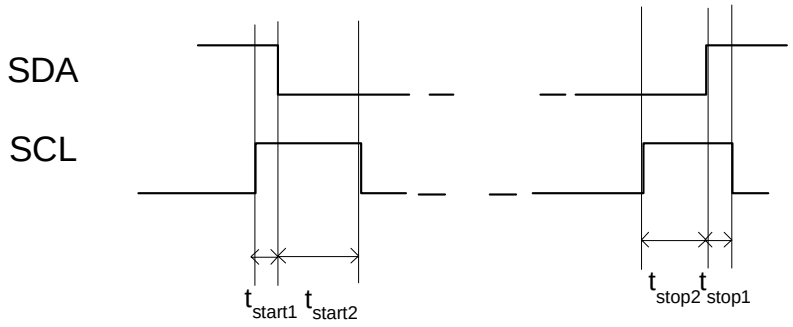
TIMING SPECIFICATION

Figure 5. Data and clock



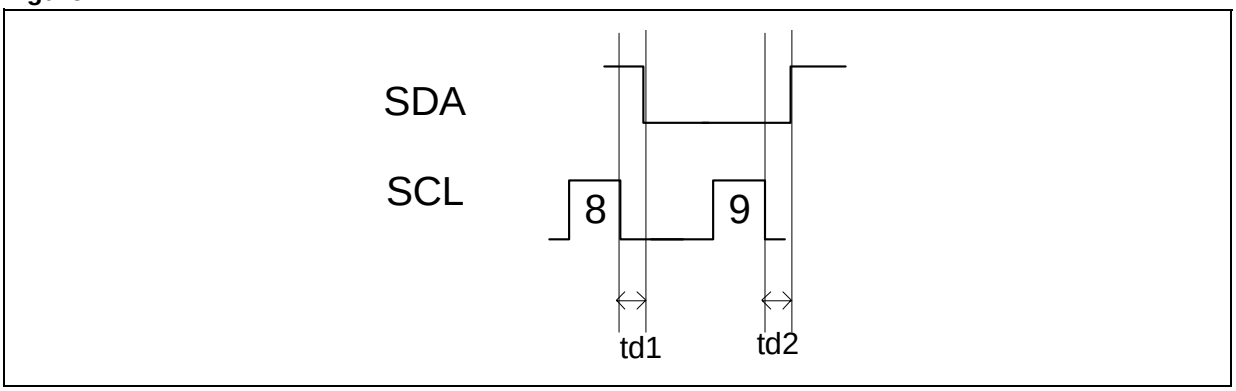
Symbol	Parameter	Minimum time (ns)
t_{cs}	Data to clock set up time	100
t_{ch}	Data to clock hold time	50
t_{cwh}	Clock pulse width high	100
t_{cwl}	Clock pulse width low	100

Figure 6. Start and stop



Symbol	Parameter	Minimum time (ns)
$Tstart_{1,2}$	Clock to data start time	100
$Tstop_{1,2}$	Data to clock down stop time	100

Figure 7.



Symbol	Parameter	Maximum time (ns)
t_{d1}	Ack begin delay	200
t_{d2}	Ack end delay	200

SOFTWARE SPECIFICATION

Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte
- A two data bytes
- A stop condition (P)

MSB chip address LSB MSB 1st data byte LSB MSB 2nd data byte LSB

S	1	1	0	0	0	0	0	0	ack	1	D6	D5	D4	D3	D2	D1	D0	ack	0	D6	D5	D4	D3	D2	D1	D0	ack	P

ack = Acknowledge

S = Start

P = Stop

"Byte by byte" option

A "byte by byte" programming mode is also possible when there is no need to use both data bytes to program the chip (for example during the setup of 2nd PLL).

To use this feature remember that first bit of both data bytes is reserved to chose the destination of the remaining 7 bits.

MSB chip address LSB MSB 1st data byte LSB

S	1	1	0	0	0	0	0	0	ack	K	D6	D5	D4	D3	D2	D1	D0	ack	P

ack = Acknowledge

S = Start

P = Stop

K= destination of the remaining 7bit:

K=1 the data byte has the same function of the 1st data byte in the normal programming mode.

K=0 the data byte has the same function of the 2nd data byte in the normal programming mode.

Table 1. First data byte selection table (selection of synthesizer channel) using a 14.72Mhz quartz

MSB						LSB	RF LO freq. selected	Units	Division ratio selected on synthesizer	Notes
D6	D5	D4	D3	D2	D1	D0			from REF1 to LO1	
0	0	0	0	1	1	0	1324.8+6*0.46 (1327.56)	MHz	360.75	Lowest selectable freq.
0	0	0	0	1	1	1	1324.8+7*0.46	MHz	360.875	
0	0	0	1	0	0	0	1324.8 + 8*0.46	MHz	361	
-	-	-	-	-	-	-				
0	0	1	1	1	0	1	1338.14	MHz	363.625	first used freq.
-	-	-	-	-	-	-	1324.8 + N*0.46 N=(D6..D0) represented decimal number	MHz	360 + N*0.125	general freq. generation rule
1	1	0	1	1	1	0	1375.4	MHz	373.75	Last used freq.
-	-	-	-	-	-	-				
1	1	1	1	1	1	1	1383.22	MHz	375.875	
0	0	0	0	0	0	0	1383.68	MHz	376	
-	-	-	-	-	-	-				
0	0	0	0	1	0	1	1324.8+133*0.46 (1385.98)	MHz	376.625	Highest selectable freq.
1	0	0	0	1	0	1	1356.54	MHz	368.625	Startup presetted data

Table 2. First data byte selection table (selection of synthesizer channel) using a 14.725Mhz quartz

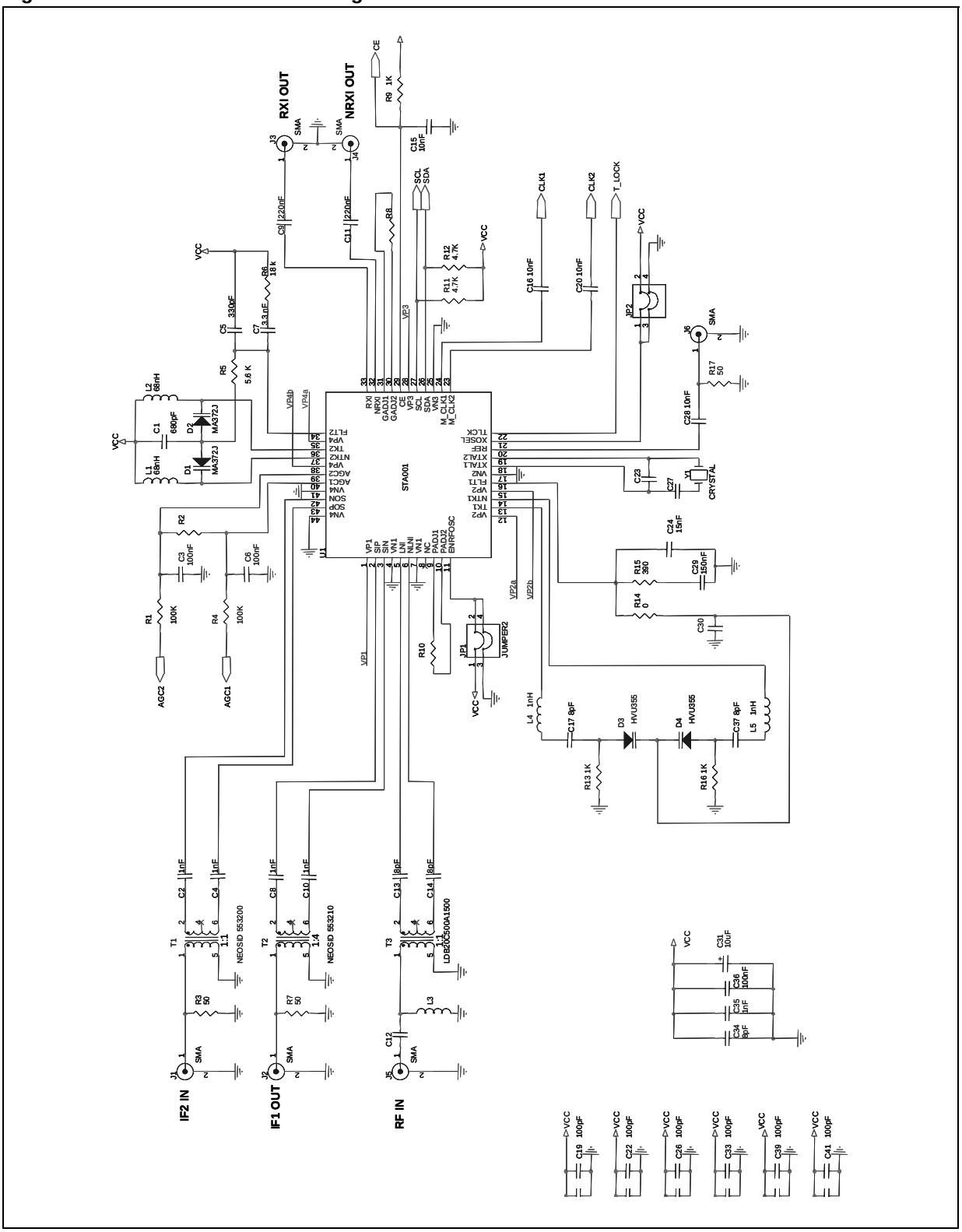
MSB						LSB	RF LO freq. selected	Units	Division ratio selected on synthesizer	Notes
D6	D5	D4	D3	D2	D1	D0			from REF1 to LO1	
0	0	0	0	1	1	0	1325.25 +6*0.46015625 (1328.010938)	MHz	360.75	Lowest selectable freq.
0	0	0	0	1	1	1	1325.25 +7*0.46015625	MHz	360.875	
0	0	0	1	0	0	0	1325.25+ 8*0.46015625	MHz	361	
-	-	-	-	-	-	-				
0	0	1	1	1	0	0	1338.134375	MHz	363.5	first used freq.
-	-	-	-	-	-	-	1325.25+ N*0.46015625 N=(D6..D0) represented decimal number	MHz	360 + N*0.125	general freq. generation rule
1	1	0	1	1	0	1	1375.407031	MHz	373.625	Last used freq.
-	-	-	-	-	-	-				
1	1	1	1	1	1	0	1383.229688	MHz	375.75	
1	1	1	1	1	1	1	1383.689844	MHz	375.875	
-	-	-	-	-	-	-				
0	0	0	0	1	0	1	1325.25 +133*0.46015625 (1386.450781)	MHz	376.625	Highest selectable freq.
1	0	0	0	1	0	1	1357.000781	MHz	368.625	Startup presetted data

Table 3. Second data byte selection table (LOCK test on both pll, dividers test and IF pll test)

MSB						LSB	Working mode	Notes
D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	Lock test on RF pll	lock flag to be tested: TLCK; Startup presetted data
0	0	0	0	1	0	0	Lock test on IF pll	lock flag to be tested: TLCK
0	0	0	0	0	0	1	Lock test on RF and IF pll	lock flag to be tested: TLCK
0	0	1	0	0	1	0	First pll programmable divider test	output freq. divided by 16 available on TLCK
0	0	1	1	0	1	0	First pll reference divider test	output freq. divided by 8 available on TLCK
0	0	1	0	1	1	0	Second pll fixed divider test	output freq. divided by 2 available on TLCK
0	0	1	1	1	1	0	Second pll reference divider test	output freq. available on TLCK
1	0	0	0	0	0	0	Test frequency on IF pll divider by 1034	Division ratio changed to 987
1	1	0	0	0	0	0	Test frequency on IF pll divider by 1034	Division ratio changed to 1081

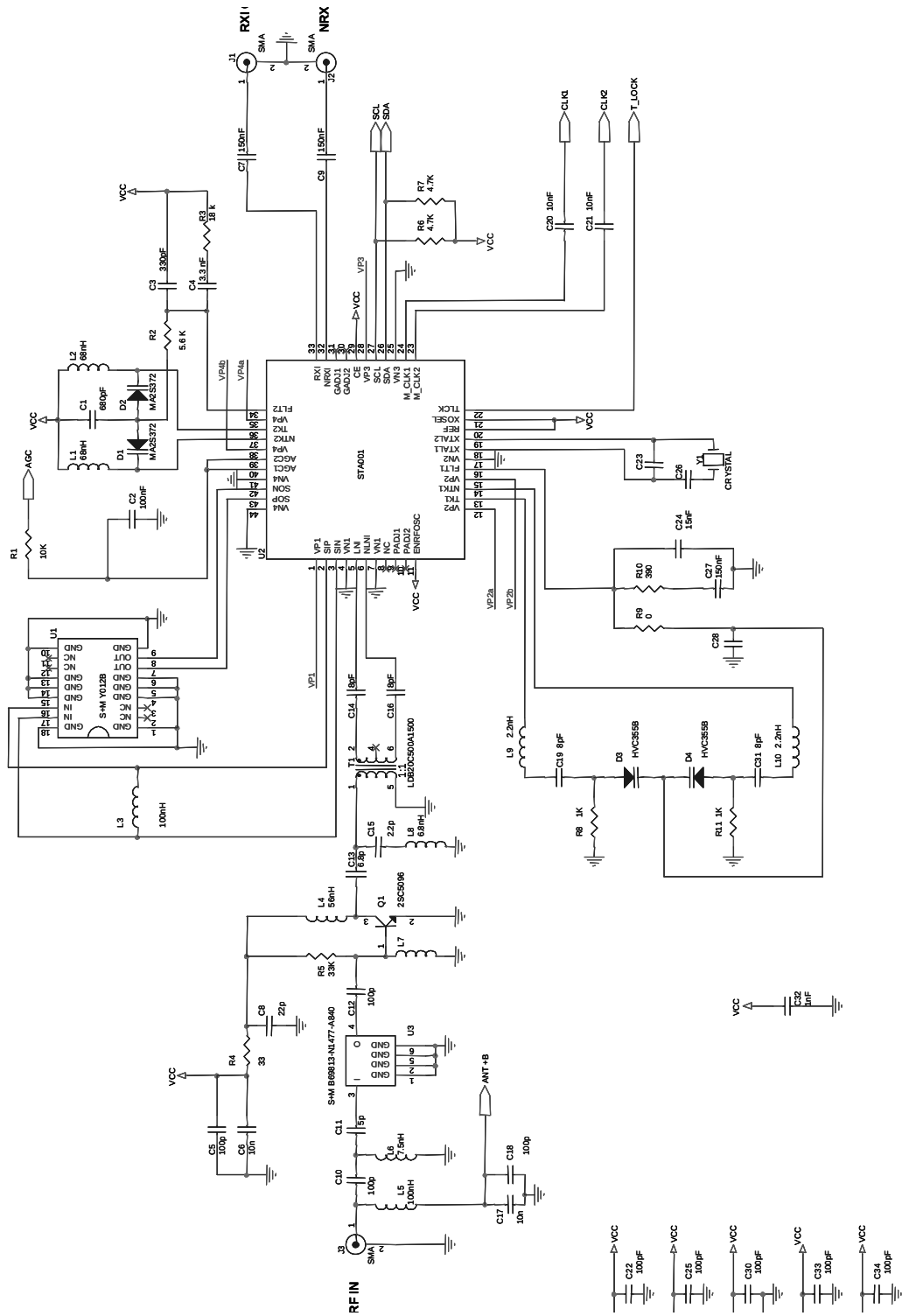
TEST AND APPLICATION BOARD SCHEMATIC

Figure 8. Test Board Schematic Diagram



NOTE: Connect a resistor from10K to 100K between pins PADJ1 (9) and PADJ2 (10) so to obtain intermediate gain between 25 and 30dB

Figure 9. Application Board Schematic Diagram



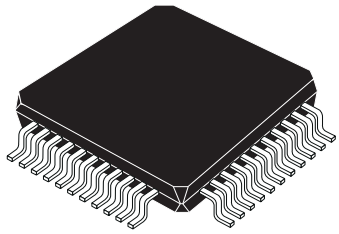
Suggested minimum differential RLoad on RXI and NRXI output 3K

Application note: the crystal oscillator must have the following features:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
CRYSTAL OSCILLATOR (T = 25°, VP-VN = 3V)						
f_{xtal1}	Quartz frequency	- Resonance mode: series - Using a 14.72		14.72		MHz
f_{xtal2}	Quartz frequency	- Resonance mode: series - using a 14.725 quartz		14.725		MHz
P_n	Phase noise	Δf = 1 KHz		-120	-118	dBc/Hz
V_{DC}	XTAL1, XTAL2 common mode DC voltage	XOSEL high	VP-1.1	VP-0.9	VP-0.7	V

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10)