# Si552
## Revision D

# Dual Frequency Voltage-Controlled Crystal Oscillator (VCXO) 10 MHz to 1.4 GHz

## Features

- Available with any-rate output frequencies from 10–945 MHz and selected frequencies to 1.4 GHz
- Two selectable output frequencies
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

**Ordering Information:**

See page 10.

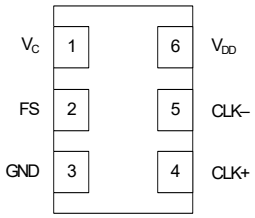
## Applications

- SONET/SDH
- xDSL
- 10 GbE LAN/WAN
- Low-jitter clock generation
- Optical modules
- Clock and data recovery

**Pin Assignments:**

See page 9.

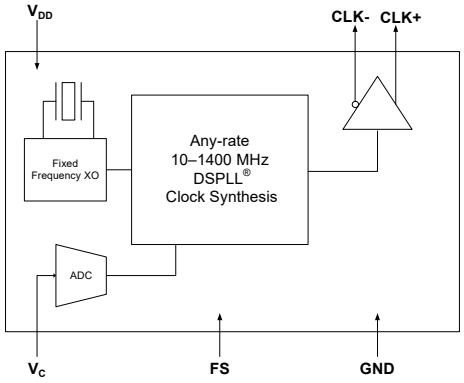
(Top View)




## Description

The Si552 dual-frequency VCXO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a very low jitter clock for all output frequencies. The Si552 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si552 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments typically found in communication systems. The Si552 IC-based VCXO is factory-configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

## Functional Block Diagram





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# 1. Electrical Specifications

### Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply Voltage[1] | $V_{DD}$ | 3.3 V option | 2.97 | 3.3 | 3.63 | V |
| | | 2.5 V option | 2.25 | 2.5 | 2.75 | V |
| | | 1.8 V option | 1.71 | 1.8 | 1.89 | V |
| Supply Current | $I_{DD}$ | Output enabled<br>LVPECL<br>CML<br>LVDS<br>CMOS | <br>—<br>—<br>—<br>— | <br>120<br>108<br>99<br>90 | <br>130<br>117<br>108<br>98 | <br>mA |
| | | Tristate mode | — | 60 | 75 | mA |
| Frequency Select (FS)[2] | | $V_{IH}$ | 0.75 x $V_{DD}$ | — | — | V |
| | | $V_{IL}$ | — | — | 0.5 | V |
| Operating Temperature Range | $T_A$ | | –40 | — | 85 | ºC |

**Notes:**
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 10 for further details.
2. FS pin includes a 17 kΩ resistor to VDD.

### Table 2. $V_C$ Control Voltage Input

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Control Voltage Tuning Slope[1,2,3] | $K_V$ | 10 to 90% of $V_{DD}$ | — | 33<br>45<br>90<br>135<br>180<br>356 | — | ppm/V |
| Control Voltage Linearity[4] | $L_{VC}$ | BSL | –5 | ±1 | +5 | % |
| | | Incremental | –10 | ±5 | +10 | % |
| Modulation Bandwidth | BW | | 9.3 | 10.0 | 10.7 | kHz |
| $V_C$ Input Impedance | $Z_{VC}$ | | 500 | — | — | kΩ |
| Nominal Control Voltage | $V_{CNOM}$ | @ $f_O$ | — | $V_{DD}/2$ | — | V |
| Control Voltage Tuning Range | $V_C$ | | 0 | | $V_{DD}$ | V |

**Notes:**
1. Positive slope; selectable option by part number. See Section 3. "Ordering Information" on page 10.
2. For best jitter and phase noise performance, always choose the smallest $K_V$ that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ($K_V$), Stability, and Absolute Pull Range (APR)" for more information.
3. $K_V$ variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with $V_C$ ranging from 10 to 90% of $V_{DD}$. Incremental slope determined with $V_C$ ranging from 10 to 90% of $V_{DD}$.

### Table 3. CLK± Output Frequency Characteristics

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Nominal Frequency[1,2,3] | $f_O$ | LVDS/CML/LVPECL | 10 | — | 945 | MHz |
| | | CMOS | 10 | — | 160 | MHz |
| Temperature Stability[1,4] | | $T_A$ = –40 to +85 °C | –20<br>–50<br>–100 | —<br>—<br>— | +20<br>+50<br>+100 | ppm |
| Absolute Pull Range[1,4] | APR | | ±12 | — | ±375 | ppm |
| Aging | | Frequency drift over first year. | — | — | ±3 | ppm |
| | | Frequency drift over 15 year life. | — | — | ±10 | ppm |
| Power up Time[5] | $t_{OSC}$ | | — | — | 10 | ms |
| Settling Time After FS Change | $t_{FRQ}$ | | — | — | 10 | ms |

**Notes:**
1. See Section 3. "Ordering Information" on page 10 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Nominal output frequency set by $V_{CNOM} = V_{DD}/2$.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to $f_O$ (to within ±1 ppm of $f_O$).

### Table 4. CLK± Output Levels and Symmetry

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LVPECL Output Option[1] | $V_O$ | mid-level | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| | $V_{OD}$ | swing (diff) | 1.1 | — | 1.9 | $V_{PP}$ |
| | $V_{SE}$ | swing (single-ended) | 0.55 | — | 0.95 | $V_{PP}$ |
| LVDS Output Option[2] | $V_O$ | mid-level | 1.125 | 1.20 | 1.275 | V |
| | $V_{OD}$ | swing (diff) | 0.5 | 0.7 | 0.9 | $V_{PP}$ |
| CML Output Option[2] | $V_O$ | 2.5/3.3 V option mid-level | — | $V_{DD}$ – 1.30 | — | V |
| | | 1.8 V option mid-level | — | $V_{DD}$ – 0.36 | — | V |
| | $V_{OD}$ | 2.5/3.3 V option swing (diff) | 1.10 | 1.50 | 1.90 | $V_{PP}$ |
| | | 1.8 V option swing (diff) | 0.35 | 0.425 | 0.50 | $V_{PP}$ |
| CMOS Output Option[3] | $V_{OH}$ | $I_{OH}$ = 32 mA | 0.8 x $V_{DD}$ | — | $V_{DD}$ | V |
| | $V_{OL}$ | $I_{OL}$ = 32 mA | — | — | 0.4 | V |
| Rise/Fall time (20/80%) | $t_R$, $t_F$ | LVPECL/LVDS/CML | — | — | 350 | ps |
| | | CMOS with $C_L$ = 15 pF | — | 1 | — | ns |
| Symmetry (duty cycle) | SYM | LVPECL: $V_{DD}$ – 1.3 V (diff)<br>LVDS: 1.25 V (diff)<br>CMOS: $V_{DD}/2$ | 45 | — | 55 | % |

**Notes:**
1. 50 Ω to $V_{DD}$ – 2.0 V.
2. $R_{term}$ = 100 Ω (differential).
3. $C_L$ = 15 pF

### Table 5. CLK± Output Phase Jitter

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS)[1,2,3] for $F_{OUT} \geq$ 500 MHz | $\phi_J$ | Kv = 33 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.26 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.26 | — | |
| | | Kv = 45 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.27 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.26 | — | |
| | | Kv = 90 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.32 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.26 | — | |
| | | Kv = 135 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.40 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.27 | — | |
| | | Kv = 180 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.49 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.28 | — | |
| | | Kv = 356 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.87 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.33 | — | |

**Notes:**

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest $K_V$ that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ($K_V$), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with $V_C$=1.65V, $V_{DD}$=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq$ 250 MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

**Table 5. CLK± Output Phase Jitter (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS)[1,2,3,4,5] for $F_{OUT}$ of 125 to 500 MHz | $\phi_J$ | Kv = 33 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.37 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.33 | — | |
| | | Kv = 45 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.37 | 0.4 | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.33 | — | |
| | | Kv = 90 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.43 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.34 | — | |
| | | Kv = 135 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.50 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.34 | — | |
| | | Kv = 180 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.59 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.35 | — | |
| | | Kv = 356 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 1.00 | — | |
| | | 50 kHz to 80 MHz (OC-192) | — | 0.39 | — | |

**Notes:**

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest $K_V$ that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ($K_V$), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with $V_C$=1.65V, $V_{DD}$=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq$ 250 MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

**Table 5. CLK± Output Phase Jitter (Continued)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS)[1,2,5] for $F_{OUT}$ 10 to 160 MHz CMOS Output Only | $\phi_J$ | Kv = 33 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.63 | — | |
| | | 50 kHz to 20 MHz | — | 0.62 | — | |
| | | Kv = 45 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.63 | — | |
| | | 50 kHz to 20 MHz | — | 0.62 | — | |
| | | Kv = 90 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.67 | — | |
| | | 50 kHz to 20 MHz | — | 0.66 | — | |
| | | Kv = 135 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.74 | — | |
| | | 50 kHz to 20 MHz | — | 0.72 | — | |
| | | Kv = 180 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 0.83 | — | |
| | | 50 kHz to 20 MHz | — | 0.8 | — | |
| | | Kv = 356 ppm/V | | | | ps |
| | | 12 kHz to 20 MHz (OC-48) | — | 1.26 | — | |
| | | 50 kHz to 20 MHz | — | 1.2 | — | |

**Notes:**
1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest $K_V$ that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ($K_V$), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with $V_C$=1.65V, $V_{DD}$=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for $F_{OUT} \geq$ 250 MHz, 20 MHz for 50 MHz $\leq F_{OUT}$ <250 MHz, 2 MHz for 10 MHz $\leq F_{OUT}$ <50 MHz.

**Table 6. CLK± Output Period Jitter**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Period Jitter* | $J_{PER}$ | RMS | — | 2 | — | ps |
| | | Peak-to-Peak | — | 14 | — | ps |

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

### Table 7. CLK± Output Phase Noise (Typical)

| Offset Frequency | 74.25 MHz<br>90 ppm/V<br>LVPECL | 491.52 MHz<br>45 ppm/V<br>LVPECL | 622.08 MHz<br>135 ppm/V<br>LVPECL | Units |
|---|---|---|---|---|
| 100 Hz | –87 | –75 | –65 | |
| 1 kHz | –114 | –100 | –90 | |
| 10 kHz | –132 | –116 | –109 | |
| 100 kHz | –142 | –124 | –121 | dBc/Hz |
| 1 MHz | –148 | –135 | –134 | |
| 10 MHz | –150 | –146 | –146 | |
| 100 MHz | n/a | –147 | –147 | |

### Table 8. Environmental Compliance

The Si552 meets the following qualification test requirements.

| Parameter | Conditions/Test Method |
|---|---|
| Mechanical Shock | MIL-STD-883F, Method 2002.3 B |
| Mechanical Vibration | MIL-STD-883F, Method 2007.3 A |
| Solderability | MIL-STD-883F, Method 203.8 |
| Gross & Fine Leak | MIL-STD-883F, Method 1014.7 |
| Resistance to Solvents | MIL-STD-883F, Method 2016 |
| Moisture Sensitivity Level | J-STD-020, MSL 1 |
| Contact Pads | J-STD-020, MSL 1 |

### Table 9. Thermal Characteristics

(Typical values TA = 25 ºC, $V_{DD}$ = 3.3 V)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still Air | — | 84.6 | — | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | Still Air | — | 38.8 | — | °C/W |
| Ambient Temperature | $T_A$ | | –40 | — | 85 | °C |
| Junction Temperature | $T_J$ | | — | — | 125 | °C |

**Table 10. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Maximum Operating Temperature | $T_{AMAX}$ | 85 | ºC |
| Supply Voltage, 1.8 V Option | $V_{DD}$ | –0.5 to +1.9 | V |
| Supply Voltage, 2.5/3.3 V Option | $V_{DD}$ | –0.5 to +3.8 | V |
| Input Voltage (any input pin) | $V_I$ | –0.5 to $V_{DD}$ + 0.3 | V |
| Storage Temperature | $T_S$ | –55 to +125 | ºC |
| ESD Sensitivity (HBM, per JESD22-A114) | ESD | 2500 | V |
| Soldering Temperature (Pb-free profile)[2] | $T_{PEAK}$ | 260 | ºC |
| Soldering Temperature Time @ $T_{PEAK}$ (Pb-free profile)[2] | $t_P$ | 20–40 | seconds |

**Notes:**
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.

## 2. Pin Descriptions

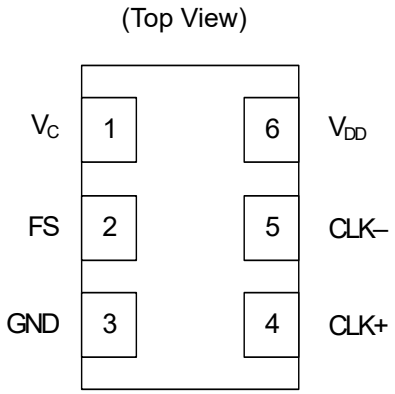



**Table 11. Si552 Pin Descriptions**

| Pin | Name | Type | Function |
|---|---|---|---|
| 1 | $V_C$ | Analog Input | Control Voltage |
| 2 | FS* | Input | Frequency Select:<br>0 = first frequency selected<br>1 = second frequency selected |
| 3 | GND | Ground | Electrical and Case Ground |
| 4 | CLK+ | Output | Oscillator Output |
| 5 | CLK–<br>(N/A for CMOS) | Output | Complementary Output<br>(N/C for CMOS) |
| 6 | $V_{DD}$ | Power | Power Supply Voltage |
| ***Note:** FS includes a 17 kΩ pullup resistor to $V_{DD}$. See Section 3. "Ordering Information" on page 10 for details on frequency select and OE polarity ordering options. | | | |

## 3. Ordering Information

The Si552 supports a variety of options including frequency, temperature stability, tuning slope, output format, and $V_{DD}$. Specific device configurations are programmed into the Si552 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si552 VCXO series is supplied in an industry-standard, RoHS-compliant, lead-free, 6-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

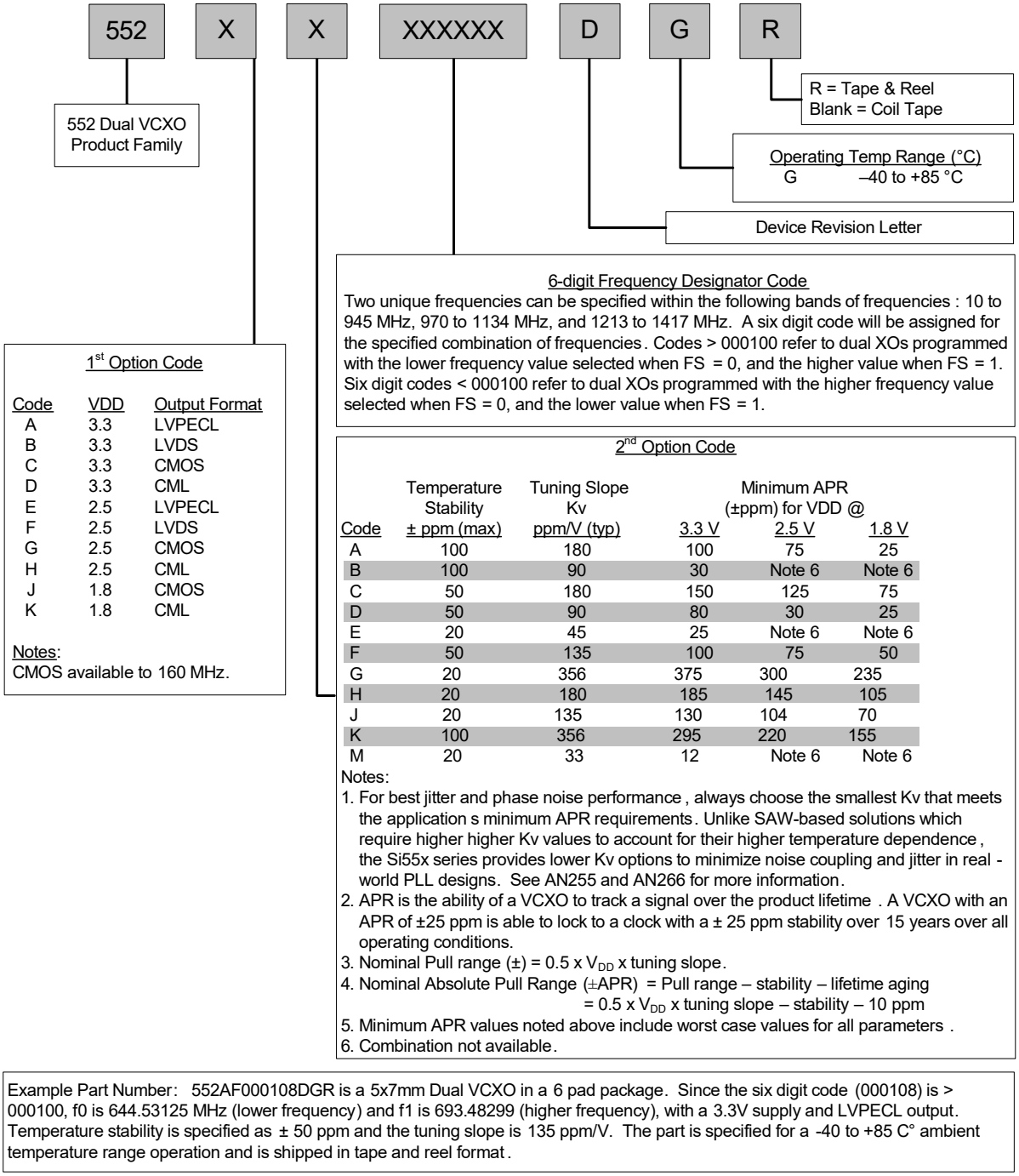



**Figure 1. Part Number Convention**

## 4. Package Outline and Suggested Pad Layout

Figure 2 illustrates the package details for the Si552. Table 12 lists the values for the dimensions shown in the illustration.

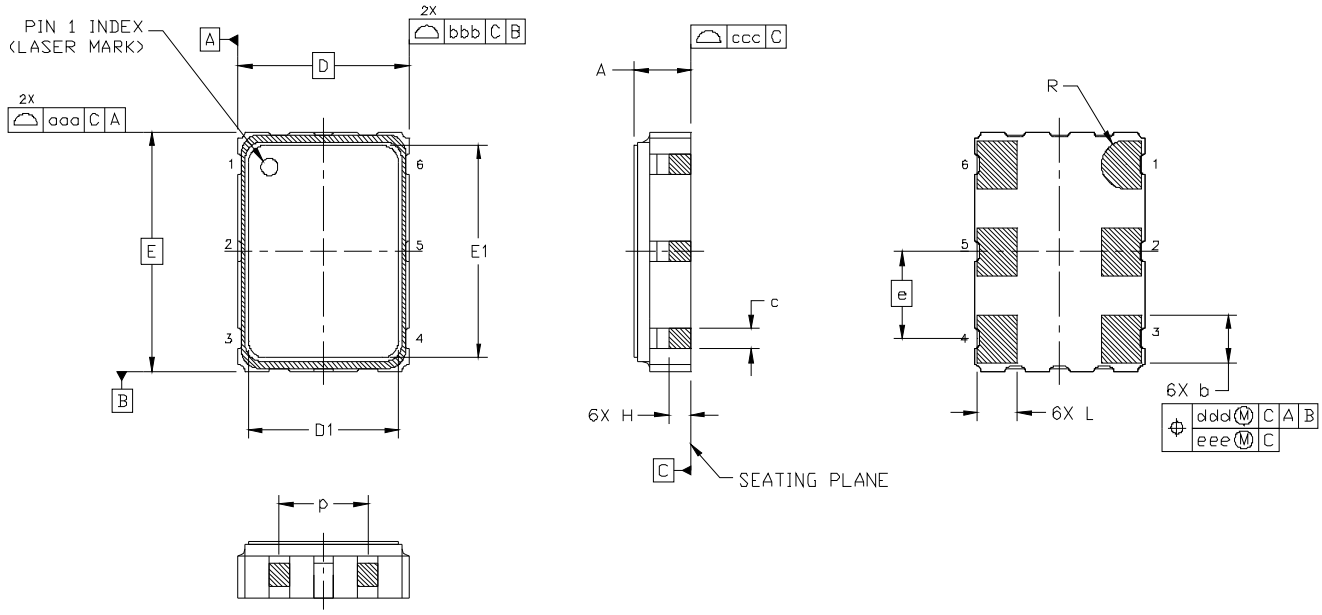



**Figure 2. Si552 Outline Diagram**

**Table 12. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.50 | 1.65 | 1.80 |
| b | 1.30 | 1.40 | 1.50 |
| c | 0.50 | 0.60 | 0.70 |
| D | | 5.00 BSC | |
| D1 | 4.30 | 4.40 | 4.50 |
| e | | 2.54 BSC. | |
| E | | 7.00 BSC. | |
| E1 | 6.10 | 6.20 | 6.30 |
| H | 0.55 | 0.65 | 0.75 |
| L | 1.17 | 1.27 | 1.37 |
| p | 1.80 | — | 2.60 |
| R | | 0.70 REF | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.10 | |
| ddd | | 0.10 | |
| eee | | 0.50 | |

## 5. 6-Pin PCB Land Pattern

Figure 3 illustrates the 6-pin PCB land pattern for the Si552. Table 13 lists the values for the dimensions shown in the illustration.

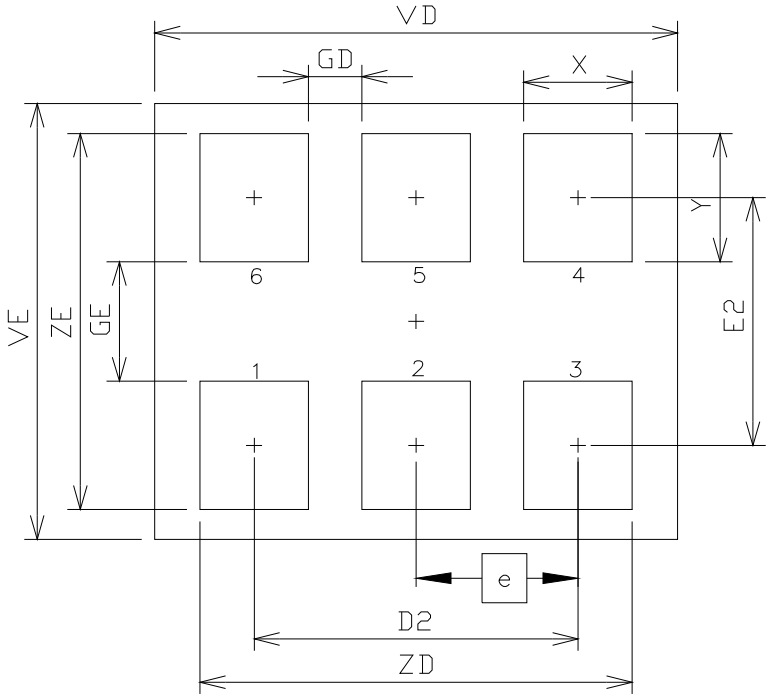



**Figure 3. Si552 PCB Land Pattern**

**Table 13. PCB Land Pattern Dimensions (mm)**

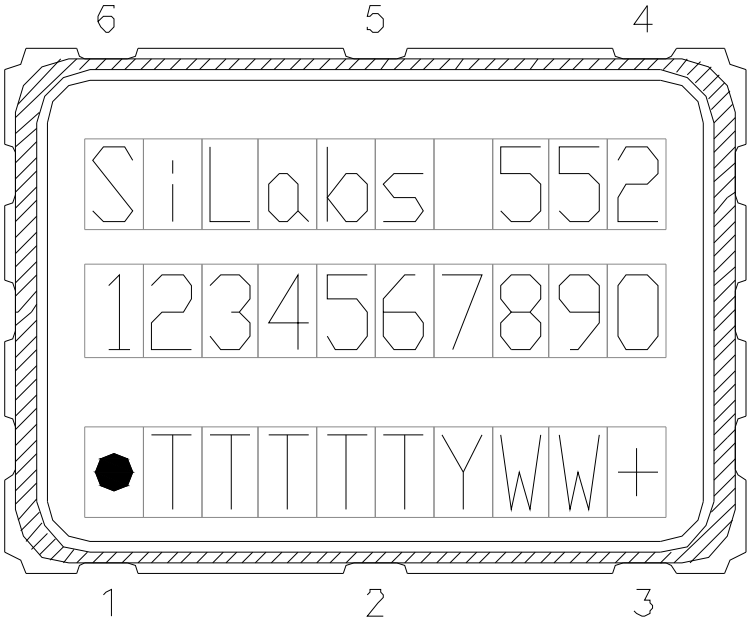
| Dimension | Min | Max |
|---|---|---|
| D2 | 5.08 REF | |
| e | 2.54 BSC | |
| E2 | 4.15 REF | |
| GD | 0.84 | — |
| GE | 2.00 | — |
| VD | 8.20 REF | |
| VE | 7.30 REF | |
| X | 1.70 TYP | |
| Y | 2.15 REF | |
| ZD | — | 6.78 |
| ZE | — | 6.30 |

**Notes:**

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

# 6. Top Marking

## 6.1. Si552 Top Marking




## 6.2. Top Marking Explanation

| Line | Position | Description |
|---|---|---|
| 1 | 1–10 | “SiLabs”+ Part Family Number, 552 (First 3 characters in part number) |
| 2 | 1–10 | Si552: Option1+Option2+Freq(7)+Temp<br>Si552 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp |
| 3 | **Trace Code** | |
| | Position 1 | Pin 1 orientation mark (dot) |
| | Position 2 | Product Revision (D) |
| | Position 3–6 | Tiny Trace Code (4 alphanumeric characters per assembly release instructions) |
| | Position 7 | Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7) |
| | Position 8–9 | Calendar Work Week number (1–53), to be assigned by assembly site |
| | Position 10 | “+” to indicate Pb-Free and RoHS-compliant |

# Document Change List

## Revision 0.6 to Revision 1.0

- Updated Table 4 on page 3.
  - Updated 2.5 V/3.3 V and 1.8 V CML output level specifications.
- Updated Table 5 on page 4.
  - Removed the words “Differential Modes: LVPECL/LVDS/CML” in the footnote referring to AN256.
  - Added footnotes clarifying max offset frequency test conditions.
  - Added CMOS phase jitter specs.
- Updated Table 10 on page 8.
  - Separated 1.8 V, 2.5 V/3.3 V supply voltage specifications.
- Updated and clarified Table 8 on page 7
  - Added “Moisture Sensitivity Level” and “Contact Pads” rows.
- Updated 6. "Top Marking" on page 13 to reflect specific marking information (previously, figure was generic).
- Updated 4. "Package Outline and Suggested Pad Layout" on page 11.
  - Added cyrstal impedance pin in Figure 2 on page 11 and Table 12 on page 11.
- Reordered spec tables and back matter to conform to data sheet quality conventions.

## Revision 1.0 to Revision 1.1

- Added Table 9, “Thermal Characteristics,” on page 7.

## Revision 1.1 to Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in section 3.“Ordering Information”.

## ClockBuilder Pro

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