

MC10EPT20, MC100EPT20

3.3V TTL/CMOS to Differential PECL Translator

The MC10EPT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead SOIC package and the single gate of the EPT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

- 390 ps Typical Propagation Delay
- Maximum Frequency > 1 Ghz Typical
- Differential 3.3 V PECL Outputs
- PNP TTL Inputs for Minimal Loading
- V_{CC} Range of 3.0V to 3.6V
- ESD Protection: >1.5 KV HBM, >200 V MM, >2 KV CDM
- Q Output will default HIGH with inputs open
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",
Oxygen Index 28 to 34
- Transistor Count = 150 devices

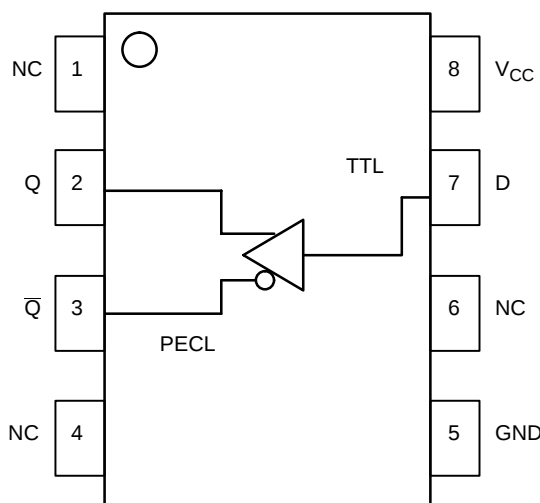


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION

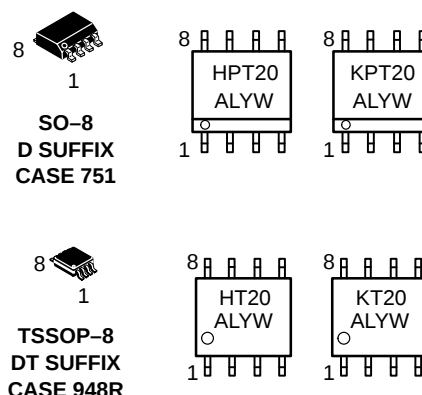
PIN	FUNCTION
Q, $\bar{Q}$	Differential PECL Outputs
D	TTL Input
V _{CC}	Positive Supply
GND	Ground
NC	No Connect



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MARKING DIAGRAMS*



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10EPT20D	SO-8	98 Units/Rail
MC10EPT20DR2	SO-8	2500 Tape & Reel
MC100EPT20D	SO-8	98 Units/Rail
MC100EPT20DR2	SO-8	2500 Tape & Reel
MC10EPT20DT	TSSOP-8	98 Units/Rail
MC10EPT20DTR2	TSSOP-8	2500 Tape & Reel
MC100EPT20DT	TSSOP-8	98 Units/Rail
MC100EPT20DTR2	TSSOP-8	2500 Tape & Reel

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MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Power Supply	GND = 0 V		6	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	6	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVTTTL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V; T_A = –40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I _{IH}	Input HIGH Current (V _{in} = 2.7V)			20	μA
I _{IHH}	Input HIGH Current MAX (V _{in} = 6.0V)			100	μA
I _{IL}	Input LOW Current (V _{in} = 0.5V)			–0.6	mA
V _{IK}	Input Clamp Voltage (I _{in} = –18mA)			–1.2	V
V _{IH}	Input HIGH Voltage	2.0			V
V _{IL}	Input LOW Voltage			0.8	V

10EPT PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3V; GND = 0V (Note 2.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CC}	Power Supply Current HIGH	18	23	28	18	23	28	19	24	29	mA
V _{OH}	Output HIGH Voltage (Note 3.)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V _{OL}	Output LOW Voltage (Note 3.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV

NOTE: 10EPT circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2. Output parameters vary 1:1 with V_{CC}.

3. All loading with 50 ohms to V_{CC}–2.0 volts.

100EPT PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0 V (Note 4.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	20	25	30	22	27	32	23	28	33	mA
V _{OH}	Output HIGH Voltage (Note 5.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 5.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: 100EPT circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

4. Output parameters vary 1:1 with V_{CC}.

5. All loading with 50 ohms to V_{CC}–2.0 volts.

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AC CHARACTERISTICS $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; GND = 0 V (Note 6.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 2. $F_{\max}/\text{JITTER}$)			> 1			> 1			> 1	GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	ps
t_{SKEW}	Device-to-Device Skew (Note 7.)			150			150			170	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{JITTER}$)		1	< 2		1	< 2		1	< 2	ps
t_r , t_f	Output Rise/Fall Times (20% – 80%) Q, $\bar{Q}$	70	100	170	80	120	180	90	140	190	ps

6. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}-2.0\text{ V}$.

7. Skew is measured between outputs under identical transitions.

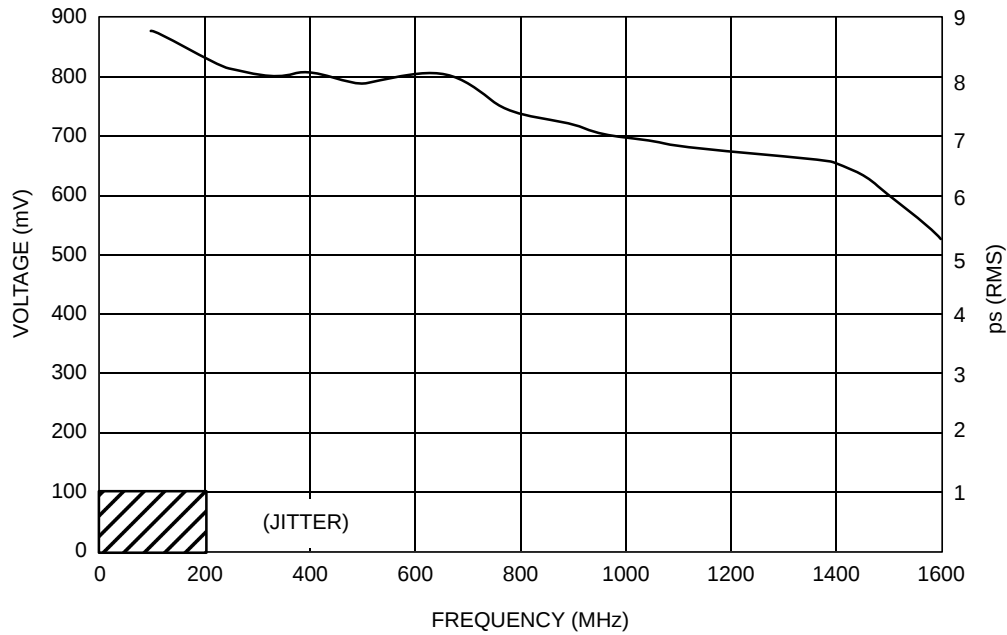


Figure 2. $F_{\max}/\text{Jitter}$

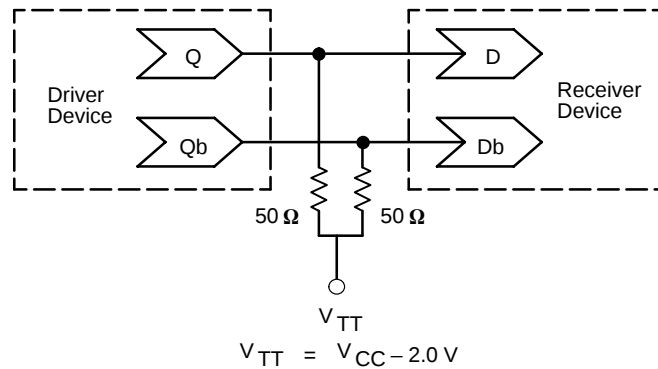


Figure 3. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020 – Termination of ECL Logic Devices.)

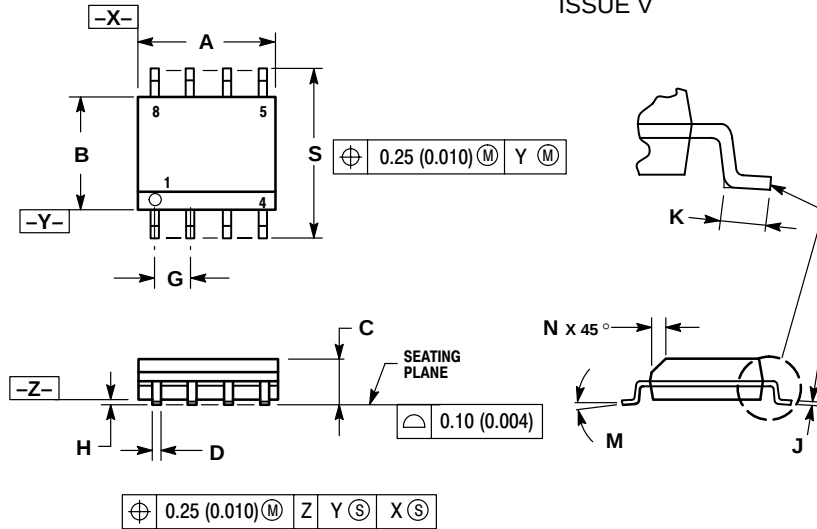
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire–OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE V



NOTES:

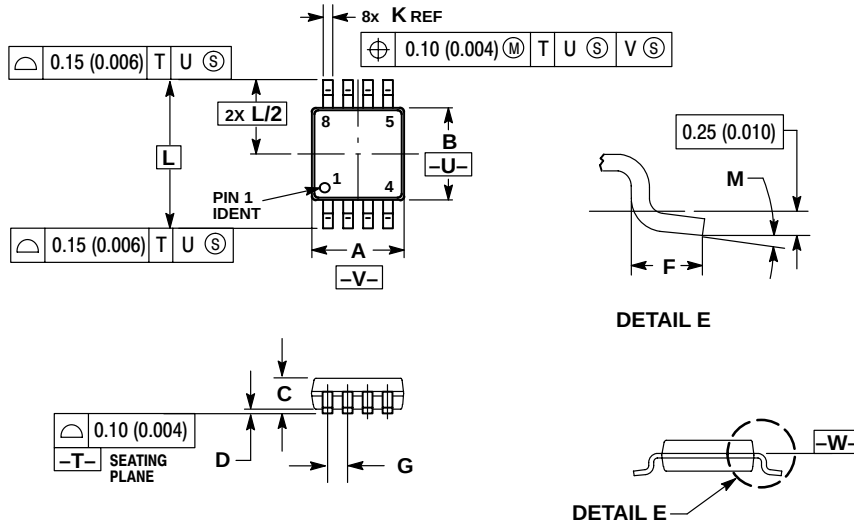
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
CASE 948R-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

Notes

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