TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC554001FI is 4,194,304 bits static random access memory organized as 524,288 words by 8 bits using CMOS technology, and operated a single 3.0~5.5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 10mA/MHz (Typ.)and minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 4μA typically. The TC554001FI has two control inputs. Chip enable inputs ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC554001FI is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required, and wide operating temperature system for TC554001FI guarantees −40~85°C operating temperature.

The TC554001FI is offered in a small - out - line plastic package and thin small - out - line plastic package (forward type).

FEATURES

- Low Power Dissipation
  : 55mW / MHz (Typ.) Operating
- Standby Current : 8μA (Max.) at Ta = 25°C
- Single Power Supply : 3.0~5.5V
- Power Down Features : $\overline{CE}$
- Data retention Supply Voltage : 2.0 ~ 5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Wide Temperature Operation : −40~85°C

- Access Time (Max.)

	5V ± 10%		3.0~5.5V
	−85V	−10V	−85V/−10V
Access Time	85ns	100ns	150ns
$\overline{CE}$ Access Time	85ns	100ns	150ns
$\overline{OE}$ Access Time	45ns	50ns	75ns

- Package:
  SOP32-P-525-1.27 (FI) (Weight: 1.14 g typ)
  TSOP II 32-P-400-1.27 (FTI) (Weight: 0.51 g typ)

PIN CONNECTION (TOP VIEW)

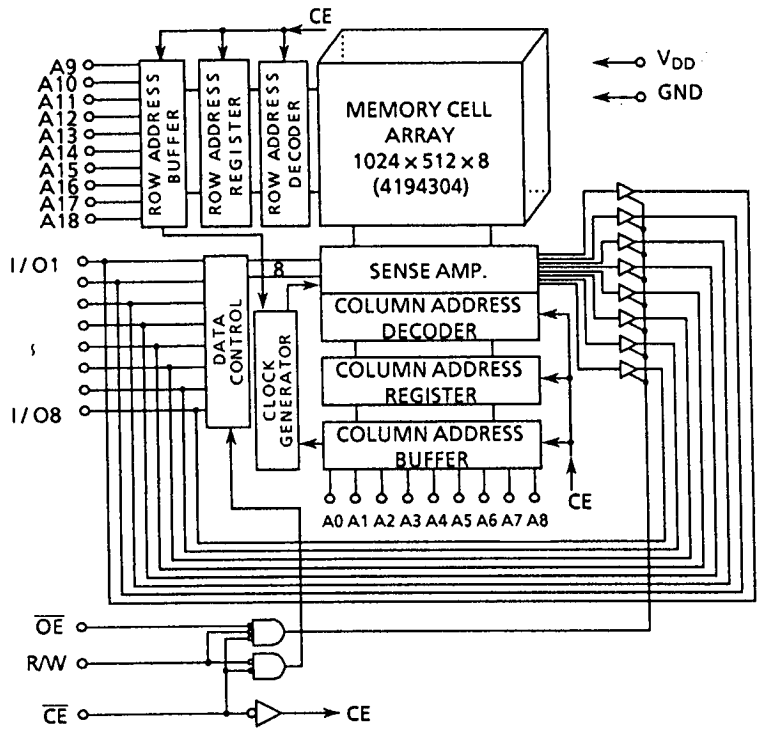
32 PIN FL / FTL

A18	1	32	V_{DD}
A16	2	31	A15
A14	3	30	A17
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

PIN NAMES

A0~A18	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+ 5V)
GND	Ground

BLOCK DIAGRAM



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OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDO}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
Tsolder	Soldering Temperature (10s)	260	°C
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	−40 ~ 85	°C

* : −3.0V at pulse width 50ns Max.

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	5V ± 10%			3.0~5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	3.0	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD} + 0.3	V_{DD} − 0.2	−	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3 *	−	0.6	−0.3 *	−	0.2	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	2.0	−	5.5	V

*: −3.0V at pulse width at 50ns Max.

D.C. and OPERATING CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0V \sim V_{DD}$				–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/\overline{W} = V_{IL}$ $V_{OUT} = 0V \sim V_{DD}$				–	–	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$				–1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$				2.1	–	–	mA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and $R/\overline{W} = V_{IH}$, IOUT = 0mA Other Inputs = V_{IH}/V_{IL}	Tcycle	Min.		–	–	80	mA
				1 μs		–	15	–	
I_{DDO2}		$\overline{CE} = 0.2V$ and $R/\overline{W} = V_{DD}-0.2V$, $I_{OUT} = 0mA$ Other Inputs = $V_{DD}-0.2V/0.2V$	Tcycle	Min.		–	–	70	mA
				1 μs		–	10	–	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$				–	–	3	mA
I_{DDS2}		$\overline{CE} = V_{DD}-0.2V$	$V_{DD} = 2.0 \sim 5.5V$		Ta = 25°C	–	4	8	μA
					Ta = –40~85°C	–	–	140	
			$V_{DD} = 3.0V$		Ta = 25°C	–	2	–	
					Ta = –40~40°C	–	–	6	
					Ta = –40~85°C	–	–	70	

D.C. and OPERATING CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{DD} = 3.3V \pm 0.3V$)

SYMBOL	PARAMETER	TEST CONDITION				MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0V \sim V_{DD}$				–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $R/\overline{W} = V_{IL}$ $V_{OUT} = 0V \sim V_{DD}$				–	–	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD}-0.2V$				–1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.2V$				0.1	–	–	mA
I_{DDO2}	Operating Current	$\overline{CE} = 0.2V$ and $R/\overline{W} = V_{DD}-0.2V$, $I_{OUT} = 0mA$ Other Inputs = $V_{DD}-0.2V/0.2V$	Tcycle	Min.		–	–	35	mA
				1 μs		–	5	–	
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD}-0.2V$	$V_{DD} = 3.3 \pm 0.3V$		Ta = 25°C	–	2	4	μA
					Ta = –40~85°C	–	–	90	
			$V_{DD} = 3.3V$		Ta = 25°C	–	2	–	
					Ta = –40~40°C	–	–	8	
					Ta = –40~85°C	–	–	80	

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note : This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554001FI/FTI				UNIT
		−85V		−10V		
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	−	100	−	ns
t_{ACC}	Address Access Time	−	85	−	100	
t_{CO}	$\overline{CE}$ Access Time	−	85	−	100	
t_{OE}	Output Enable to Output in Valid	−	45	−	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	−	10	−	
t_{OEE}	Output Enable to Output in Low-Z	5	−	5	−	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	−	30	−	35	
t_{ODO}	Output Enable to Output in High-Z	−	30	−	35	
t_{OH}	Output Data Hold Time	10	−	10	−	

WRITE CYCLE

SYMBOL	PARAMETER	TC554001FI/FTI				UNIT
		−85V		−10V		
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	−	100	−	ns
t_{WP}	Write Pulse Width	55	−	60	−	
t_{CW}	Chip Selection to End of Write	70	−	80	−	
t_{AS}	Address Set up Time	0	−	0	−	
t_{WR}	Write Recovery Time	0	−	0	−	
t_{ODW}	R/W to Output in High-Z	−	25	−	25	
t_{OEW}	R/W to Output in Low-Z	5	−	5	−	
t_{DS}	Data Set up Time	35	−	40	−	
t_{DH}	Data Hold Time	0	−	0	−	

A.C. TEST CONDITIONS

- Output Load : 100pF + 1 TTL Gate
- Input Pulse Level : 0.4V, 2.6V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 3.0V ~5.5V)

READ CYCLE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	150	–	ns
t_{ACC}	Address Access Time	–	150	
t_{CO}	$\overline{CE}$ Access Time	–	150	
t_{OE}	Output Enable to Output in Valid	–	75	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	50	
t_{OH}	Output Data Hold Time	10	–	

WRITE CYCLE

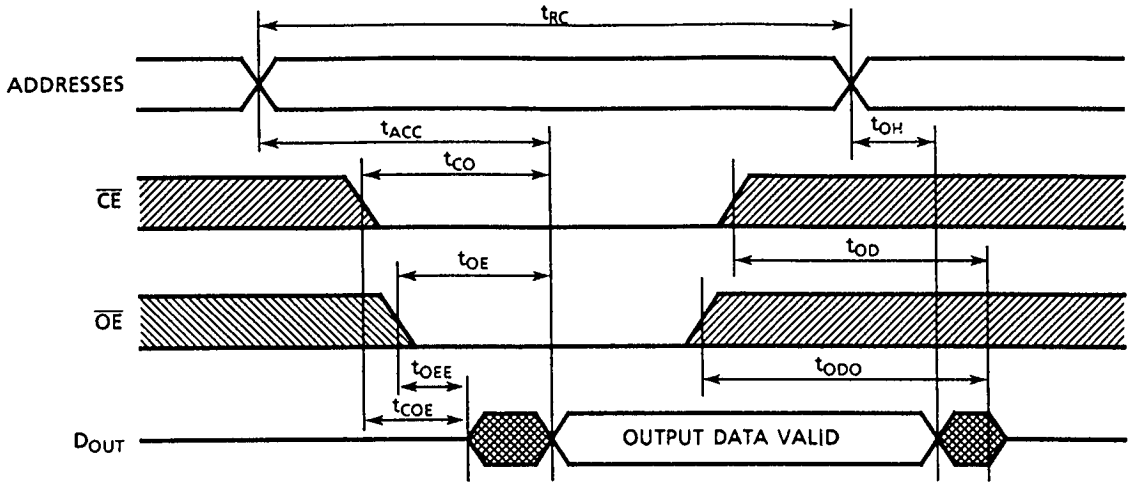
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WC}	Write Cycle Time	150	–	ns
t_{WP}	Write Pulse Width	100	–	
t_{CW}	Chip Enable to End of Write	120	–	
t_{AS}	Address Setup Time	0	–	
t_{WR}	Write Recovery Time	0	–	
t_{ODW}	R/W Low to Output High-Z	–	50	
t_{OEW}	R/W High to Output Active	5	–	
t_{DS}	Data Setup Time	60	–	
t_{DH}	Data Hold Time	0	–	

A.C. TEST CONDITIONS

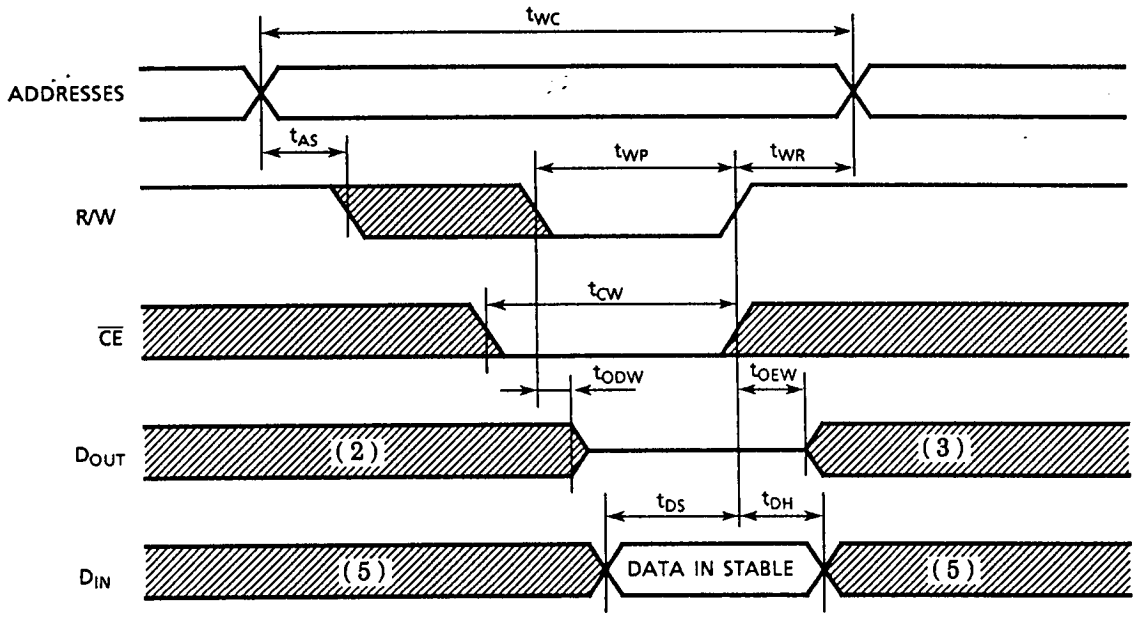
- Output Load : 100pF (Include Jig)
- Input Pulse Level : V_{DD}−0.2V/ 0.2V
- Timing Measurement V_{IN} : 1.5V
  Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

TIMING WAVEFORMS

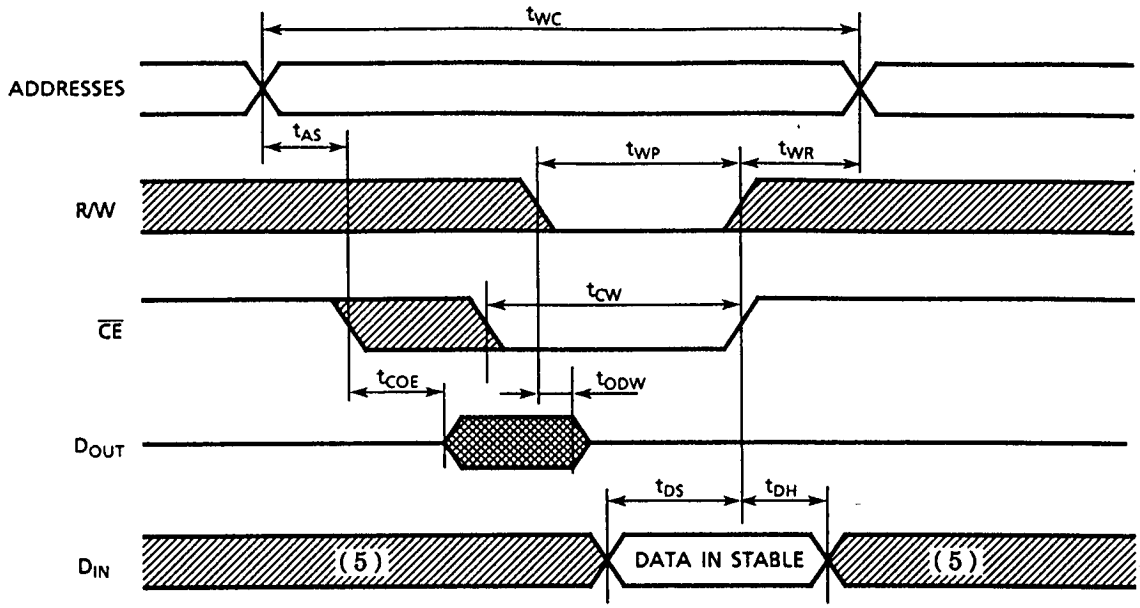
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE}$ Low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

(3) Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

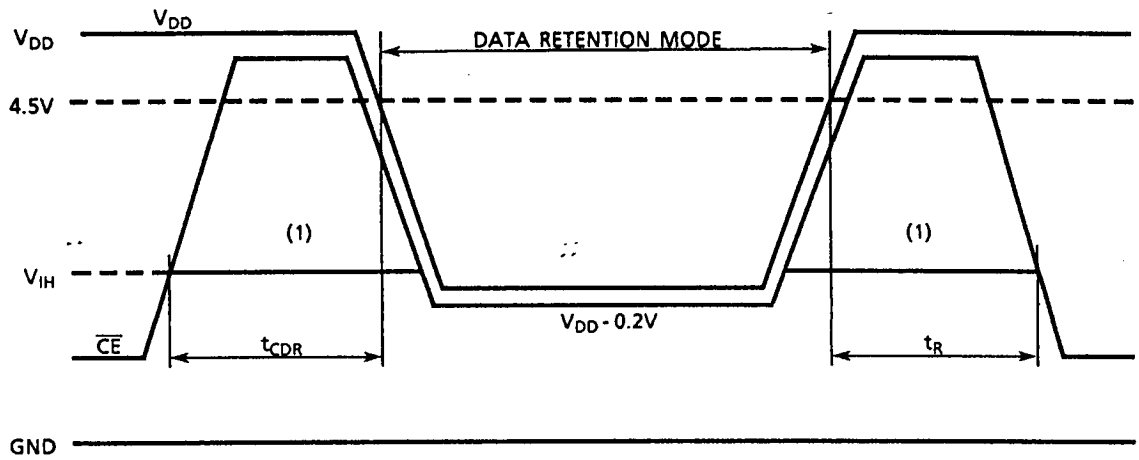
(5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = −40 ~ 85 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.3V	–	–	80 *	μA
		V_{DD} = 5.5V	–	–	140	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	nS
t_R	Recovery Time		5	–	–	mS

*) 8μA (MAX.) Ta = −40 ~ 40 °C

$\overline{CE}$ Controlled Data Retention Mode

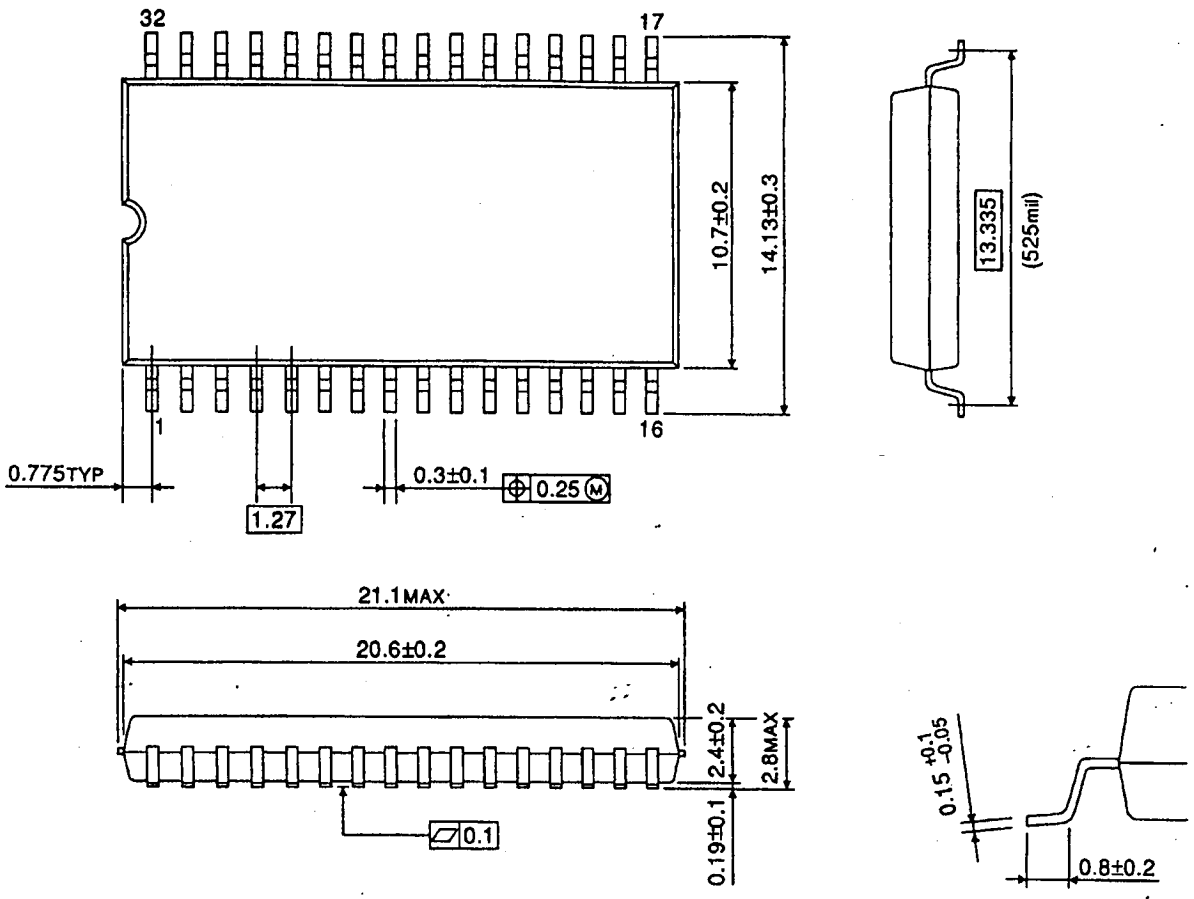


NOTE:

(1) If the V_{IH} of $\overline{CE}$ is 2.4V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.6V, I_{DDS1} current flows.

OUTLINE DRAWING (SOP32-P-525-1.27)

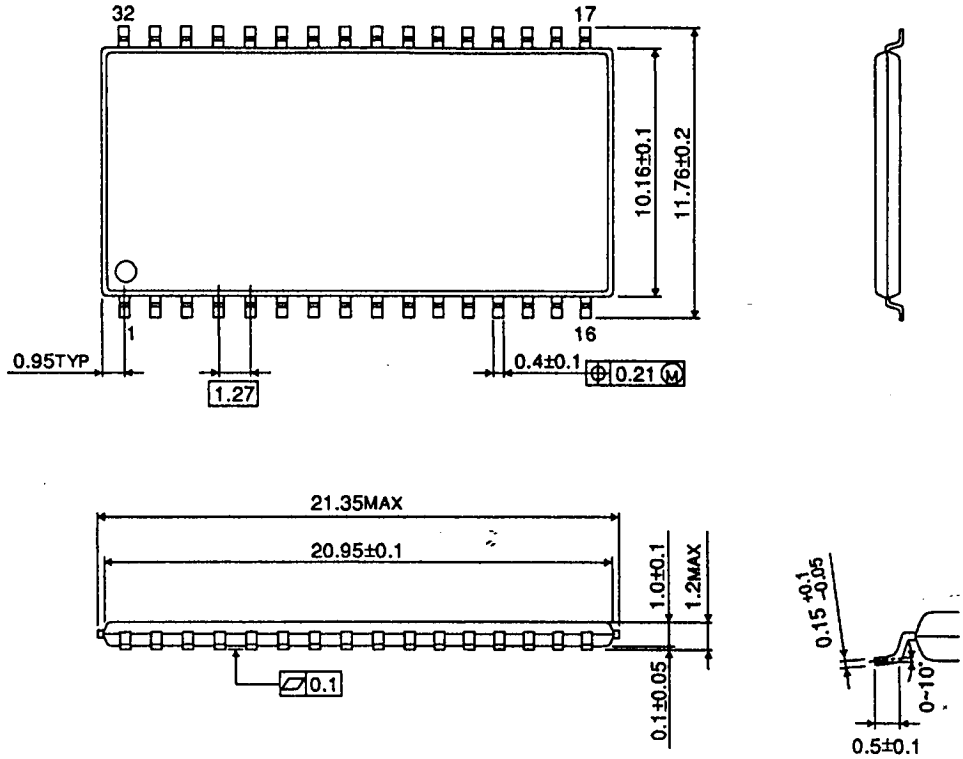
Unit in mm



Weight : 1.14 g (Typ.)

OUTLINE DRAWING (TSOPII 32-P-400-1.27)

Unit in mm



Weight : 0.51g (Typ.)