

TOSHIBA SM12(G,J)48, USM12(G,J)48, SM12(G,J)48A, USM12(G,J)48A

TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM12G48, USM12G48, SM12J48, USM12J48 SM12G48A, USM12G48A, SM12J48A, USM12J48A

AC POWER CONTROL APPLICATIONS

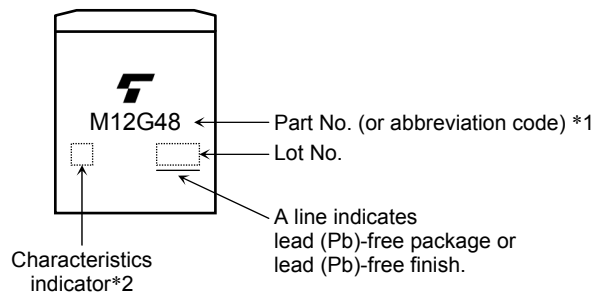
- Repetitive Peak Off-State Voltage : $V_{DRM}=400V, 600V$
- R.M.S. On-State Current : $I_T (RMS) = 12A$
- Gate Trigger Current : $I_{GT}=30mA \text{ Max.}$
: $I_{GT}=20mA \text{ Max. ("A"Type)}$

Unit: mm

SM12G48, SM12J48, SM12G48A, SM12J48A	USM12G48, USM12J48, USM12G48A, USM12J48A
JEDEC —	JEDEC —
JEITA —	JEITA —
TOSHIBA 13-10J1A	TOSHIBA 13-10J2A

Weight: 1.7g

MARKING



	Part No. (or abbreviation code)	Part No.
*1	M12G48	SM12G48, SM12G48A
		USM12G48, USM12G48A
*1	M12J48	SM12J48, SM12J48A
		USM12J48, USM12J48A
*2	Nothing	SM12G48, SM12J48
		USM12G48, USM12J48
	A	SM12G48A, SM12J48A
		USM12G48A, USM12J48A

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage	(U)SM12G48 (U)SM12G48A	400	V
	(U)SM12J48 (U)SM12J48A	600	
R.M.S On-State Current	I_T (RMS)	12	A
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	120 (50Hz)	A
		132 (60Hz)	
I^2t Limit Value	I^2t	72	A^2s
Critical Rate of Rise of On-State Current (Note 1)	di/dt	50	A / μs
Peak Gate Power Dissipation	P_{GM}	5	W
Average Gate Power Dissipation	P_G (AV)	0.5	W
Peak Forward Gate Voltage	V_{GM}	10	V
Peak Forward Gate Current	I_{GM}	2	A
Junction Temperature	T_j	-40~125	$^{\circ}C$
Storage Temperature Range	T_{stg}	-40~125	$^{\circ}C$

Note 1 : $V_{DRM}=0.5 \times \text{Rated}$

$I_{TM} \leq 15A$

$t_{gw} \geq 10\mu s$

$t_{gr} \leq 250ns$

$i_{gp} = I_{GT} \times 2.0$

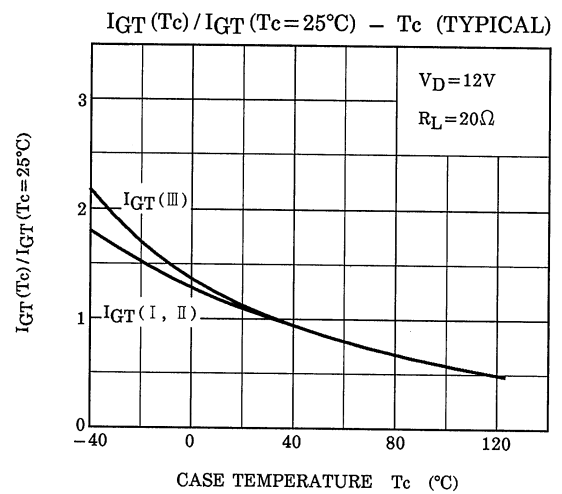
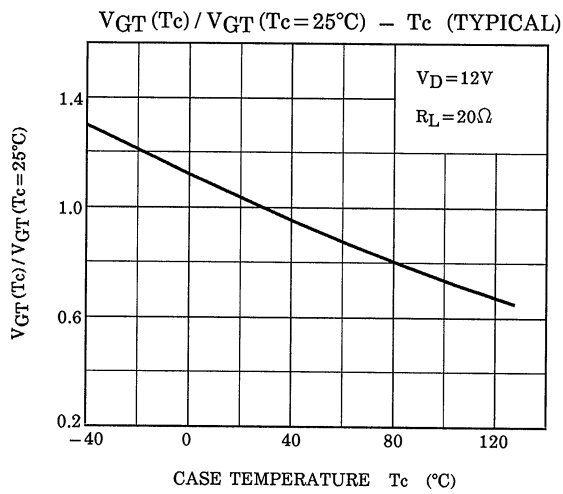
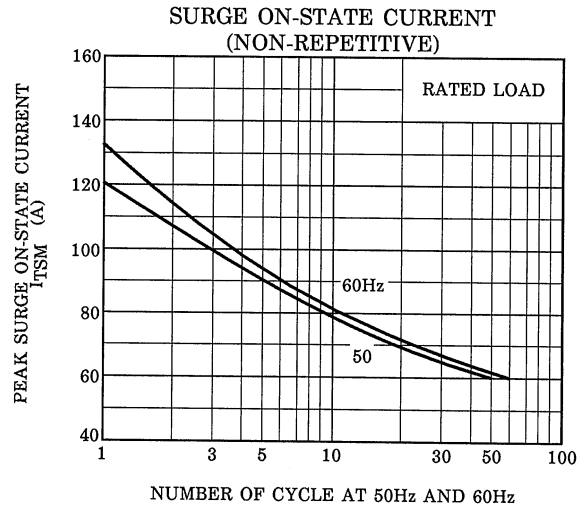
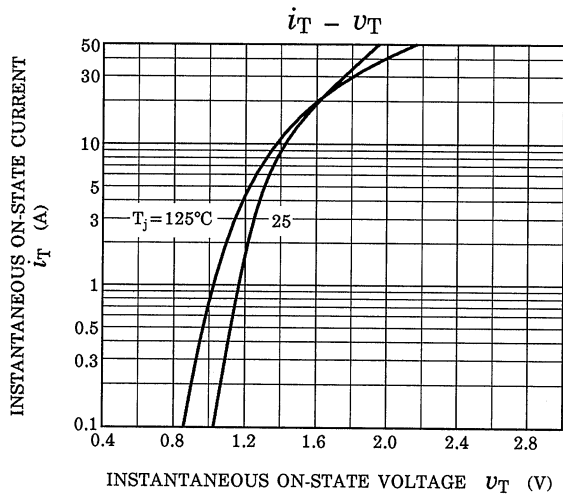
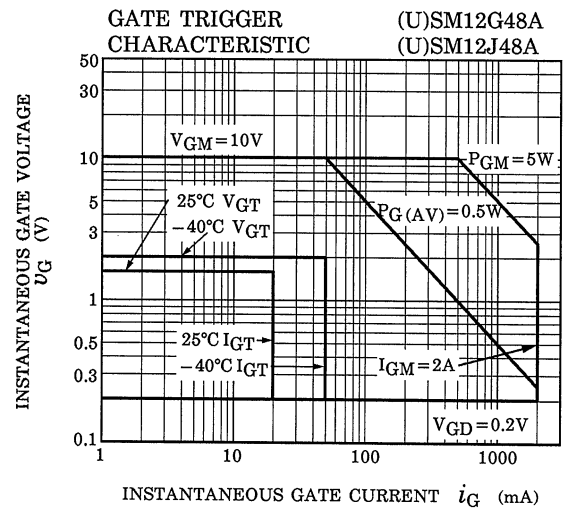
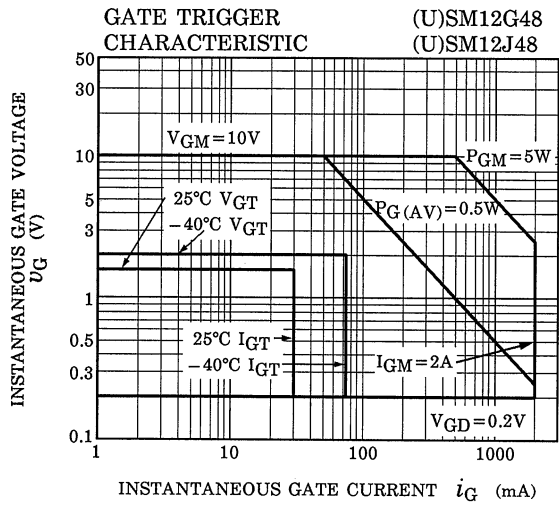
Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

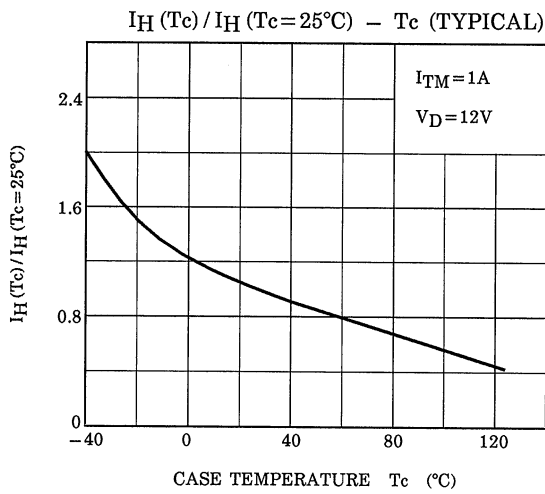
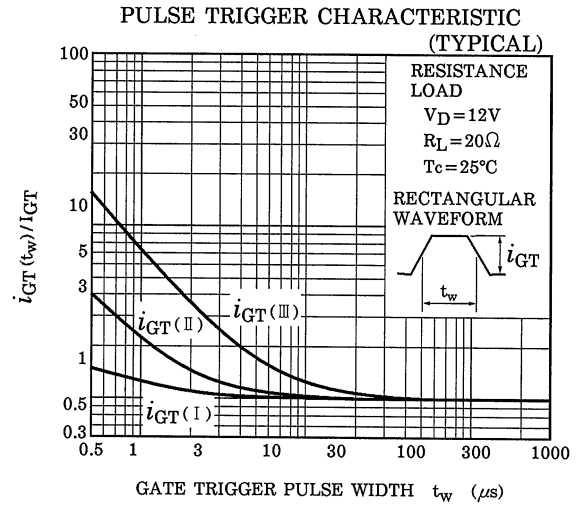
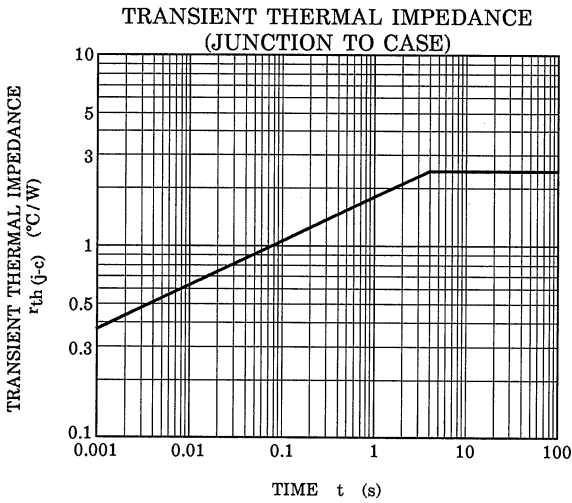
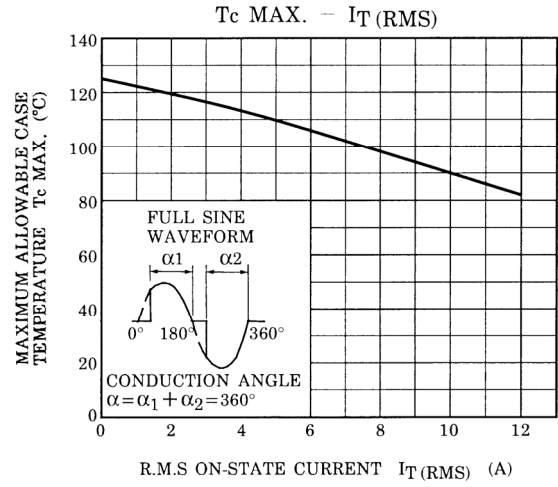
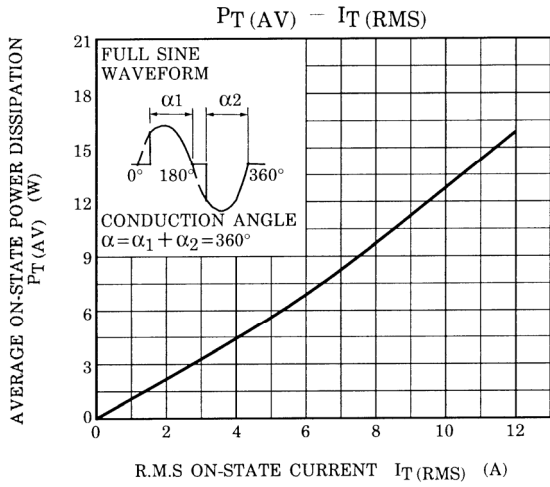
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

TOSHIBA SM12(G,J)48,USM12(G,J)48,SM12(G,J)48A,USM12(G,J)48A

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Repetitive Peak Off-State Current		I_{DRM}	$V_{DRM}=\text{Rated}$	—	—	20	μA		
Gate Trigger Voltage	I	V_{GT}	$V_D=12\text{V}$ $R_L=20\Omega$	T2 (+), Gate (+)	—	—	1.5	V	
	II			T2 (+), Gate (-)	—	—	1.5		
	III			T2 (-), Gate (-)	—	—	1.5		
	IV			T2 (-), Gate (+)	—	—	—		
Gate Trigger Current	SM12G48 SM12J48	I_{GT}	$V_D=12\text{V}$ $R_L=20\Omega$	T2 (+), Gate (+)	—	—	30	mA	
				II	T2 (+), Gate (-)	—	—		30
				III	T2 (-), Gate (-)	—	—		30
				IV	T2 (-), Gate (+)	—	—		—
	SM12G48A SM12J48A			I	T2 (+), Gate (+)	—	—		20
				II	T2 (+), Gate (-)	—	—		20
				III	T2 (-), Gate (-)	—	—		20
				IV	T2 (-), Gate (+)	—	—		—
Peak On-State Voltage		V_{TM}	$I_{TM}=17\text{A}$	—	—	1.5	V		
Gate Non-Trigger Voltage		V_{GD}	$V_D=\text{Rated}$, $T_c=125^\circ\text{C}$	0.2	—	—	V		
Holding Current		I_H	$V_D=12\text{V}$, $I_{TM}=1\text{A}$	—	—	50	mA		
Thermal Resistance		$R_{th(j-c)}$	Junction to Case, AC	—	—	2.4	$^\circ\text{C} / \text{W}$		
Critical Rate of Rise of Off-State Voltage	(U)SM12G48 (U)SM12J48	dv / dt	$V_{DRM}=\text{Rated}$, $T_j=125^\circ\text{C}$ Exponential Rise	—	300	—	V / μs		
	(U)SM12G48A (U)SM12J48A			—	200	—			
Critical Rate of Rise of Off-State Voltage at Commutation	(U)SM12G48 (U)SM12J48	$(dv / dt)_c$	$V_{DRM}=400\text{V}$, $T_j=125^\circ\text{C}$ $(di / dt)_c=-6.5\text{A} / \text{ms}$	10	—	—	V / μs		
	(U)SM12G48A (U)SM12J48A			4	—	—			





RESTRICTIONS ON PRODUCT USE

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