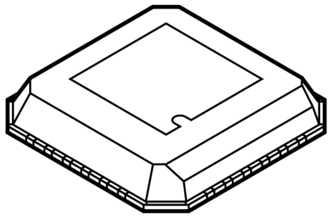
TOSHIBA Bipolar Linear IC   Silicon Monolithic

TA2152FL

Low Current Consumption Headphone Amplifier (for 1.5-V/3-V Use)

The TA2152FL is a headphone amplifier of low current consumption type developed for portable digital audio.

It is especially suitable for portable CD players, portable MD players etc.



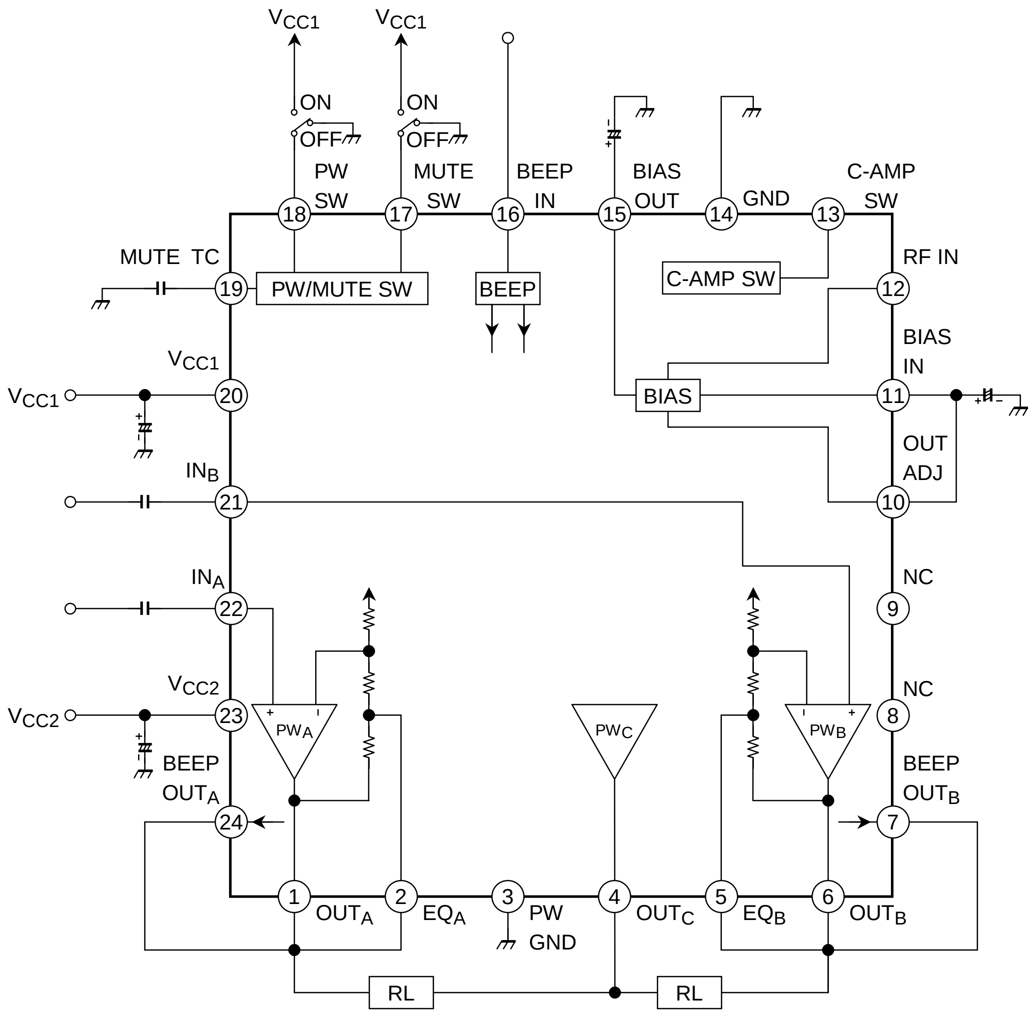
QON24-P-0505-0.50

Weight: 0.05 g (typ.)
Marking: 2152

Features

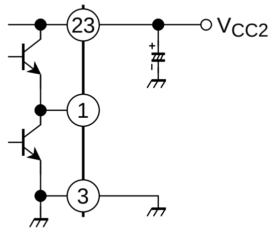
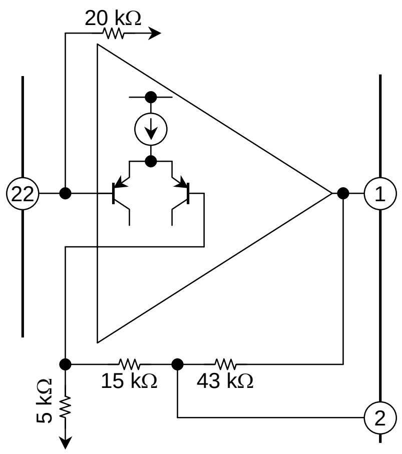
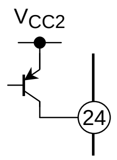
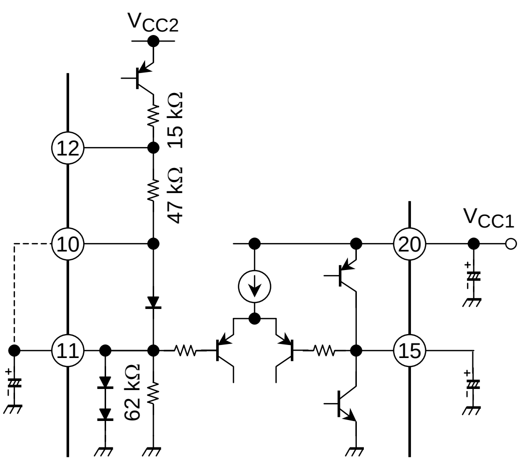
- Low current consumption
  - The power amplifier output stage can be driven using a single battery.
    As a result, overall current consumption is low.
  - Built-in center amplifier switch
    For the output-coupling type, the consumption current has been decreased still further.
  - Current value (V_{CC1} = 2.4 V, V_{CC2} = 1.2 V, f = 1 kHz, R_L = 16 Ω, Ta = 25°C, typ.)
    - Output-coupling type
      - No Signal: I_{CC} (V_{CC1}) = 0.4 mA, I_{CC} (V_{CC2}) = 0.3 mA
      - 0.1 mW × 2 ch: I_{CC} (V_{CC1}) = 0.5 mA, I_{CC} (V_{CC2}) = 2.2 mA
      - 0.5 mW × 2 ch: I_{CC} (V_{CC1}) = 0.5 mA, I_{CC} (V_{CC2}) = 5.0 mA
    - OCL type
      - No Signal: I_{CC} (V_{CC1}) = 0.7 mA, I_{CC} (V_{CC2}) = 0.7 mA
      - 0.1 mW × 2 ch: I_{CC} (V_{CC1}) = 0.7 mA, I_{CC} (V_{CC2}) = 4.5 mA
      - 0.5 mW × 2 ch: I_{CC} (V_{CC1}) = 0.8 mA, I_{CC} (V_{CC2}) = 10.0 mA
- Output power: P_o = 8 mW (typ.)
  (V_{CC1} = 2.4 V, V_{CC2} = 1.2 V, f = 1 kHz, R_L = 16 Ω, THD = 10%, Ta = 25°C)
- Voltage gain: G_V = 11.5dB (typ.)
- Built-in beep function
- Built-in low-pass compensation (output-coupling type)
- Built-in mute switch
- Built-in power switch
- Operating supply voltage range (Ta = 25°C)
  $V_{CC1\ (opr)}$ = 1.8 V~4.5 V
  $V_{CC2\ (opr)}$ = 0.9 V~4.5 V

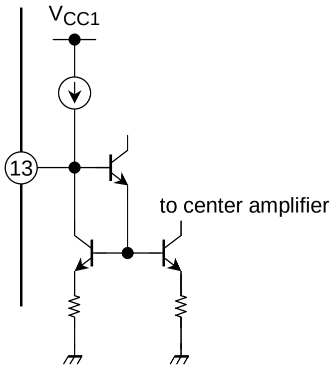
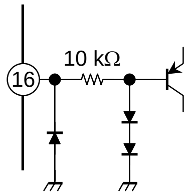
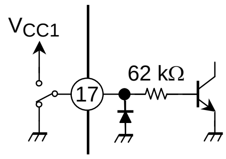
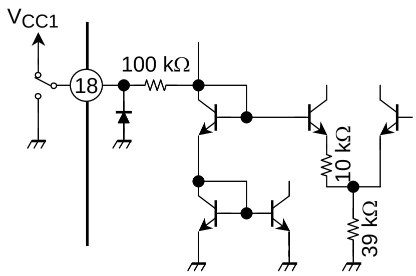
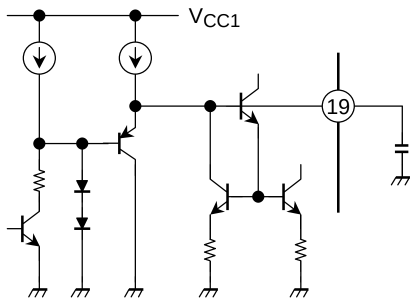
Block Diagram (of OCL Application)



Pin Descriptions

Pin Voltage: Typical pin voltage for test circuit when no input signal is applied (V_{CC1} = 2.4 V, V_{CC2} = 1.2 V, Ta = 25°C)

Pin No.	Pin Name	Function	Internal Circuit	Pin Voltage (V)
1	OUT_A	Outputs from power amplifier		0.6
4	OUT_C			
6	OUT_B			
3	PW GND	GND for power drive stage		0
23	V_{CC2}	V_{CC} for power drive stage		1.2
2	EQ_A	Low-pass compensation pins		0.6
5	EQ_B			
21	IN_B	Inputs to power amplifier		0.6
22	IN_A			
7	BEEP OUT_B	Outputs for beep signal		—
24	BEEP OUT_A			
14	GND	GND for everything other than power drive stage	—	0
8	NC	Not connected	—	—
9	NC			
10	OUT ADJ	DC output voltage adjustment Either connect this pin or leave it open depending on the level of V_{CC2}. If the power supply of a 1.5 V system is applied to V_{CC2}, connect this pin to BIAS IN (pin11) If the power supply of a 3 V system is applied to V_{CC2}, leave this pin open.		0.6
11	BIAS IN	Bias circuit input		0.6
12	RF IN	Ripple filter input		1.1
15	BIAS OUT	Bias circuit output		0.6
20	V_{CC1}	V_{CC} for everything other than power drive stage		2.4

Pin No.	Pin Name	Function	Internal Circuit	Pin Voltage (V)
13	C-AMP SW	Center amplifier switch (C-Cup type: GND (OCL type: Open		―
16	BEEP IN	Beep signal input If the beep function is not used, this pin is connected to GND.		―
17	MUTE SW	Mute switch (Mute OFF: L level (Mute ON: H level Refer to application note (6)		―
18	PW SW	Power switch (IC ON: H level (IC OFF: L level Refer to application note (6)		―
19	MUTE TC	Mute smoothing Reduces pop noises during switching.		―

Application Notes

(1) Beep function

In Power Mute Mode, the beep signal from the microcomputer or other controlling device is input on the BEEP IN pin (pin 16). This signal is output as a current which flows to the load via the BEEP output pin (pin 7/24). The beep level is set to $V_O = -50dBV$ ($R_L = 16\ \Omega$ (typ.)). For the beep signal timing, please refer to Figure 1.

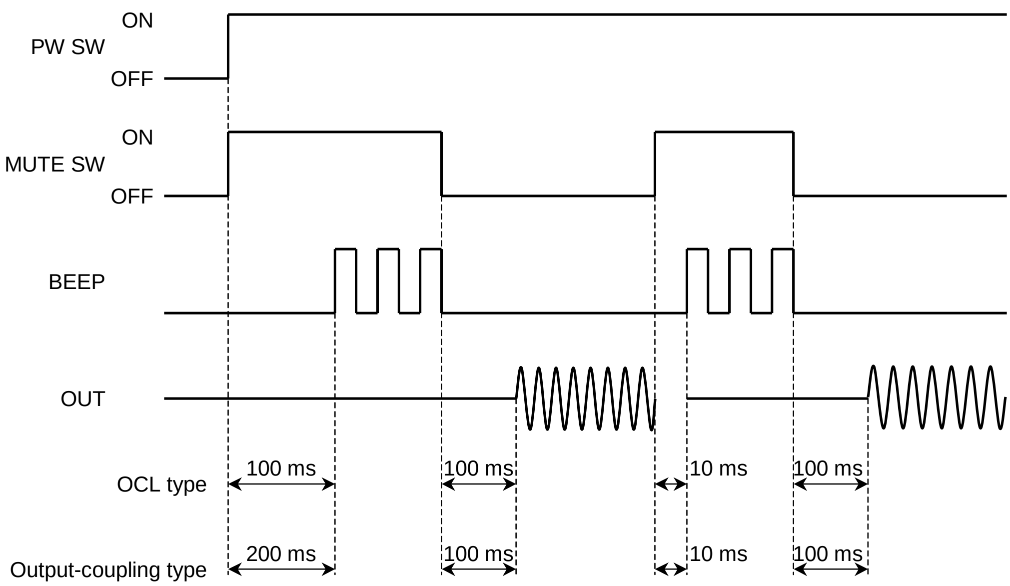


Figure 1 Timing chart for beep and output signals

(2) Low-cut compensation

For output-coupling type, the low-frequency range can be decreased using an output-coupling capacitor and a load (f_c = 45 Hz at C = 220 μF, R = 16 Ω). However, since the capacitor is connected between the IC's output pin (pin 1/6) and EQ pin (pin 2/5), the low-frequency gain of the power amplifier increases, enabling low-cut compensation to be performed. For the response of capacitors of different values, please refer to Figure 2.

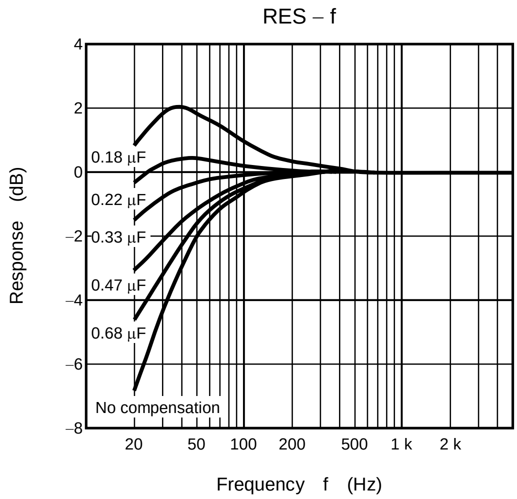


Figure 2 Capacitor response

(3) Adjustment of DC output voltage

Please perform the OUT ADJ pin (pin 10) as follows by the power supply of V_{CC1} and V_{CC2}.

- If a boost voltage is applied to V_{CC1}, V_{CC2} is connected to a battery and the difference between V_{CC1} and V_{CC2} is greater than or equal to 0.7 V, short pins 10 and 11 together. In this case the DC output voltage will be $\frac{V_{CC2}}{2}$.
- If the difference between V_{CC1} and V_{CC2} is less than 0.7 V, or if V_{CC1} and V_{CC2} are connected to the same power supply, leave pin 10 open.

  In these cases the DC output voltage will be $\frac{V_{CC2} - 0.7\ V}{2}$.

However, when the voltage level of V_{CC2} is high, the DC output voltage is will be set to approximately 1.4 V.

(4) RF IN pin

The ripple rejection ratio can by improved by connecting a capacitor to this pin. Connection of a capacitor is recommended, particularly for output-coupling type.

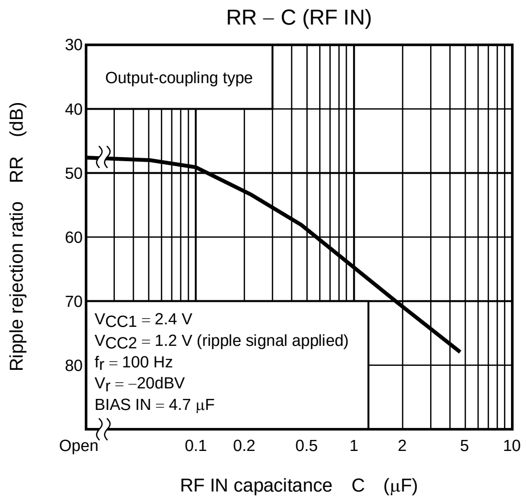


Figure 3 Improvement of ripple rejection ratio

(5) Output application of power amplifier

For output-coupling type the center amplifier is not used with the result that current consumption is low. Please set the C-AMP SW pin (pin 13) accordingly.

- Output-coupling type: Pin 13 is connected to GND.
- OCL type: Pin 13 is open.

(6) Switching pins

(a) PW SW

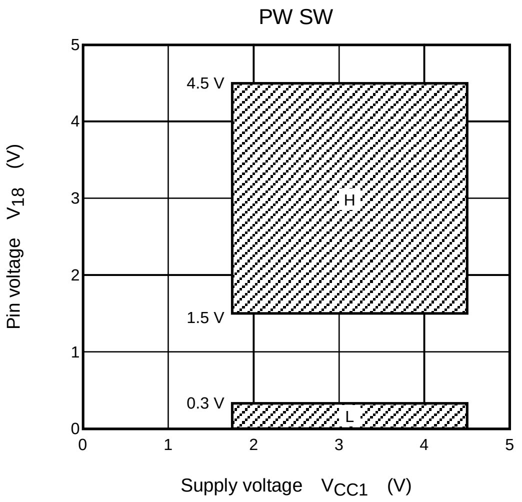
The device is ON when this pin is set to High. To prevent the IC being turned ON by external noise, it is necessary to connect an external pull-down resistor to the PW SW pin. The pin is highly sensitive.

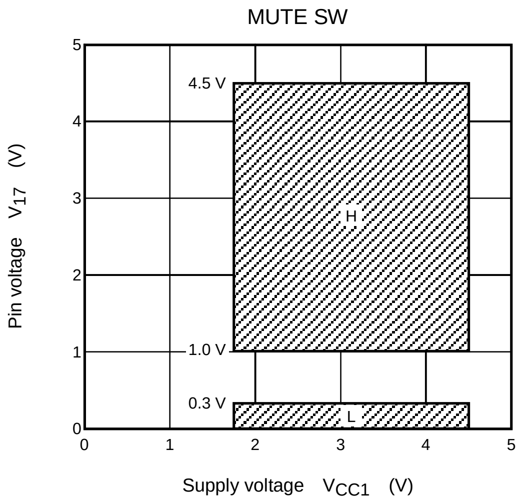
(b) MUTE SW

If the MUTE SW pin is fixed to High, current will flow through the pin, even when the PW SW pin is in OFF Mode. To prevent the IC being turned ON by external noise, it is necessary to connect an external pull-down resistor.

The pop noise heard when the MUTE SW switch is turned ON or OFF can be reduced by connecting an external capacitor to the MUTE TC pin.

(c) Switch sensitivity (Ta = 25°C)





	PW SW
H level	IC ON
L level	IC OFF

	MUTE SW
H level	Mute ON
L level	Mute OFF

Figure 4 Switch sensitivity

(7) Miscellaneous

The following capacitors must have excellent temperature and frequency characteristics.

- Capacitor between V_{CC1} (pin 20) and GND (pin 14)
- Capacitor between V_{CC2} (pin 23) and PW GND (pin 3)
- Capacitor between BIAS IN (pin 11) and GND (pin 14)
- Capacitor between BIAS OUT (pin 15) and GND (pin 14)
- Capacitor between RF IN (pin 12) and GND (pin 14)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage 1	V_{CC1}	4.5	V
Supply voltage 2	V_{CC2}	4.5	
Output current	$I_{o\ (peak)}$	100	mA
Power dissipation	P_D (Note)	350	mW
Operating temperature	T_{opr}	−25~75	°C
Storage temperature	T_{stg}	−55~150	°C

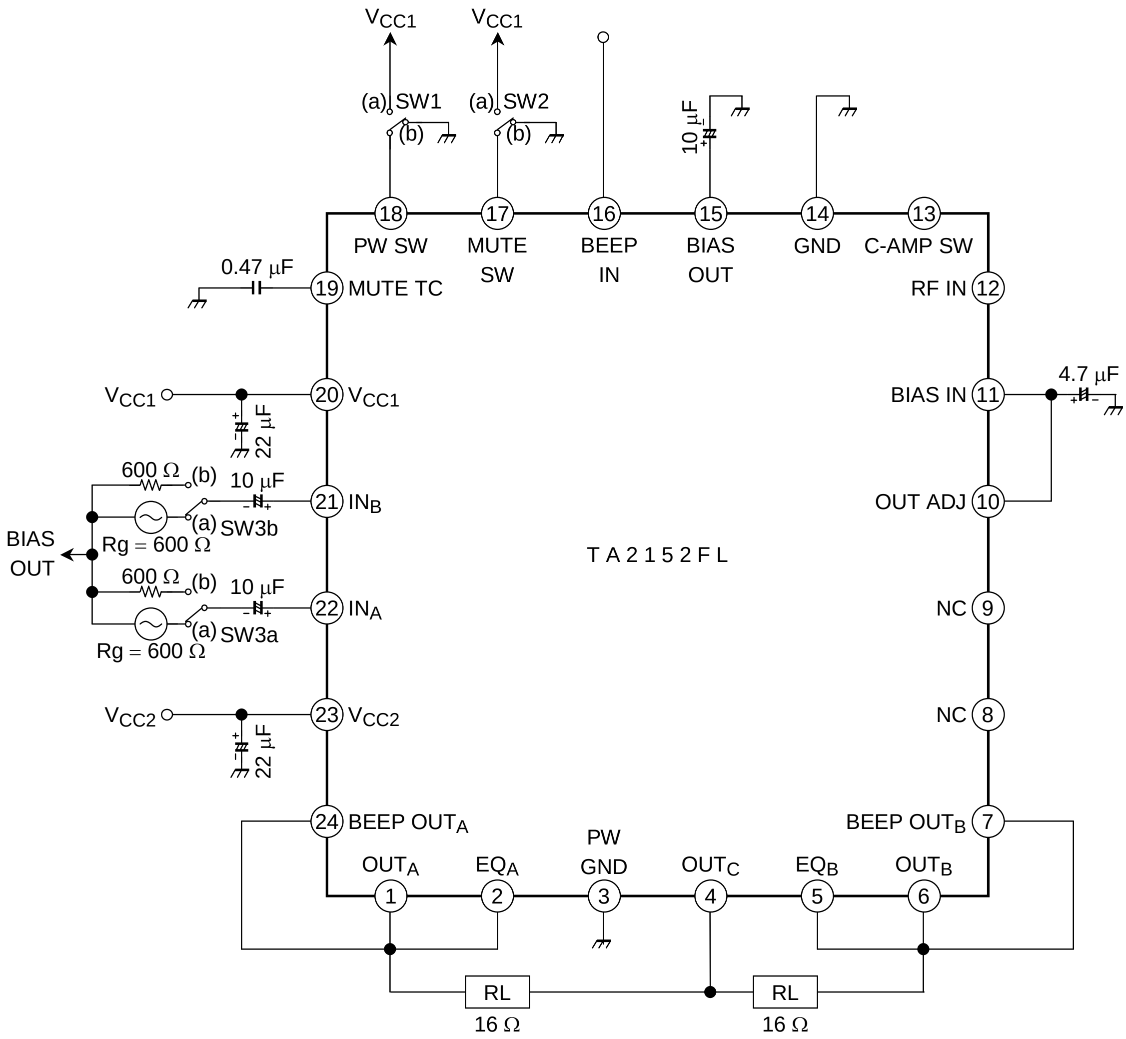
Note: Derated by 2.8 mW/°C above Ta = 25°C

Electrical Characteristics

(Unless otherwise specified V_{CC1} = 2.4 V, V_{CC2} = 1.2 V, Rg = 600 Ω, R_L = 16 Ω, f = 1 kHz, Ta = 25°C, SW1: a, SW2: b, SW3: a)

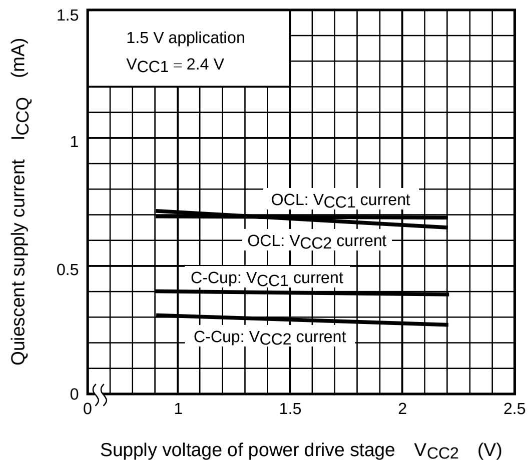
Characteristic	Symbol	Test conditions	Min	Typ.	Max	Unit
Quiescent supply current	I_{CCQ1}	IC OFF (V_{CC1}), SW1: b	—	0.1	5	μA
	I_{CCQ2}	IC OFF (V_{CC2}), SW1: b	—	0.1	5	
	I_{CCQ3}	OCL, Mute ON (V_{CC1}), SW2: a	—	400	600	
	I_{CCQ4}	OCL, Mute ON (V_{CC2}), SW2: a	—	650	1400	
	I_{CCQ5}	C-Cup, Mute ON (V_{CC1}), SW2: a	—	170	250	
	I_{CCQ6}	C-Cup, Mute ON (V_{CC2}), SW2: a	—	85	170	
	I_{CCQ7}	OCL, no signal (V_{CC1})	—	0.7	1.1	mA
	I_{CCQ8}	OCL, no signal (V_{CC2})	—	0.7	1.5	
	I_{CCQ9}	C-Cup, no signal (V_{CC1})	—	0.4	0.6	
	I_{CCQ10}	C-Cup, no signal (V_{CC2})	—	0.3	0.6	
Power supply current during drive	I_{CC1}	OCL, 0.5 mW × 2 ch (V_{CC1})	—	0.8	—	mA
	I_{CC2}	OCL, 0.5 mW × 2 ch (V_{CC2})	—	10.0	—	
	I_{CC3}	C-Cup, 0.5 mW × 2 ch (V_{CC1})	—	0.5	—	
	I_{CC4}	C-Cup, 0.5 mW × 2 ch (V_{CC2})	—	5.0	—	
Voltage gain	G_V	V_o = −22 dBV	9.5	11.5	13.5	dB
Channel balance	CB	V_o = −22 dBV	−1.5	0	+1.5	
Output power	P_o	THD = 10%	5	8	—	mW
Total harmonic distortion	THD	P_o = 1 mW	—	0.1	1.0	%
Output noise voltage	V_{no}	Rg = 600 Ω, Filter: IHF-A, SW3: b	—	−100	−96	dBV
Cross talk	CT	V_o = −22 dBV	−25	−35	—	dB
Ripple rejection ratio 1	RR1	Inflow to V_{CC1}, SW3: b f_r = 100 Hz, V_r = −20 dBV	−65	−85	—	
Ripple rejection ratio 2	RR2	Inflow to V_{CC2}, SW3: b f_r = 100 Hz, V_r = −20 dBV	−85	−100	—	
Muting attenuation	ATT	V_o = −12 dBV	−100	−115	—	
Beep sound output voltage	$V_{BEEP\ (OUT)}$	$V_{BEEP\ (IN)}$ = 2 V_{p-p}	−55	−50	−45	dBV
PW SW ON current	I18	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	5	—	—	μA
PW SW OFF voltage	V18	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	0	—	0.3	V
Mute SW ON current	I17	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	5	—	—	μA
Mute SW OFF voltage	V17	V_{CC1} = 1.8 V, V_{CC2} = 0.9 V	0	—	0.3	V

Test Circuit

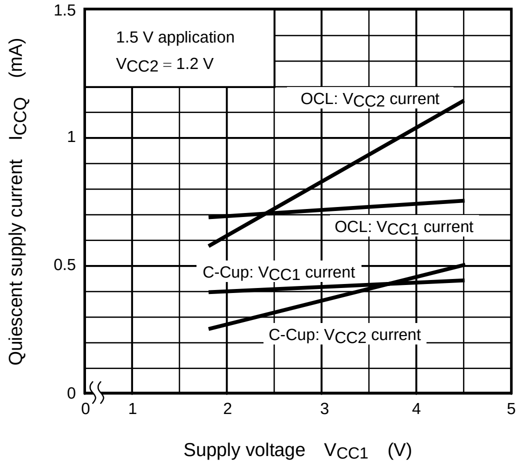


Characteristic Curves (unless otherwise specified, $V_{CC1} = 2.4$ V, $V_{CC2} = 1.2$ V, $R_g = 600\ \Omega$, $R_L = 16\ \Omega$, f = 1 kHz, Ta = 25°C)

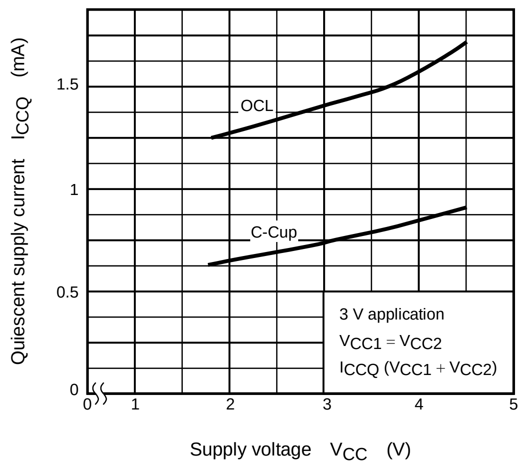
$I_{CCQ} – V_{CC2}$



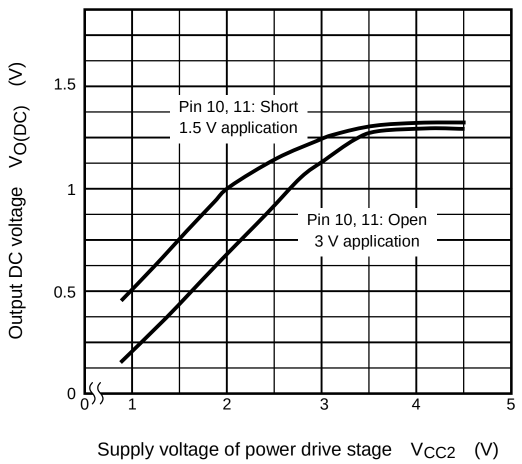
$I_{CCQ} – V_{CC1}$



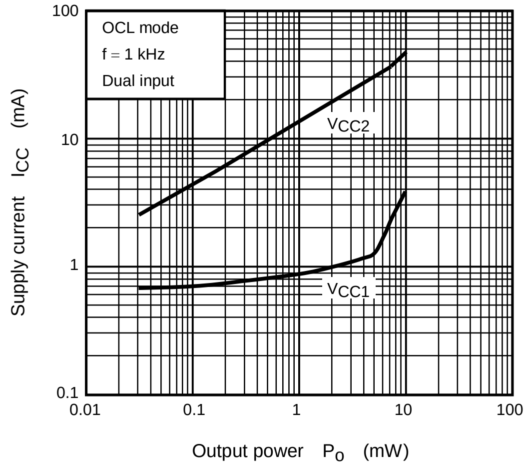
$I_{CCQ} – V_{CC}$



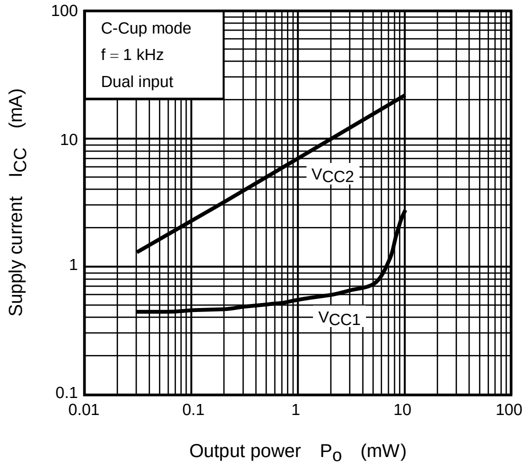
$V_{O\ (DC)} – V_{CC2}$

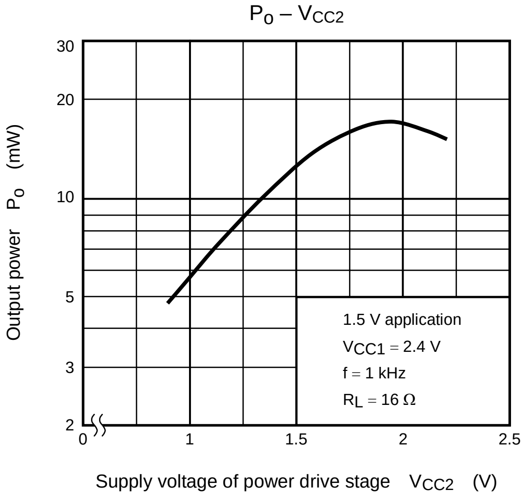


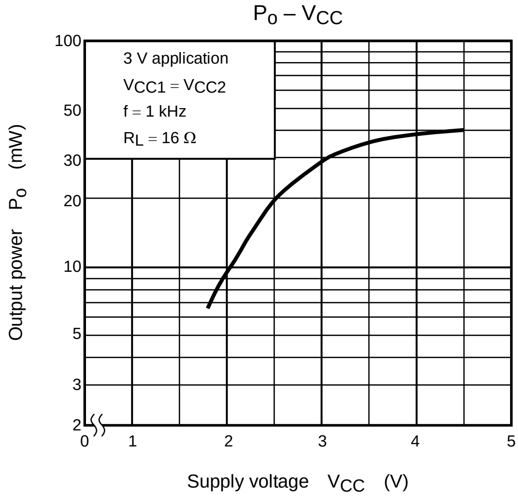
$I_{CC} – P_o$

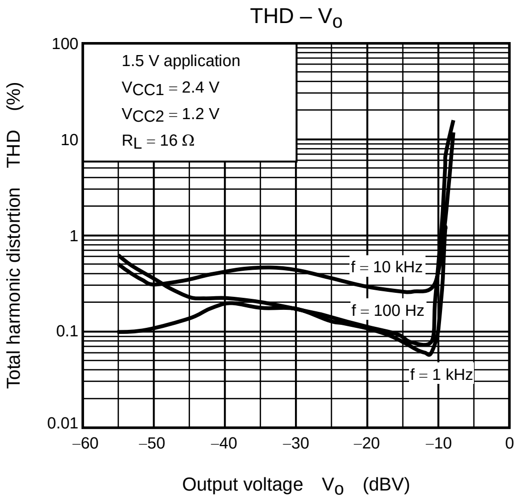


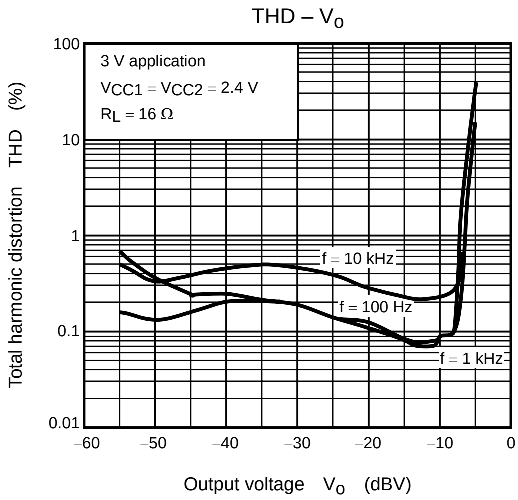
$I_{CC} – P_o$

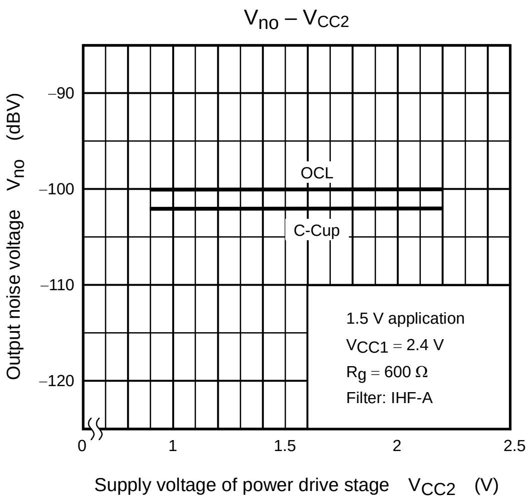


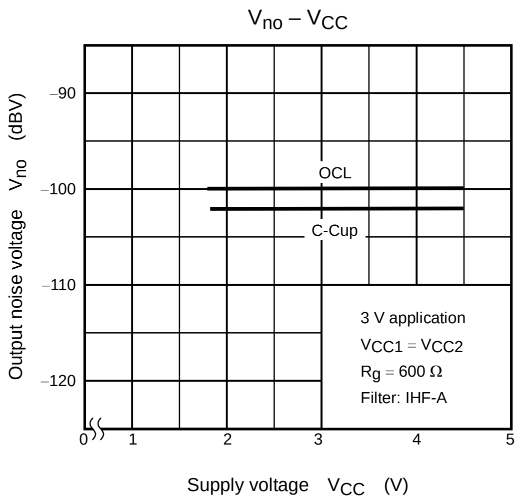

Po – VCC2
Output power Po (mW)
30
20
10
5
3
2
0
1
1.5
2
2.5
1.5 V application
VCC1 = 2.4 V
f = 1 kHz
RL = 16 Ω
Supply voltage of power drive stage VCC2 (V)

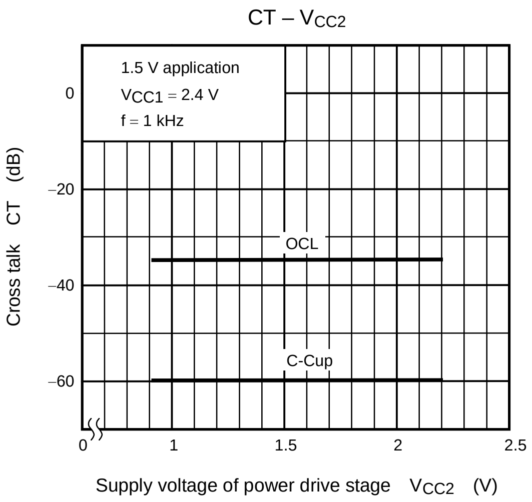

Po – VCC
Output power Po (mW)
100
50
30
20
10
5
3
2
0
1
2
3
4
5
3 V application
VCC1 = VCC2
f = 1 kHz
RL = 16 Ω
Supply voltage VCC (V)

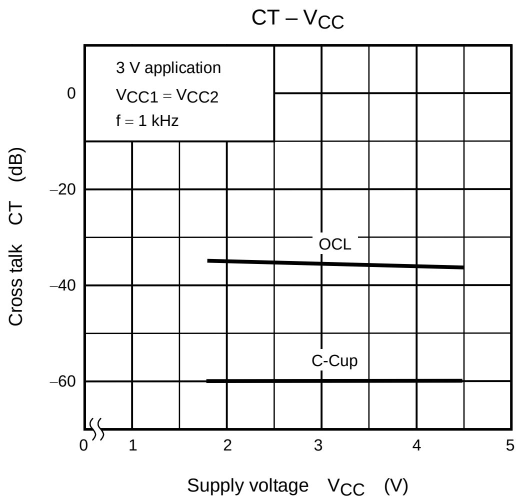

THD – Vo
Total harmonic distortion THD (%)
100
10
1
0.1
0.01
1.5 V application
VCC1 = 2.4 V
VCC2 = 1.2 V
RL = 16 Ω
f = 10 kHz
f = 100 Hz
f = 1 kHz
−60
−50
−40
−30
−20
−10
0
Output voltage Vo (dBV)

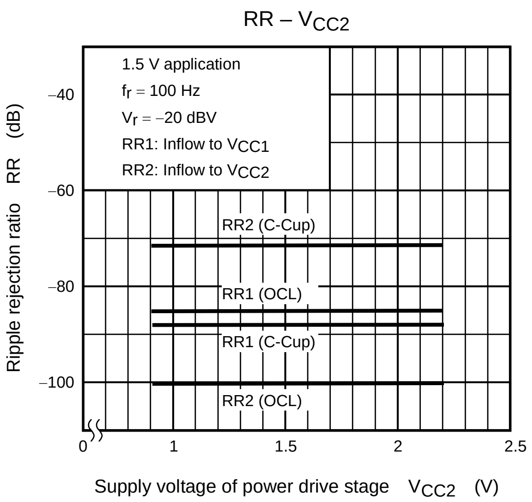

THD – Vo
Total harmonic distortion THD (%)
100
10
1
0.1
0.01
3 V application
VCC1 = VCC2 = 2.4 V
RL = 16 Ω
f = 10 kHz
f = 100 Hz
f = 1 kHz
−60
−50
−40
−30
−20
−10
0
Output voltage Vo (dBV)

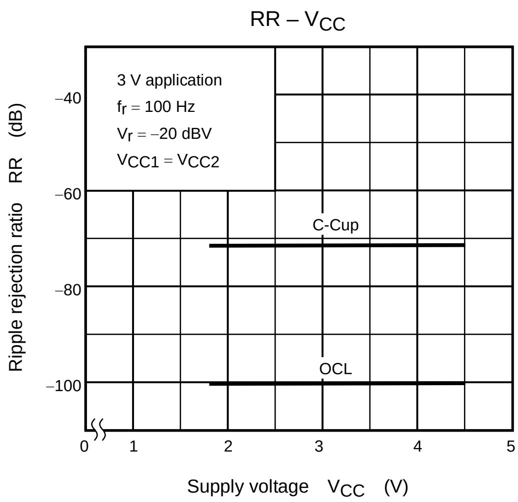

Vno – VCC2
Output noise voltage Vno (dBV)
−90
−100
−110
−120
OCL
C-Cup
1.5 V application
VCC1 = 2.4 V
Rg = 600 Ω
Filter: IHF-A
0
1
1.5
2
2.5
Supply voltage of power drive stage VCC2 (V)

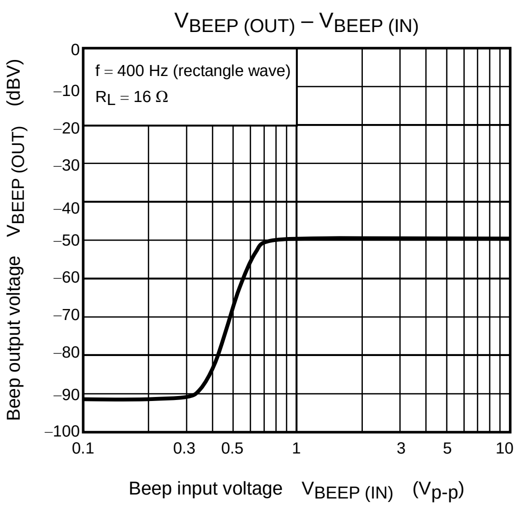

Vno – VCC
Output noise voltage Vno (dBV)
−90
−100
−110
−120
OCL
C-Cup
3 V application
VCC1 = VCC2
Rg = 600 Ω
Filter: IHF-A
0
1
2
3
4
5
Supply voltage VCC (V)


CT – VCC2
1.5 V application
VCC1 = 2.4 V
f = 1 kHz
OCL
C-Cup
Cross talk CT (dB)
Supply voltage of power drive stage VCC2 (V)

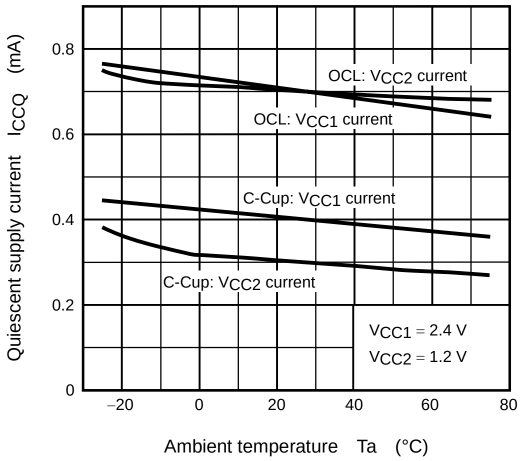

CT – VCC
3 V application
VCC1 = VCC2
f = 1 kHz
OCL
C-Cup
Cross talk CT (dB)
Supply voltage VCC (V)


RR – VCC2
1.5 V application
fr = 100 Hz
Vr = −20 dBV
RR1: Inflow to VCC1
RR2: Inflow to VCC2
RR2 (C-Cup)
RR1 (OCL)
RR1 (C-Cup)
RR2 (OCL)
Ripple rejection ratio RR (dB)
Supply voltage of power drive stage VCC2 (V)

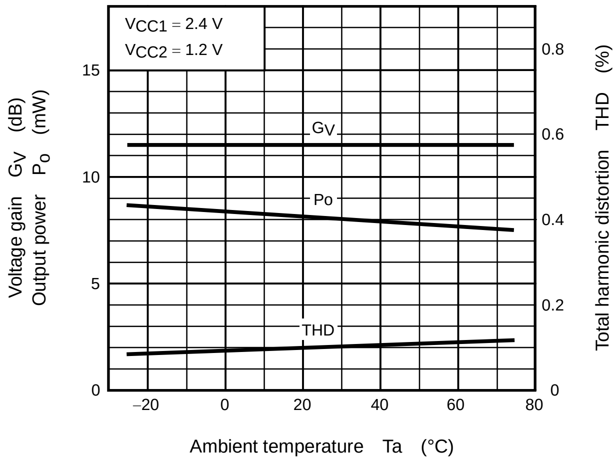

RR – VCC
3 V application
fr = 100 Hz
Vr = −20 dBV
VCC1 = VCC2
C-Cup
OCL
Ripple rejection ratio RR (dB)
Supply voltage VCC (V)


VBEEP (OUT) – VBEEP (IN)
f = 400 Hz (rectangle wave)
RL = 16 Ω
Beep output voltage VBEEP (OUT) (dBV)
Beep input voltage VBEEP (IN) (Vp-p)

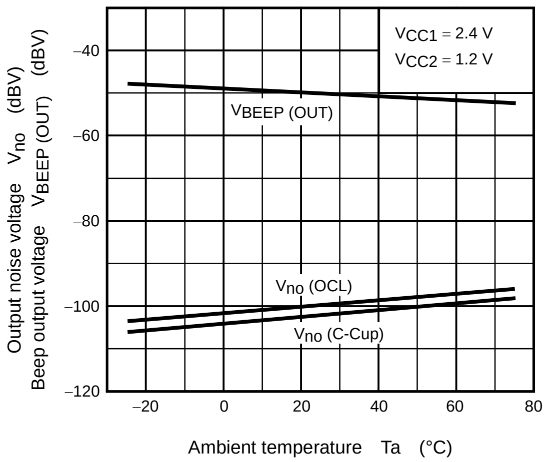
I_{CCQ} – Ta



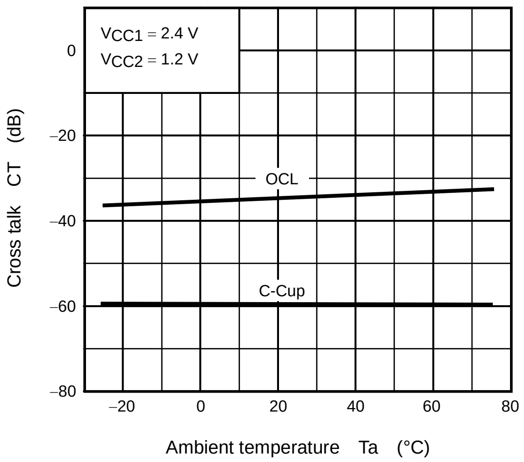
G_V, Po, THD – Ta



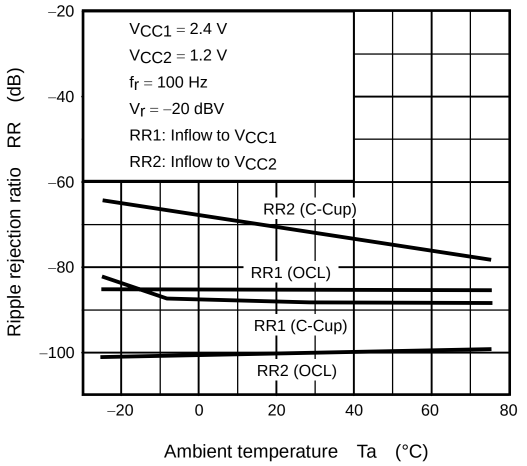
V_{no}, $V_{BEEP (OUT)}$ – Ta



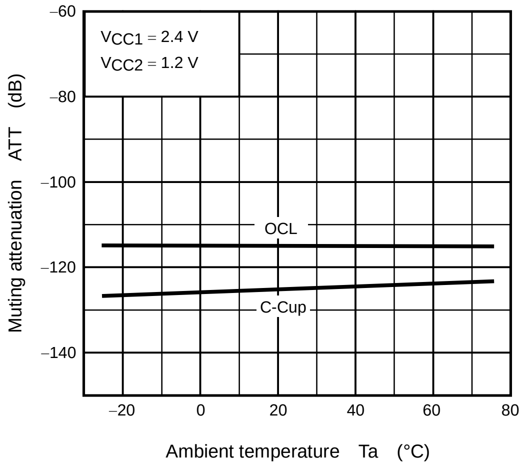
CT – Ta



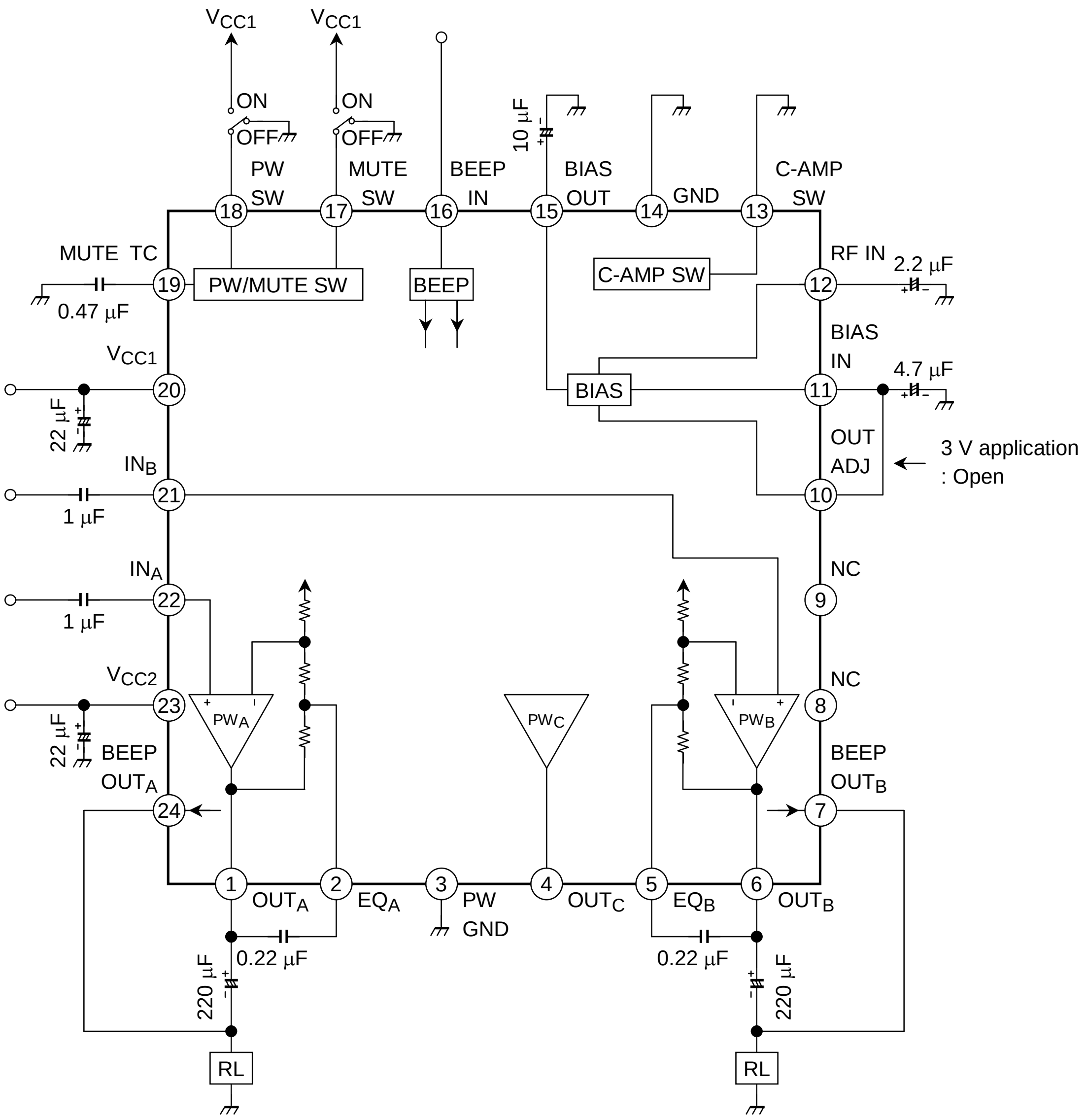
RR – Ta



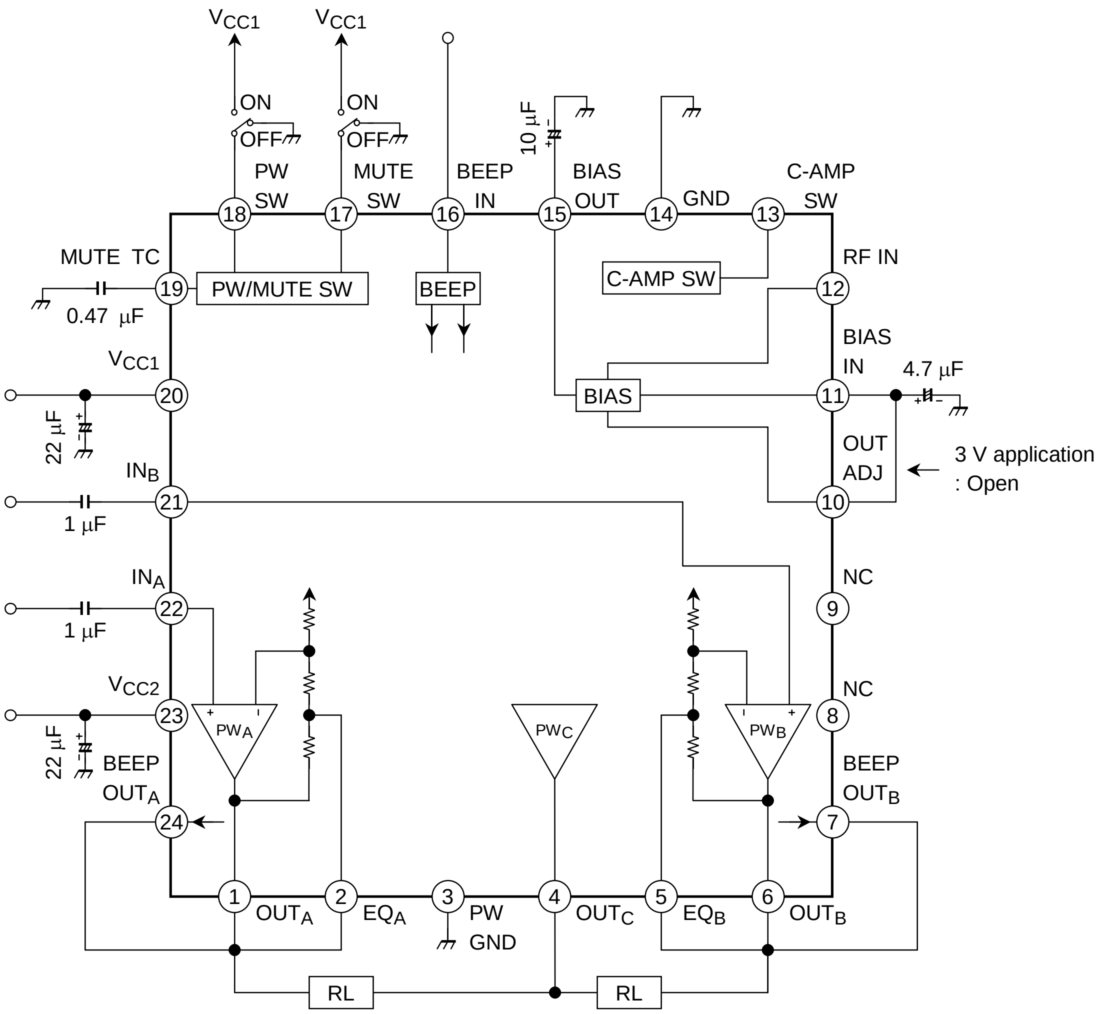
ATT – Ta



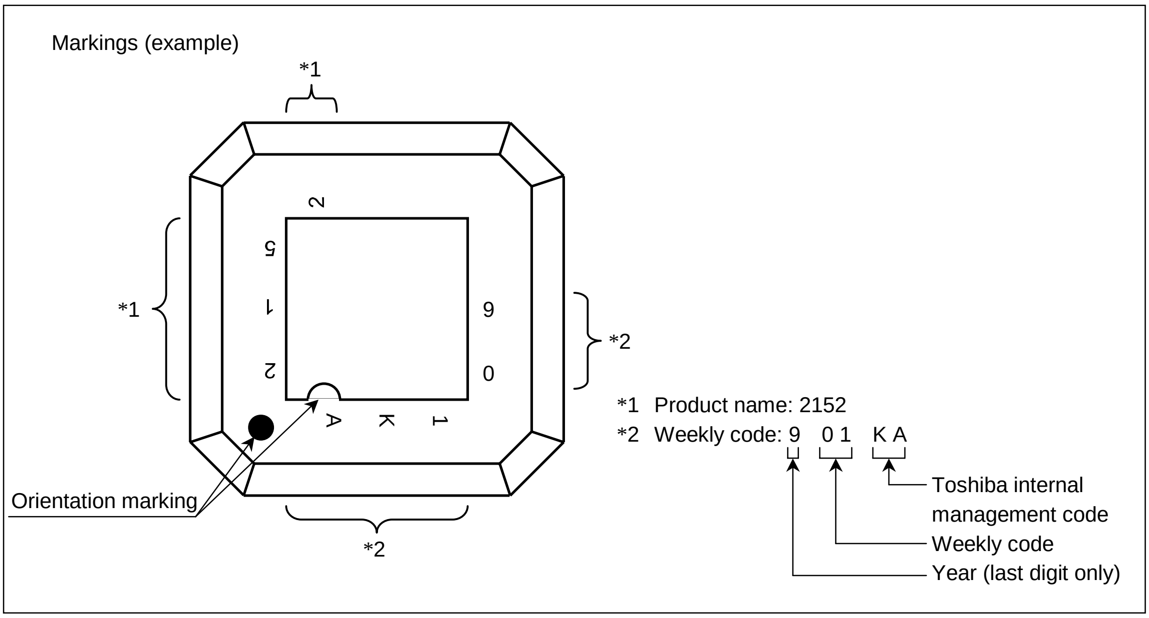
Application Circuit1 (1.5 V Output Coupling Type)



Application Circuit2 (1.5 V OCL Type)



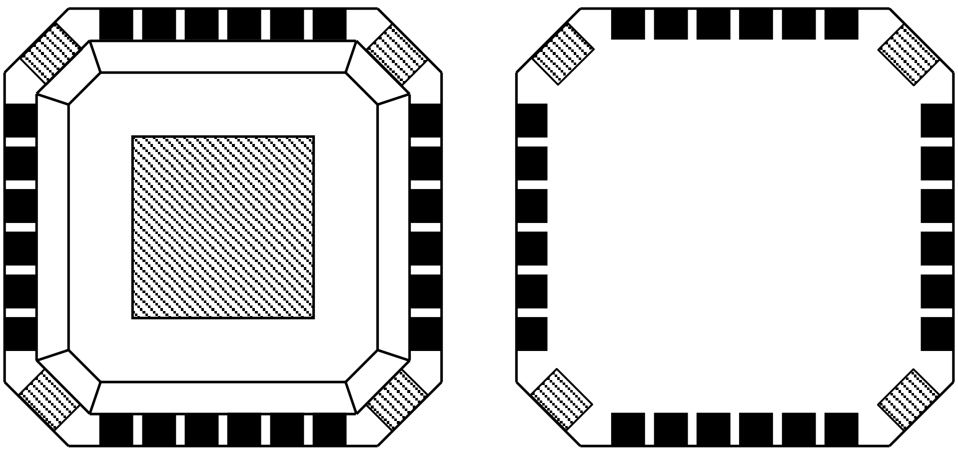
Markings



Precautions when using QON

Package outline

(Upper surface) (lower surface)



Please take into account the following points regarding the QON package

(1) Do not attempt to strengthen the device mechanically by performing soldering on the island sections at the four corners of the package (the sections illustrated by diagonal lines) on the diagram of the lower surface.

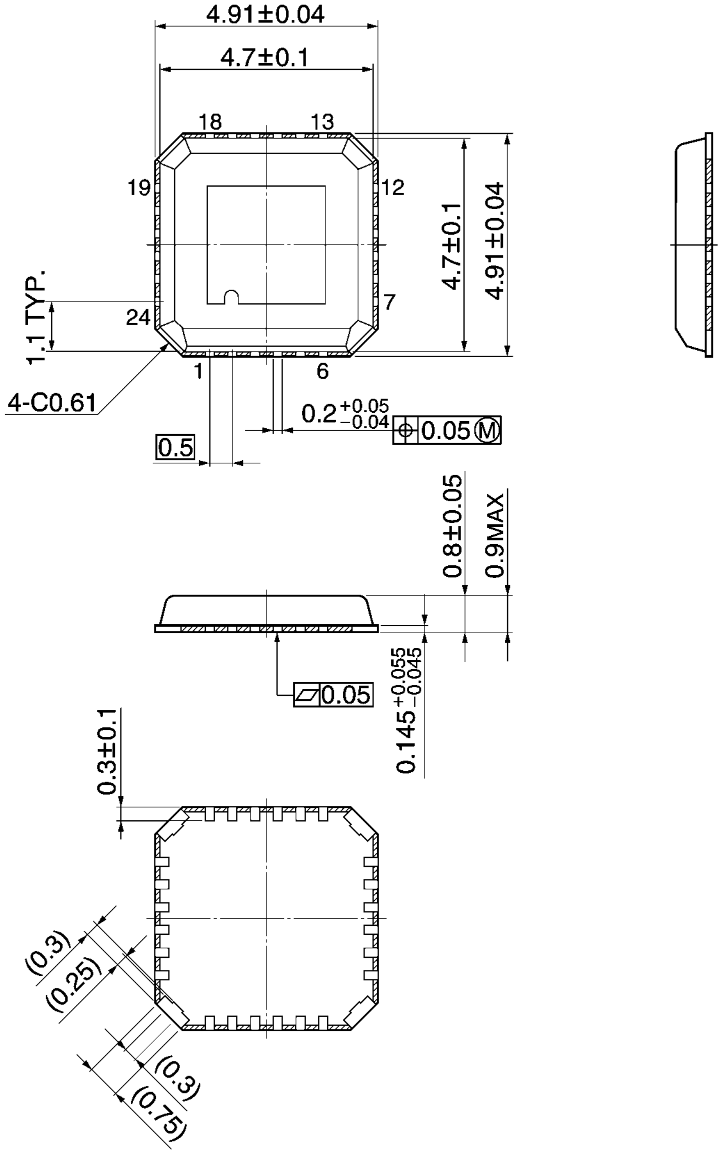
(2) This island sections on the package surfaces (the sections illustrated by diagonal lines on the upper and lower surface diagrams) must be electrically insulated.

*1: Ensure that the island sections on the lower surface (as indicated by the diagonal lines on the diagram) do not come into contact with solder from via holes in the board.

- When mounting or soldering, take care to ensure that neither static electricity nor electrical overstress is applied to the IC (by taking measures to prevent antistatic, leaks etc.).
- When incorporating the device into an item of equipment employ a set design which does not result in voltage being applied directly to the island section.

Package Dimensions

QON24-P-0505-0.50 Unit: mm



Note 1) The solder plating portion in four corners of tne package shall not be treated as an external terminal.

Note 2) Don`t carry out soldering to four corners of the package.

Note 3) [hatched] area : Resin surface

Weight: 0.05 g (typ.)