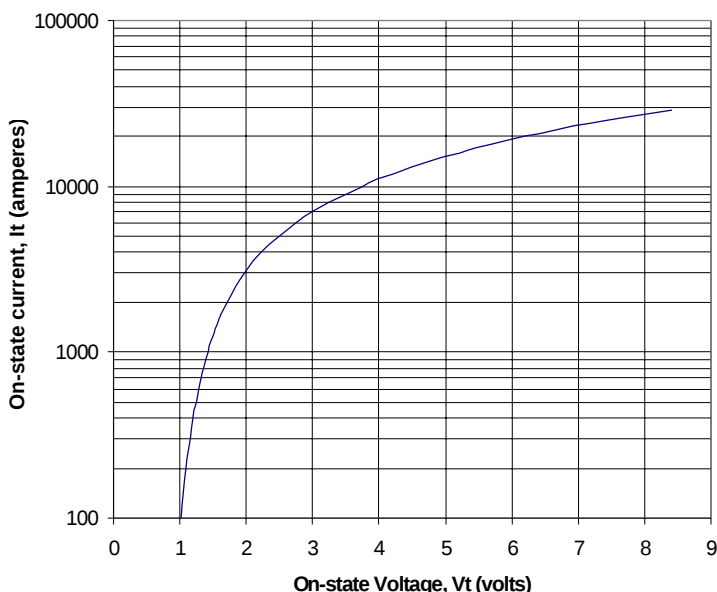


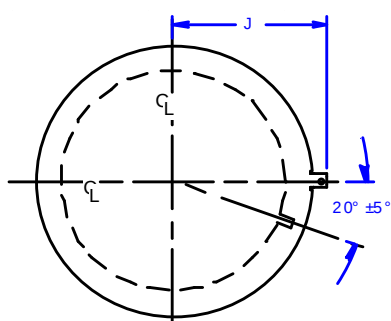
Type C783 reverse blocking thyristor features a 77mm silicon junction design having the exclusive linear amplifying type gate manufactured by the proven multi-diffused process.

It is supplied as a Presspak ready to mount using commercially available heat dissipators or factory-certified, double-sided, cooled assemblies.

### ON-STATE CHARACTERISTIC



### MECHANICAL OUTLINE



AF = 4.35 in (110.5 mm)  
BF = 2.88 in (73.2 mm)  
D = 1.45 in (36.8 mm)

### PRINCIPAL RATINGS AND CHARACTERISTICS

#### OPERATING JUNCTION TEMPERATURE RANGE

-40 to +125°C

|                                                               |                        |                                   |
|---------------------------------------------------------------|------------------------|-----------------------------------|
| Repetitive peak off-state and reverse voltage                 | $V_{DRM}$<br>$V_{RRM}$ | b<br>3800V                        |
| Average on-state current @ $T_c = 70^\circ\text{C}$           | $I_{T(AV)}$            | 1800A                             |
| Peak half cycle surge current for $V_r = 0\text{ V}$          | $I_{TSM}$              | 8.3 ms / 10.0 ms<br>29 kA / 27 kA |
| On-state Voltage @ $I_T = 2000\text{A}$ , $125^\circ\text{C}$ | $V_{TM}$               | 1.71V                             |
| Critical rate of rise of current @ $V_D = 2000\text{V}$       | $di/dt$                | 100A/us                           |
| Critical rate of rise of off-state voltage                    | $dv/dt$                | 500V/us<br>to 0.8V <sub>DRM</sub> |
| Max peak recovery current @ $T_j = 125^\circ\text{C}$         | $I_{RM}$               | 2A/us / 10A/us<br>66A / 250A      |
| Circuit commutated turn-off time (typ)                        | $t_q$                  | 300us                             |

| Model No. | $V_{DRM} / V_{RRM}$<br>-40°C | 0 to +125°C |
|-----------|------------------------------|-------------|
| C783CS    | 3700 V                       | 3800 V      |
| C783CM    | 3600                         | 3700        |
| C783CE    | 3500                         | 3600        |
| C783CD    | 3400                         | 3500        |
| C783CC    | 3300                         | 3400        |
| C783CB    | 3200                         | 3300        |

#### GATE DRIVE REQUIREMENTS

Open circuit voltage / short circuit current 30V / 3A

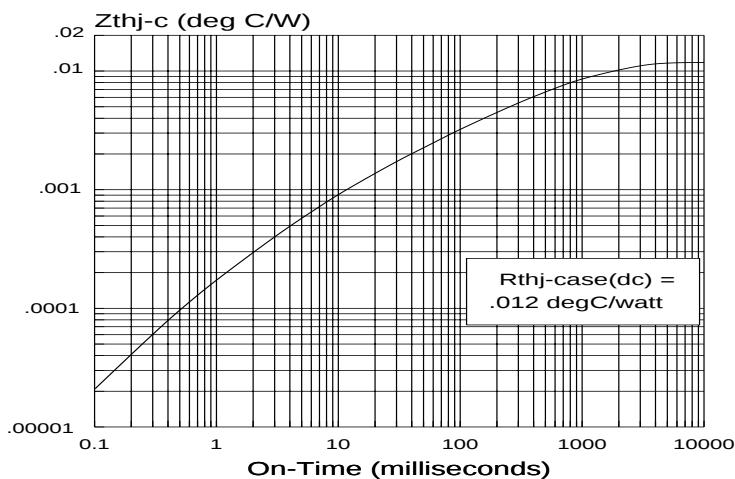
Short circuit risetime 0.5us

Minimum pulse duration 10us

#### EXTERNALLY REQUIRED CLAMPING FORCE

8000 - 9000 lbs. / 35.6 - 40.0 kN

#### THERMAL IMPEDANCE vs. ON-TIME



| TEST                                                                                                          | SYMBOL                               | MIN.        | TYP.     | MAX.         | UNITS                                | TEST CONDITIONS                                                                                                                                                                                                                                                                      |
|---------------------------------------------------------------------------------------------------------------|--------------------------------------|-------------|----------|--------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Peak Reverse and off-state blocking current                                                                   | $I_{\text{DRM}}$<br>$I_{\text{RRM}}$ |             |          | 10<br>100    | mA<br>mA                             | $V = V_{\text{DRM}} = V_{\text{RRM}}$<br>$T_J = 25^\circ\text{C}$<br>$T_J = 125^\circ\text{C}$                                                                                                                                                                                       |
| Effective thermal resistance, junction to case - double-sided cooling                                         | $R_{\theta\text{JC}}$<br>DC          | -           | -        | 0.012        | $^\circ\text{C/W}$                   | Double-sided cooling -<br>(add 0.002 $^\circ\text{C/W}$ for interfaces case to sink)                                                                                                                                                                                                 |
| Critical exponential rate of rise of forward blocking voltage (higher values may cause destructive switching) | dv/dt                                | 500<br>1500 |          |              | V/ $\mu\text{s}$<br>V/ $\mu\text{s}$ | $T_J = +125^\circ\text{C}$ ; $V_{\text{DM}} = 0.8V_{\text{DRM}}$<br>- open gate standard selection<br>- open gate special selection                                                                                                                                                  |
| Delay time                                                                                                    | $t_d$                                |             | 3<br>4   | 3.5<br>5     | $\mu\text{s}$                        | Gate source 30V / 10 $\Omega$<br>rise time 0.5 $\mu\text{s}$ ; $T_J = 25\text{-}125^\circ\text{C}$<br>- Bias $V_{\text{DM}} = 1800\text{V}$<br>- Bias $V_{\text{DM}} = 500\text{V}$                                                                                                  |
| Gate pulse amplitude (operational)                                                                            |                                      |             |          |              |                                      | - $T_C = 40$ to $+125^\circ\text{C}$<br>- Gate source voltage 30 - 40V<br>- Gate source impedance $\sim 10\Omega$<br>- Current rise time $\sim 0.5\mu\text{s}$                                                                                                                       |
| Gate pulse width (operational)                                                                                |                                      |             |          | 10           | $\mu\text{s}$                        | See triggering characteristics                                                                                                                                                                                                                                                       |
| DC gate trigger current (non-operational * )                                                                  | $I_{\text{GT}}$                      | 20          |          | 300          | mA <sub>dc</sub>                     | - $T_C = 25^\circ\text{C}$ , $V_D = 10\text{Vdc}$ , $R_L = 3\Omega$<br>- $T_C = 125^\circ\text{C}$ , $V_D = 0.5V_{\text{DRM}}$ , $R_L = 1\text{k}\Omega$                                                                                                                             |
| DC gate trigger voltage (non-operational * )                                                                  | $V_{\text{GT}}$                      | 0.5         |          | 4.5          | V <sub>dc</sub>                      | - $T_C = 25^\circ\text{C}$ , $V_D = 10\text{Vdc}$<br>- $T_C = 125^\circ\text{C}$ , $V_D = 0.5V_{\text{DRM}}$ , $R_L = 1\text{k}\Omega$                                                                                                                                               |
| Peak on-state voltage                                                                                         | $V_{\text{TM}}$                      |             | -<br>-   | 1.71<br>1.93 | V                                    | $I_T = 2000\text{A}$ duty cycle $\leq 0.01\%$<br>- $T_C = 125^\circ\text{C}$<br>- $T_C = 25^\circ\text{C}$                                                                                                                                                                           |
| Suppressible surge current                                                                                    | $I_{\text{TM(sup)}}$                 |             | 24<br>22 |              | kA                                   | - 60Hz $T_C = 115^\circ\text{C}$<br>- 50Hz resistive circuit<br>sinusoidal blocking voltage applied after completion of surge<br>$0.5V_{\text{RRM}}$ $0.5V_{\text{DRM}}$                                                                                                             |
| Circuit commutated turn-off time                                                                              | $t_q$                                | -           | 200      | 300          | $\mu\text{s}$                        | $T_C = 125^\circ\text{C}$ , $I_{\text{TM}} = 500\text{A}$<br>- Commutating di/dt = 25A/ $\mu\text{s}$<br>- Min. reverse voltage $V_R = 50\text{V}$<br>- Reapplied off state voltage 20V/ $\mu\text{s}$ to $0.8V_{\text{DRM}}$<br>- Gate bias during turn-off interval zero volts/100 |
| * characteristic only, di/dt rating does not apply.                                                           |                                      |             |          |              |                                      |                                                                                                                                                                                                                                                                                      |