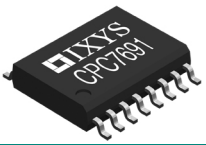
CPC7691
Line Card Access Switch

IXYS INTEGRATED CIRCUITS DIVISION



Features

- Improved switch dV/dt immunity of 1500V/µs
- Drop-In Replacement for CPC7591
- Replaces CPC7581, and allows removal of power-up control discrete components
- TTL logic level inputs for 3.3V logic interfaces
- Smart logic for power-up / hot-plug state control
- Small 16-pin SOIC package
- Monolithic IC reliability
- Low, matched R_{ON}
- Eliminates the need for zero-cross switching
- Flexible switch timing for transition from ringing mode to idle/talk mode.
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting, voltage clamping, and thermal shutdown for SLIC protection
- 5V operation with power consumption < 10.5 mW
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry

Applications

- VoIP Gateways
- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

Description

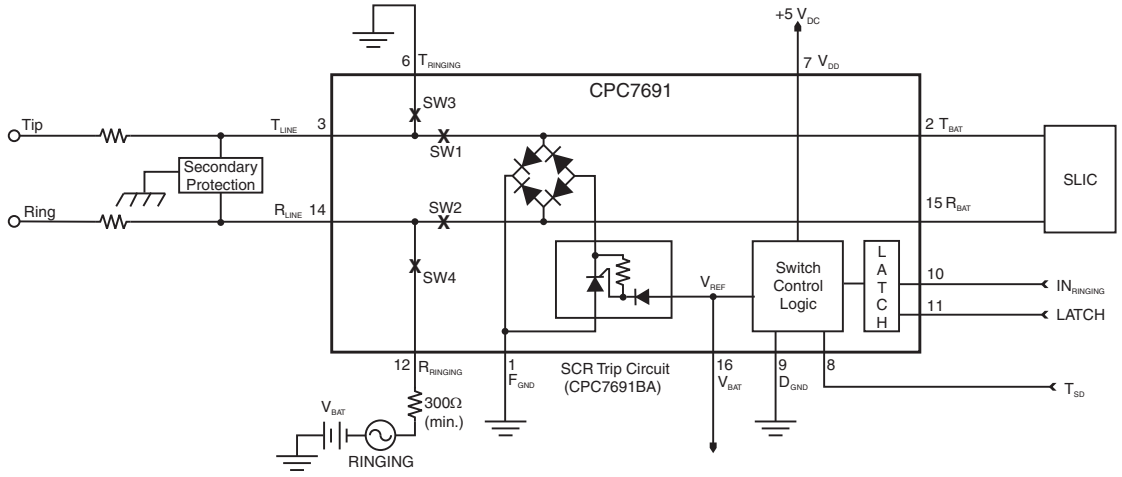
The CPC7691 is a member of IXYS Integrated Circuits Division's third-generation Line Card Access Switch (LCAS) family. This monolithic 4-pole solid state switch, available in a 16-pin SOIC package, provides the necessary functions to replace the 2-Form-C electromechanical ringing relay and it's associated snubber circuitry on traditional analog line cards or contemporary integrated voice and data (IVD) line cards found in Central Office (CO), Access, and PBX equipment. Because this device contains solid state switches for tip and ring line break and for ringing injection/return, it requires only a +5V supply for operation and TTL logic-level inputs for control. The CPC7691 provides stable start-up conditioning during system power-up and for hot plug insertion applications. Once active, the inputs respond to traditional TTL logic levels, enabling the CPC7691 to be used with 3.3V-only logic.

For negative transient voltage protection the CPC7691BA version employs SCRs to provide voltage fold-back protection for the SLIC and subsequent circuitry, while the CPC7691BB version utilizes clamping diodes to the V_{BAT} pin. For positive transient voltage protection all versions provide clamping diodes to the F_{GND} pin.

Ordering Information

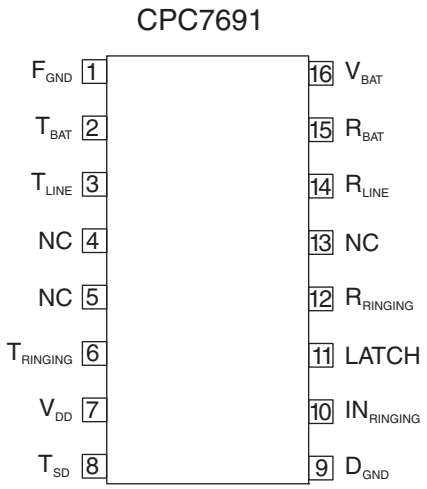
Device	Description
CPC7691BA	With Protection SCR, in Tubes (50/Tube)
CPC7691BATR	With Protection SCR, Tape & Reel (1000/Reel)
CPC7691BB	Without Protection SCR, in Tubes (50/Tube)
CPC7691BBTR	Without Protection SCR, Tape & Reel (1000/Reel)

Figure 1. CPC7691 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pinout

Pin	Name	Description
1	F_{GND}	Fault ground.
2	T_{BAT}	Tip lead to the SLIC.
3	T_{LINE}	Tip lead of the line side.
4	NC	No connection.
5	NC	No connection.
6	$T_{RINGING}$	Ringing generator return.
7	V_{DD}	+5V supply.
8	T_{SD}	Temperature shutdown pin.
9	D_{GND}	Digital ground.
10	$IN_{RINGING}$	Logic control input.
11	LATCH	Data latch enable control input.
12	$R_{RINGING}$	Ringing generator source.
13	NC	No connection.
14	R_{LINE}	Ring lead of the line side.
15	R_{BAT}	Ring lead to the SLIC.
16	V_{BAT}	Battery supply.

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
+5V power supply (V_{DD})	-0.3	7	V
Battery Supply	-	-85	V
D_{GND} to F_{GND} Separation	-5	+5	V
Logic input voltage	-0.3	V_{DD} + 0.3	V
Logic input to switch output isolation	-	320	V
Switch open-contact isolation (SW1, SW2, SW3)	-	320	V
Switch open-contact isolation (SW4)	-	465	V
Operating relative humidity	5	95	%
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C

Absolute maximum electrical ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 ESD Rating

ESD Rating (Human Body Model)
1000V

1.5 General Conditions

Unless otherwise specified, minimum and maximum values are guaranteed by production testing requirements.

Typical values are characteristic of the device at +25°C and are the result of engineering evaluations. They are provided for information purposes only and are not part of the manufacturing testing requirements.

Specifications cover the operating temperature range T_A = -40°C to +85°C. Also, unless otherwise specified all testing is performed with V_{DD} = $5V_{DC}$, logic low input voltage is $0V_{DC}$ and logic high voltage is $5V_{DC}$.

1.6 Switch Specifications

1.6.1 Break Switches: SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW1} (differential) = T_{LINE} to T_{BAT} V_{SW2} (differential) = R_{LINE} to R_{BAT} All-Off state.					
	+25°C, V_{SW} (differential) = -320V to GND V_{SW} (differential) = +260V to -60V	I_{SW}	-	0.1	1	µA
	+85°C, V_{SW} (differential) = -330V to GND V_{SW} (differential) = +270V to -60V			0.3		
	-40°C, V_{SW} (differential) = -310V to GND V_{SW} (differential) = +250V to -60V			0.1		
On-Resistance	I_{SW}(on) = ±10 mA, ±40 mA, R_{BAT} and T_{BAT} = -2V					
	+25°C	R_{ON}	-	14.5	-	Ω
	+85°C			20.5	28	
	-40°C			10.5	-	
On-Resistance Matching	Per SW1 & SW2 On-Resistance test conditions	ΔR_{ON}	-	0.15	0.8	Ω
DC current limit	V_{SW} (on) = ±10V					
	+25°C	I_{SW}	-	300	-	mA
	+85°C		80	160		
	-40°C		-	400	425	
Dynamic current limit (t ≤ 0.5 µs)	Break switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic input to switch output isolation	Logic inputs = GND					
	+25°C, V_{SW} (T_{LINE}, R_{LINE}) = ±320V	I_{SW}	-	0.1	1	µA
	+85°C, V_{SW} (T_{LINE}, R_{LINE}) = ±330V		-	0.3		
	-40°C, V_{SW} (T_{LINE}, R_{LINE}) = ±310V		-	0.1		
Transient Immunity	$100V_{PP}$ Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/µs

1.6.2 Ringing Return Switch: SW3

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW3} (differential) = T_{LINE} to $T_{RINGING}$ All-Off state.					
	+25°C, V_{SW} (differential) = -320V to GND V_{SW} (differential) = +260V to -60V	I_{SW}	-	0.1	1	µA
	+85°C, V_{SW} (differential) = -330V to GND V_{SW} (differential) = +270V to -60V			0.3		
	-40°C, V_{SW} (differential) = -310V to GND V_{SW} (differential) = +250V to -60V			0.1		
On-Resistance	I_{SW}(on) = ±0 mA, ±10 mA					
	+25°C	R_{ON}	-	60	-	Ω
	+85°C			85	100	
	-40°C			45	-	
DC current limit	V_{SW} (on) = ± 10V					
	+25°C	I_{SW}	-	135	-	mA
	+85°C		70	85		
	-40°C		-	210		
Dynamic current limit (t ≤ 0.5 µs)	Ringing switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	2.5	-	A
Logic input to switch output isolation	Logic inputs = GND					
	+25°C, V_{SW} ($T_{RINGING}$, T_{LINE})= ±320V	I_{SW}	-	0.1	1	µA
	+85°C, V_{SW} ($T_{RINGING}$, T_{LINE})= ±330V			0.3		
	-40°C, V_{SW} ($T_{RINGING}$, T_{LINE}) = ±310V			0.1		
Transient Immunity	$100V_{PP}$ Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/µs

1.6.3 Ringing Switch: SW4

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-State Leakage Current	V_{SW4} (differential) = R_{LINE} to $R_{RINGING}$ All-Off state.					
	+25°C V_{SW} (differential) = -255V to +210V V_{SW} (differential) = +255V to -210V	I_{SW}	-	0.05	1	µA
	+85°C V_{SW} (differential) = -270V to +210V V_{SW} (differential) = +270V to -210V			0.1		
	-40°C V_{SW} (differential) = -245V to +210V V_{SW} (differential) = +245V to -210V			0.05		
On-Resistance	I_{SW} (on) = ±70 mA, ±80 mA	R_{ON}	-	10	15	Ω
On Voltage	I_{SW} (on) = ± 1mA	V_{ON}	-	1.5	3	V
On-State Leakage Current	Inputs set for ringing -Measure ringing generator current to ground.	$I_{RINGING}$	-	0.1	0.25	mA
Steady-State Current*	Inputs set for ringing mode.	I_{SW}	-	-	150	mA
Surge Current*	Ringing switches on, all other switches off. Apply ±1 kV 10x1000 µs pulse with appropriate protection in place.	I_{SW}	-	-	2	A
Release Current	SW4 transition from on to off.	$I_{RINGING}$	-	300	-	µA
Logic input to switch output isolation	Logic inputs = GND					
	+25°C, V_{SW} ($R_{RINGING}$, R_{LINE})= ±320V	I_{SW}	-	0.1	1	µA
	+85°C, V_{SW} ($R_{RINGING}$, R_{LINE})= ±330V			0.3		
	-40°C, V_{SW} ($R_{RINGING}$, R_{LINE})= ±310V			0.1		
Transient Immunity	$100V_{PP}$ Square Wave, 100Hz (Not production tested - limits are guaranteed by design and quality control sampling audits.)	dV/dt	1500	2100	-	V/µs

**Secondary protection and current limiting must prevent exceeding this parameter.*

1.7 Digital I/O Electrical Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input Characteristics						
Input voltage, Logic low	Input voltage falling	V_{IL}	0.8	1.1		V
Input voltage, Logic high	Input voltage rising	V_{IH}		1.7	2.0	
Input leakage current, $IN_{RINGING}$, Logic high	V_{DD} = 5.5V, V_{BAT} = -75V, V_{HI} = 2.4V	I_{IH}	-	0.1	1	µA
Input leakage current, $IN_{RINGING}$, Logic low	V_{DD} = 5.5V, V_{BAT} = -75V, V_{IL} = 0.4V	I_{IL}	-	0.1	1	µA
Input leakage current, LATCH Logic high	V_{DD} = 4.5V, V_{BAT} = -75V, V_{IH} = 2.4V	I_{IH}	7	19	-	µA
LATCH Pull-up Minimum Load	V_{DD} = 4.5V, V_{BAT} = -75V, I_{IN} = -10 µA Latch input transitions to logic high.	Logic = High	True			
Input leakage current, LATCH Logic low	V_{DD} = 5.5V, V_{BAT} = -75V, V_{IL} = 0.4V	I_{IL}	-	46	125	µA
Input leakage current, T_{SD} Logic high	V_{DD} = 5.5V, V_{BAT} = -75V, V_{IH} = 2.4V	I_{IH}	10	16	30	µA
Input leakage current, T_{SD} Logic low	V_{DD} = 5.5V, V_{BAT} = -75V, V_{IL} = 0.4V	I_{IL}	10	16	30	µA
Output Characteristics						
Output voltage, T_{SD} Logic high	V_{DD} = 5.5V, V_{BAT} = -75V, I_{TSD} = 10µA	V_{TSD_off}	2.4	V_{DD}	-	V
Output voltage, T_{SD} Logic low	V_{DD} = 5.5V, V_{BAT} = -75V, I_{TSD} = 1mA (Not production tested - limits are guaranteed by design and quality control sampling audits.)	V_{TSD_on}	-	0	0.4	V

1.8 Voltage and Power Specifications

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Voltage Requirements						
V_{DD}	-	V_{DD}	4.5	5.0	5.5	V
V_{BAT}[1]	-	V_{BAT}	-19	-48	-72	V
[1] V_{BAT} is used only for internal protection circuitry. If V_{BAT} goes more positive than -10 V, the device will enter the All-Off state, and will remain in the All-Off state until the battery goes more negative than -15V						
Power Specifications						
Power consumption	V_{DD} = 5V, V_{BAT} = -48V, Measure I_{DD} and I_{BAT},					
	Talk and All-Off states	P	-	5.5	10.5	mW
	Ringing state	P	-	6.5	10.5	mW
V_{DD} current	V_{DD} = 5V, V_{BAT} = -48V					
	Talk and All-Off states	I_{DD}	-	1.1	2.0	mA
	Ringing state	I_{DD}	-	1.3	2.0	mA
V_{BAT} current	V_{DD} = 5V, V_{BAT} = -48V, All states	I_{BAT}	-	0.1	10	µA

1.9 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Protection Diode Bridge						
Forward Voltage drop, continuous current (50/60 Hz)	Apply ± DC current limit of break switches	V_F	-	2.1	3.0	V
Forward Voltage drop, surge current	Apply ± dynamic current limit of break switches		-	5	-	
Protection SCR (CPC7691BA)						
Surge current	-	-	-	-	*	A
Trigger current: Current into V_{BAT} pin	SCR activates, +25°C	I_{TRIG}	-	65	-	mA
	SCR activates, +85°C			45		
Hold current: Current through protection SCR	SCR remains active, +25°C	I_{HOLD}	-	195	-	mA
	SCR remains active, +85°C		110	130		
Gate trigger voltage	$I_{GATE} = I_{TRIGGER}$§	V_{TBAT} or V_{RBAT}	V_{BAT} -4	-	V_{BAT} -2	V
Reverse leakage current	V_{BAT} = -48V	I_{VBAT}	-	0.2	1.0	µA
On-state voltage	0.5A, t = 0.5 µs	V_{TBAT} or V_{RBAT}	-	-3	-	V
	2.0A, t = 0.5 µs			-5		
Temperature Shutdown Specifications						
Shutdown activation temperature	Not production tested - limits are guaranteed by design and Quality Control sampling audits.	T_{TSD_on}	110	125	150	°C
Shutdown circuit hysteresis		T_{TSD_off}	10	-	25	°C

*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.
§V_{BAT} must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

1.10 Truth Table

State	$IN_{RINGING}$	Latch	T_{SD}	Break Switches	Ringing Switches
Talk	0	0	Z [1]	On	Off
Ringing	1			Off	On
Latched [2]	X	1		Unchanged	Unchanged
All-Off	X	X	0	Off	Off

[1] Z = High Impedance. Because T_{SD} has an internal pull-up at this pin, it should be controlled with an open-collector or open-drain type device.
[2] Not a state; indicates existing state can not be changed via the $IN_{RINGING}$ input.

2. Functional Description

2.1 Introduction

The CPC7691 has three states:

- **Talk**. Line break switches SW1 and SW2 closed, ringing switches SW3 and SW4 open.
- **Ringing**. Ringing switches SW3 and SW4 closed, line break switches SW1 and SW2 open.
- **All-Off**. All switches open.

See "Truth Table" on page 8 for more information.

The CPC7691 offers both break-before-make and make-before-break switching techniques when transitioning from the ringing state to the talk state with simple TTL level logic input control. Solid-state switch construction means no impulse noise is generated when switching during ringing cadence or ring trip thereby eliminating the need for external zero-cross switching circuitry. State-control input is via TTL logic levels so no additional driver circuitry is required. The linear line break switches, SW1 and SW2, have exceptionally low R_{ON} and excellent matching characteristics. SW4, the ringing switch, has a minimum open contact breakdown voltage of 465V at +25°C and a minimum dv/dt immunity of 1500v/us, sufficiently high to prevent breakdown in the presence of a transient fault condition (i.e., prevent passing the transient on to the ringing generator).

Integrated into the CPC7691 is an over-voltage clamping circuit, active current limiting, and a thermal shutdown mechanism to provide protection to the SLIC during a fault condition. Positive and negative lightning surge currents are reduced by the current limiting circuitry and hazardous potentials are diverted away from the SLIC via the protection diode bridge or the optional integrated protection SCR. Power-cross potentials are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7691 from an over-voltage fault condition, the use of a secondary protector is required. The secondary protector must limit the voltage seen at the T_{LINE} and R_{LINE} terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is highly recommended. With proper selection of the secondary protector, a line card using the CPC7691 will meet all relevant ITU, LSSGR, TIA/EIA and IEC protection requirements.

The CPC7691 operates from a single +5V supply giving the device extremely low power consumption with virtually any range of battery voltage. The battery voltage used by the CPC7691 has a twofold function. First, for protection purposes, it is used as a current source during fault conditions by the integrated internal protection circuitry. Second, it is used as a reference so that in the event of battery voltage loss, the CPC7691 will enter the All-Off state.

2.2 Start-up

The CPC7691 uses smart logic to monitor the V_{DD} supply. Any time V_{DD} is below the internally set Under Voltage Lock Out (UVLO) threshold, the smart logic places the switch control logic into the All-Off state. An internal pull-up at the LATCH pin holds the CPC7691 in the All-Off state until the LATCH pin is pulled down to a logic low. The control input, $IN_{RINGING}$, must be properly conditioned prior to the assertion of a logic low at the LATCH pin.

2.3 Data Latch

The CPC7691 has an integrated transparent data latch. Latch enable operation is controlled by the application of TTL logic input levels at the LATCH pin. Data into the latch is via the input pin, $IN_{RINGING}$, while the data latch output is an internal node used for state control. When the LATCH enable control pin is at logic 0, the data latch is transparent, and the $IN_{RINGING}$ data signal flows directly through the latch to the state control circuitry. With LATCH = 0, a change at $IN_{RINGING}$ will be reflected by a switch state change.

Whenever LATCH = 1, the data latch is active and data is locked. Subsequent changes at $IN_{RINGING}$ will not result in a change to the control logic or affect the existing state.

As can be seen in "Figure 1. CPC7691 Block Diagram" on page 1 the T_{SD} control bypasses the latch, therefore the T_{SD} control functions are independent of the latch.

On designs that do not wish to individually control the LATCH pins of multiple-port cards it is possible to bus many (or all) of the LATCH pins together to create a single, board-level enable control. The weak internal pull-up allows a fan out of up to 32 when the system's LATCH control driver has a logic low minimum sink capability of 4mA.

2.4 T_{SD} Pin Description

The T_{SD} pin is a bidirectional I/O structure with an internal pull-up current source biased from V_{DD} having a nominal value of 16µA.

As an output, this pin indicates the status of the thermal shutdown circuitry. During normal operation this pin will be pulled up to V_{DD}, but under fault conditions that create excess thermal loading, the CPC7691 will enter thermal shutdown, and a logic low will be output at the T_{SD} pin.

As an input, T_{SD} is utilized to place the CPC7691 into the "All-Off" state. This is accomplished by simply pulling T_{SD} to a TTL input logic low level. When used as an input, forcing a logic high condition at T_{SD} will not override the thermal shutdown capability.

As discussed earlier the T_{SD} control bypasses the latch so that neither the input nor the output control functions are affected by the latch. Consequently, because T_{SD} is independent of the latch, the internal thermal shutdown function and the external "All-Off" control features are not affected by the state of the LATCH input.

For applications using low-voltage logic devices (lower than V_{DD}), IXYS Integrated Circuits Division recommends the use of an open-collector or an open-drain type output to control T_{SD}. This avoids sinking the T_{SD} pull-up bias current to ground during normal operation when the All-Off state is not required. In general, IXYS Integrated Circuits Division recommends all applications use an open-collector or open-drain type device to drive this pin.

2.5 Under Voltage Switch Lock Out Circuitry

2.5.1 Overview

Smart logic in the CPC7691 now provides for switch state control during both power-up and power loss transitions. An internal detector is used to evaluate the V_{DD} supply to determine when to de-assert the under voltage switch lock out circuitry with a rising V_{DD} and when to assert the under voltage switch lock out circuitry with a falling V_{DD}. Any time an unsatisfactory low V_{DD} condition exists, the under voltage lock out circuit overrides user switch control by blocking the information at the external input pins, and conditioning internal switch commands to the All-Off state. Upon restoration of V_{DD}, the switches will remain in the All-Off state until the LATCH input is pulled low.

The rising V_{DD} switch lock-out release threshold is internally set to ensure all internal logic is properly biased and functional before accepting external switch commands at the inputs to control the switch states. For a falling V_{DD} event, the lock-out threshold is set to assure proper logic and switch behavior up to the moment the switches are forced off and external inputs are suppressed.

To facilitate hot plug insertion and system power-up state control, the LATCH pin has an integrated weak pull-up sourced from the V_{DD} power rail that will hold a non-driven LATCH pin at a logic high state. This enables board designers to use the CPC7691 with FPGAs or other devices that provide high impedance outputs during power-up and logic configuration.

2.5.2 Hot Plug and power-up Design Considerations

There are six possible start-up scenarios that can occur during power-up with $T_{SD} \neq 0$. They are:

1. $IN_{RINGING}$ defined at power-up & LATCH = 0
2. $IN_{RINGING}$ defined at power-up & LATCH = 1
3. $IN_{RINGING}$ defined at power-up & LATCH = Z
4. $IN_{RINGING}$ not defined at power-up & LATCH = 0
5. $IN_{RINGING}$ not defined at power-up & LATCH = 1
6. $IN_{RINGING}$ not defined at power-up & LATCH = Z

Under all start-up situations the CPC7691 will condition the internal switch control logic for the All-Off state thereby ensuring all of the switches will remain off during power-up. When V_{DD} requirements have been satisfied the LCAS will complete it's start-up procedure in one of three conditions.

For start-up scenario 1, the CPC7691 will transition from the All-Off state to the state defined by the $IN_{RINGING}$ input when V_{DD} is valid.

For start-up scenarios 2, 3, 5, and 6, the CPC7691 will power up in the All-Off state and remain there until the LATCH pin is pulled low. This allows for an indefinite All-Off state for boards inserted into a powered system but are not configured for service or boards that need to wait for other devices to be configured first.

Scenario 4 will start up with all switches in the All-Off state, but upon the acceptance of a valid V_{DD} the LCAS will revert to either the Talk state or the Ringing state, and thereafter may randomly change states based on input pin leakage currents and loading. This start-up condition should never be utilized as the LCAS state after power-up can not be predicted.

For the start-up scenario when $T_{SD} = 0$ the CPC7691 will condition the internal control logic for the All-Off state as it does when $T_{SD} \neq 0$. Start-up behavior with an initial $T_{SD} = 0$ is dependent on when T_{SD} is released with respect to the status of the Under Voltage Lock Out circuitry. Releasing T_{SD} (which allows the internal pull-up to raise the input from a logic level low to a logic level high before, or concurrent with, the Under Voltage Lock Out deactivation) has no effect on the start-up behavior, and the start-up scenarios previously described are applicable.

With T_{SD} held low beyond the deactivation of the internal Under Voltage Lock Out control, the device will remain in the All-Off state regardless of the levels on the $IN_{RINGING}$ or LATCH inputs. However, it is important to note that the LATCH is fully functional once the Under Voltage Lock Out deactivates. This allows the LATCH to be preconfigured to the state desired with the release of T_{SD}.

2.6 V_{BAT} Pin

Although battery power is not used for switch control, it is required to direct negative potential faults away from the SLIC. Because the CPC7691 requires V_{BAT} to protect the SLIC from negative potential faults, the CPC7691 will deactivate and enter the All-Off state whenever V_{BAT} is unavailable.

2.6.1 Protection

In the presence of a negative potential fault the CPC7691BA will draw current from V_{BAT} to supply trigger current for the internal integrated protection circuitry SCR. This integrated SCR is designed to activate whenever the voltage at T_{BAT} or R_{BAT} drops 2V to 4V below the applied voltage on the V_{BAT} pin. Because the battery supply at this pin is required to source trigger current during negative over-voltage fault conditions at tip and ring, it is important that the net supplying this current be a low impedance path for high speed transients such as lightning. This will permit trigger currents to flow enabling the SCR to activate, and thereby prevent a fault induced negative over-voltage event at the T_{BAT} or R_{BAT} nodes.

Although the CPC7691BB does not have the SCR for negative potential fault protection, it utilizes a power switching diode from each of the T_{BAT} and R_{BAT} nodes to V_{BAT}, which forward conduct in the presence of potentials at these nodes more negative than V_{BAT}. Proper protection requires V_{BAT} to supply sufficient current to counter the transient fault currents restricted by the current limit functions of the break switches.

2.6.2 Battery Voltage Monitor

The CPC7691 also uses the V_{BAT} pin to monitor the battery voltage. If system battery voltage is lost, the CPC7691 immediately enters the All-Off state, and remains in this state until the battery voltage is restored. An internal detector monitoring the system battery voltage forces the All-Off state anytime the battery voltage goes more positive than –10V. The All-Off state is maintained until the battery voltage goes more negative than –15 V. This battery monitor feature draws a small current from V_{BAT} (typically <1μA) and will add slightly to the device's overall power dissipation.

This monitor function performs properly if the CPC7691 and SLIC share a common battery supply origin. Otherwise, if battery is lost to the CPC7691 but not to the SLIC, the V_{BAT} pin will be internally biased by the potential applied at the T_{BAT} or R_{BAT} pins via the internal protection circuitry.

2.7 Ringing to Talk State Switch Timing

The CPC7691 provides, when switching from the Ringing state to the Talk state, the ability to control the release timing of the ringing switches, SW3 and SW4, relative to the activation of the break switches, SW1 and SW2, using simple TTL logic-level inputs. The two available techniques are referred to as make-before-break and break-before-make. When the switch contacts of SW1 and SW2 are closed (made) before the switch contacts of SW3 and SW4 are opened (broken), this is referred to as make-before-break operation. Break-before-make operation occurs when the contacts of SW3 and SW4 are opened (broken) before the switch contacts of SW1 and SW2 are closed (made). With the CPC7691, make-before-break and break-before-make operations can easily be accomplished by applying the proper sequence of inputs to the device.

2.7.1 Make-Before-Break Operation

To use make-before-break operation, change $IN_{RINGING}$ from the Ringing state directly to the Talk state. Assertion of the Talk state opens the ringing return switch, SW3, as the break switches, SW1 and SW2, close. The ringing switch, SW4, remains closed until the next zero-crossing of the ringing current. While in the make-before-break state, ringing potentials in excess of the CPC7691 protection circuitry thresholds will be diverted away from the SLIC. This operational sequence is shown below in the **Ringing to Talk Logic Sequence: Make-Before-Break**.

Ringing to Talk Logic Sequence: Make-Before-Break

State	$IN_{RINGING}$	Latch	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)
Ringing	1	0	Z	-	Off	On	On
Make-Before-Break	0			SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of the ringing cycle. In this transition state, current that is limited to the DC break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On
Talk	0			Zero-cross current has occurred	On	Off	Off

2.7.2 Break-Before-Make Operation

Break-before-make switch timing is performed via the bidirectional T_{SD} interface. As an input, T_{SD} can disable all of the CPC7691 switches when pulled to a logic low. Although logically disabled, an active (closed) ringing switch (SW4) will remain active until the next zero crossing current event. This operational sequence is shown below in the **Ringing to Talk Logic Sequence: Break-Before-Make**.

1. Pull T_{SD} to a logic low to end the ringing state. This opens the ringing return switch (SW3) and prevents any other switches from closing.
2. Keep T_{SD} low for at least one-half the duration of the ringing cycle period to allow sufficient time for a zero crossing current event to occur and for the circuit to enter the break-before-make state.
3. During the T_{SD} low period, clear the $IN_{RINGING}$ input for the talk state (logic low).
4. Release T_{SD} allowing the internal pull-up to activate the break switches.

When using T_{SD} as an input, the two recommended states are “0,” which overrides the logic inputs while forcing an All-Off state, and “Z,” which allows normal switch control via the logic input pins. This requires the use of an open-collector or open-drain type buffer.

Ringing to Talk Logic Sequence: Break-Before-Make

State	$IN_{RINGING}$	Latch	T_{SD}	Timing	Break Switches	Ringing Return Switch (SW3)	Ringing Switch (SW4)
Ringing	1	0	Z	-	Off	On	On
All-Off	1		0	Hold this state for one-half of the ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On
All-Off	0			Zero current has occurred. SW4 has opened	Off	Off	Off
Talk	0		Z	Close break switches	On	Off	Off

Logic states and explanations are provided in the **"Introduction" on page 9**.

2.8 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic change to cease ringing, the ringing switch (SW4), designed to delay deactivation until a zero current event, will remain active until a current zero-crossing occurs. Once on (active) the ringing switch requires a zero current event to turn off and therefore should not be used to switch a DC-only signal. This zero current switching characteristic will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See IXYS Integrated Circuits Division application note **AN-144, Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300Ω in series with the ringing generator is recommended.

2.9 Power Supplies

Both a +5V supply and battery voltage are connected to the CPC7691. Switch state control is powered exclusively by the +5V supply. As a result, the CPC7691 exhibits extremely low power consumption during active and idle states.

2.10 Internal Protection

The CPC7691 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning and fault conditions such as power induction and power-cross.

2.10.1 Current Limiting Function

If a lightning strike transient occurs when the device is in the talk state, the current passed from the line to the internal integrated protection circuitry is restricted by the dynamic current limit response of the active break switches. For instance, during the talk state when a 1000V 10x1000 μs lightning pulse (GR-1089-CORE) is applied to the line though a properly clamped external protector, the current seen at T_{LINE} or R_{LINE} will be a pulse having a typical magnitude of 2.5A with a duration less than 0.5 μs.

Whenever a power-cross fault occurs with the device in the talk state, the current passed though the break switches SW1 and SW2 on to the integrated protection circuit is limited by the DC current limit response of the break switches. The DC current limit specified over temperature ranges from 80mA to 425mA and has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to a power-cross fault condition, the measured current into T_{LINE} or R_{LINE} will decrease as the device temperature increases. If the device temperature rises sufficiently, the thermal shutdown mechanism will activate, and the device will enter the All-Off state.

2.10.2 Diode Bridge/SCR

During a positive potential transient or other fault condition, the fault currents from T_{LINE} or R_{LINE}, limited by the break switches, are conducted through switching power diodes from T_{BAT} and R_{BAT} to ground via F_{GND}. Both versions of the CPC7691 utilize a pair

of switching power diodes connected to F_{GND}, one from T_{BAT} and the other from R_{BAT}, oriented to forward conduct whenever the potential at either T_{BAT} or R_{BAT} becomes positive with respect to F_{GND}.

For negative potential fault situations, the CPC7691BA utilizes a voltage fold-back SCR to direct fault currents to F_{GND}, away from the external devices, while the CPC7691BB uses a pair of switching power diodes to direct the fault currents to V_{BAT}.

The SCR protection technique of the CPC7691BA uses the V_{BAT} supply as a reference and as a current source for the SCR trigger to activate the SCR. During a negative transient event resulting in a bias at T_{BAT} or R_{BAT} of 2V to 4V more negative than V_{BAT}, the SCR conducts and faults are shunted to F_{GND}. In order for the SCR to crowbar (or foldback), the SCR's on-voltage (see **"Protection Circuitry Electrical Specifications" on page 8**) must be less than the applied voltage at the V_{BAT} pin. If the V_{BAT} voltage is less negative than the SCR on-voltage, or if the V_{BAT} supply is unable to source the trigger current, the SCR will not crowbar.

Unlike the CPC7691BA which uses one-half of a diode bridge and an SCR for the internal protection, the CPC7691BB instead uses a full diode bridge to clamp both polarities of a transient fault. In the CPC7691BB a pair of power switching diodes are used to direct excessive negative potentials at the T_{BAT} and R_{BAT} nodes into V_{BAT}. These diodes are oriented so that anytime the potentials at the T_{BAT} or R_{BAT} nodes become more negative than V_{BAT} they forward conduct.

Because these diodes direct negative potential faults to the V_{BAT} pin, the battery supply must be capable of sourcing currents equal in magnitude to the total currents of all simultaneous faults. As mentioned earlier, the fault currents are restricted by the current limits of the break switches.

Use of the CPC7691BA is recommended for applications where the local V_{BAT} supply is incapable of sourcing the cumulative transient current demands of simultaneous multiple port faults.

2.10.3 Thermal Shutdown

The thermal shutdown mechanism activates when the device die temperature reaches a minimum of 110°C, placing the device in the All-Off state regardless of logic input. During thermal shutdown events the T_{SD} pin will output a logic low with a nominal 0V level. A logic high is output from the T_{SD} pin during normal operation with a typical output level equal to V_{DD}.

When presented with short duration transients such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross event, fault currents limited by the DC current limit function flowing through the active switches will cause the device temperature to rise until the thermal shutdown mechanism activates. Activation of the thermal shutdown mechanism forces the CPC7691 into the All-Off state. At this point the current measured into T_{LINE} or R_{LINE} will drop to zero. Once the device enters thermal shutdown it will remain in the All-Off state until the device temperature drops below the de-activation level of the thermal shutdown circuit. This permits the device to autonomously return to normal operation.

If the fault condition has not passed, the limited current will again flow through the active switches and heating will resume, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector will activate shunting the fault current to ground.

2.11 External Protection Elements

The CPC7691 requires only over-voltage secondary protection on the loop (line) side of the device. The integrated protection feature described above negates the need for additional external protection on the SLIC side. The secondary protector must limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7691. A foldback or crowbar type protector is recommended to minimize stresses on the switches.

Consult IXYS Integrated Circuits Division's application note, **AN-144, Impulse Noise Benefits of Line Card Access Switches** for equations related to the specifications of external secondary protectors, fuse resistors and PTCs.

3. Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC7691BA / CPC7691BB	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

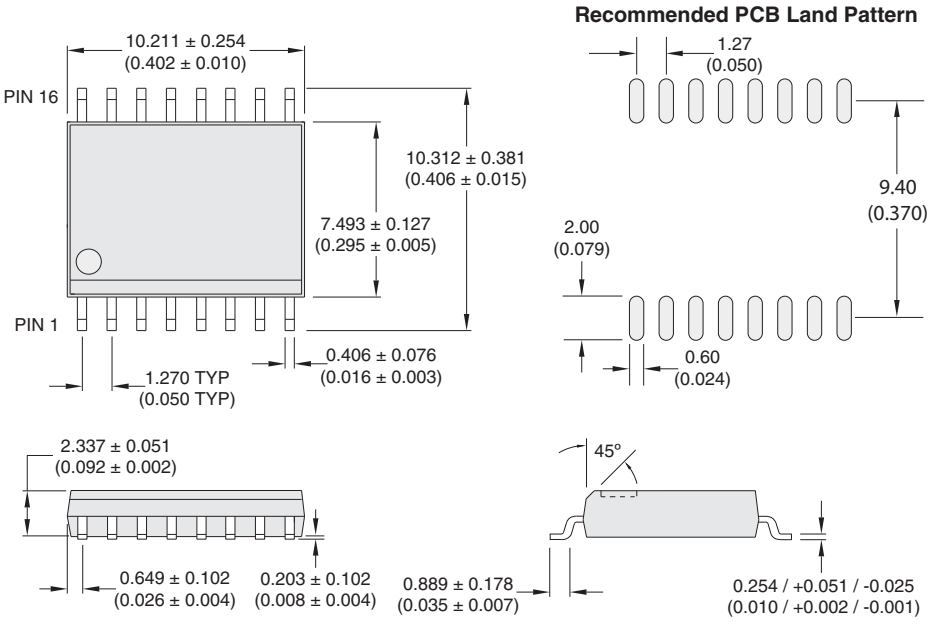
This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC7691BA / CPC7691BB	260°C for 30 seconds

3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

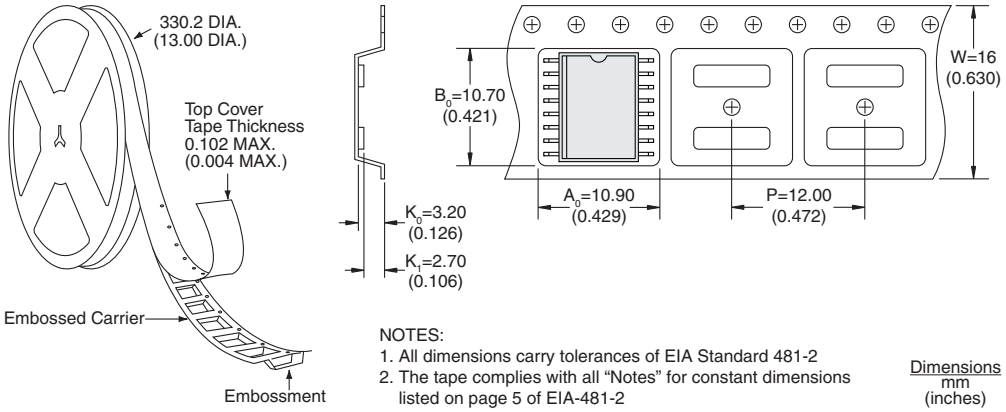
3.5 Package Mechanical Dimensions



NOTES:
1. Coplanarity = 0.1016 (0.004) max.
2. Leadframe thickness does not include solder plating (1000 microinch maximum).

DIMENSIONS
mm
(inches)

3.6 Tape and Reel Specifications



NOTES:
1. All dimensions carry tolerances of EIA Standard 481-2
2. The tape complies with all "Notes" for constant dimensions listed on page 5 of EIA-481-2

Dimensions
mm
(inches)

For additional information please visit www.ixysic.com

Specification: DS-CPC7691-R01

6/10/2013