Document Number: MW6IC2240N
Rev. 6, 12/2008

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MW6IC2240NBR1
MW6IC2240GNBR1

2110-2170 MHz, 4.5 W AVG., 28 V
2 x W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MW6IC2240N wideband integrated circuit is designed with on-chip matching that makes it usable from 2110 to 2170 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulation formats including TD-SCDMA.

Final Application

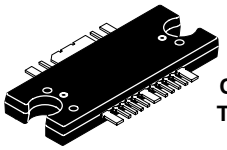
- Typical 2-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 210 mA, I_{DQ2} = 370 mA, P_{out} = 4.5 Watts Avg., f = 2157 MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 28 dB
  Power Added Efficiency — 15%
  IM3 @ 10 MHz Offset — -43 dBc in 3.84 MHz Bandwidth
  ACPR @ 5 MHz Offset — -46 dBc in 3.84 MHz Bandwidth

Driver Application

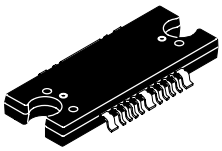
- Typical 2-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 300 mA, I_{DQ2} = 320 mA, P_{out} = 25 dBm, Full Frequency Band (2110-2170 MHz), Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 29 dB
  IM3 @ 10 MHz Offset — -59 dBc in 3.84 MHz Bandwidth
  ACPR @ 5 MHz Offset — -62 dBc in 3.84 MHz Bandwidth
- Capable of Handling 3:1 VSWR, @ 28 Vdc, 2170 MHz, 20 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 10 Watts CW P_{out}.

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >3 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel



CASE 1329-09
TO-272 WB-16
PLASTIC
MW6IC2240NBR1



CASE 1329A-04
TO-272 WB-16 GULL
PLASTIC
MW6IC2240GNBR1

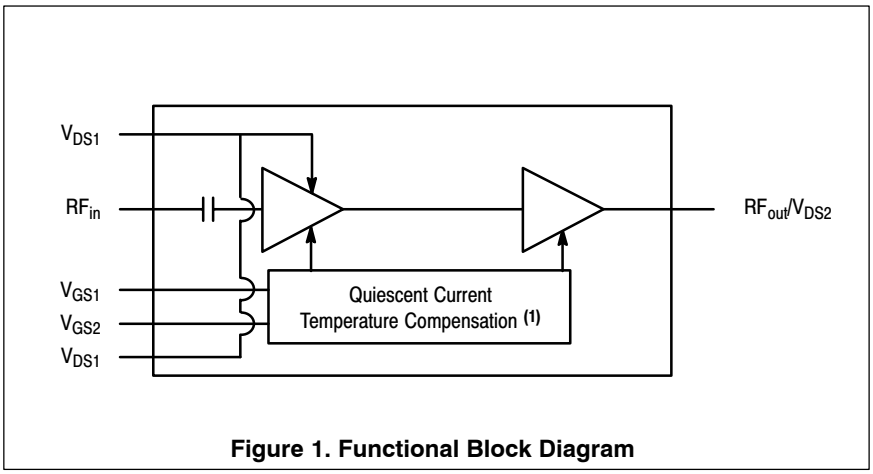
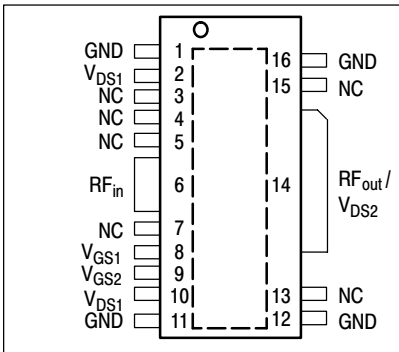


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	23	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
W-CDMA Application (P_{out} = 4.5 W Avg.)	Stage 1, 28 Vdc, I_{DQ} = 210 mA		1.8	
	Stage 2, 28 Vdc, I_{DQ} = 370 mA		1.0	
W-CDMA Application (P_{out} = 40 W CW)	Stage 1, 28 Vdc, I_{DQ} = 110 mA		2.0	
	Stage 2, 28 Vdc, I_{DQ} = 370 mA		0.87	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Wideband 2110-2170 MHz Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 210 mA, I_{DQ2} = 370 mA, P_{out} = 4.5 W Avg., f = 2157 MHz, 2-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset. IM3 measured in 3.84 MHz Channel Bandwidth @ ±10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.					
Power Gain	G_{ps}	25.5	28	30	dB
Power Added Efficiency	PAE	13.7	15	—	%
Intermodulation Distortion	IM3	—	-43	-40	dBc
Adjacent Channel Power Ratio	ACPR	—	-46	-43	dBc
Input Return Loss	IRL	—	-15	-10	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

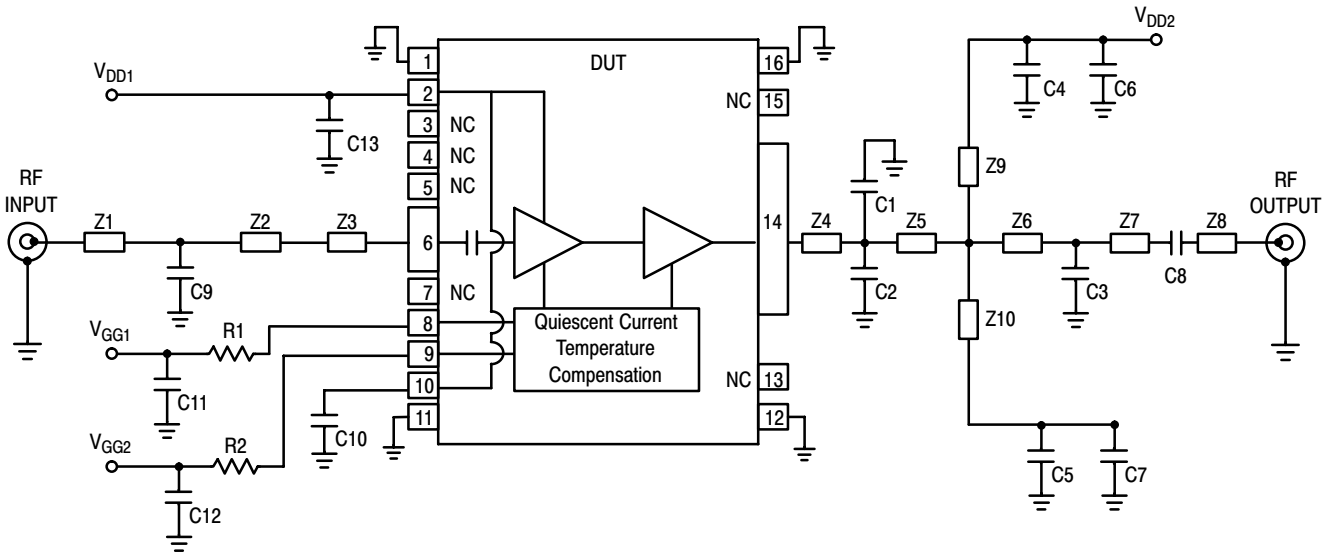
Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 210 mA, I_{DQ2} = 370 mA, 2110 MHz<Frequency<2170 MHz					
Video Bandwidth (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	30	—	MHz
Quiescent Current Accuracy over Temperature with 18 kΩ Gate Feed Resistors (-10 to 85°C) (1)	ΔI_{QT}	—	±5	—	%
Gain Flatness in 30 MHz Bandwidth @ P_{out} = 1 W CW	G_F	—	0.2	—	dB
Deviation from Linear Phase in 30 MHz Bandwidth @ P_{out} = 1 W CW	Φ	—	±1	—	°
Delay @ P_{out} = 1 W CW Including Output Matching	Delay	—	2.8	—	ns
Part-to-Part Phase Variation @ P_{out} = 1 W CW	ΔΦ	—	±9	—	°

Table 6. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 110 mA, I_{DQ2} = 370 mA, 2110 MHz<Frequency<2170 MHz					
Saturated Pulsed Output Power (8 μsec(on), 1 msec(off))	P_{sat}	—	60	—	W

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.



Z1*	1.73″ x 0.090″ Microstrip	Z7*	0.94″ x 0.090″ Microstrip
Z2*	0.47″ x 0.090″ Microstrip	Z8	0.34″ x 0.090″ Microstrip
Z3	0.13″ x 0.040″ Microstrip	Z9, Z10	1.00″ x 0.080″ Microstrip
Z4*	0.22″ x 0.315″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z5*	0.34″ x 0.315″ Microstrip		
Z6*	0.34″ x 0.090″ Microstrip	* Variable for tuning	

Figure 3. MW6IC2240NBR1(GNBR1) Test Circuit Schematic

Table 7. MW6IC2240NBR1(GNBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	1.5 pF Chip Capacitors	ATC100B1R5BT500XT	ATC
C3	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C4, C5	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C6, C7, C10, C11, C12, C13	4.7 µF Chip Capacitors	C4532X5R1H475MT	TDK
C8	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C9	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1	18 kΩ, 1/4 W Chip Resistor	CRCW12061802FKEA	Vishay
R2	8.2 kΩ, 1/4 W Chip Resistor	CRCW12068201FKEA	Vishay

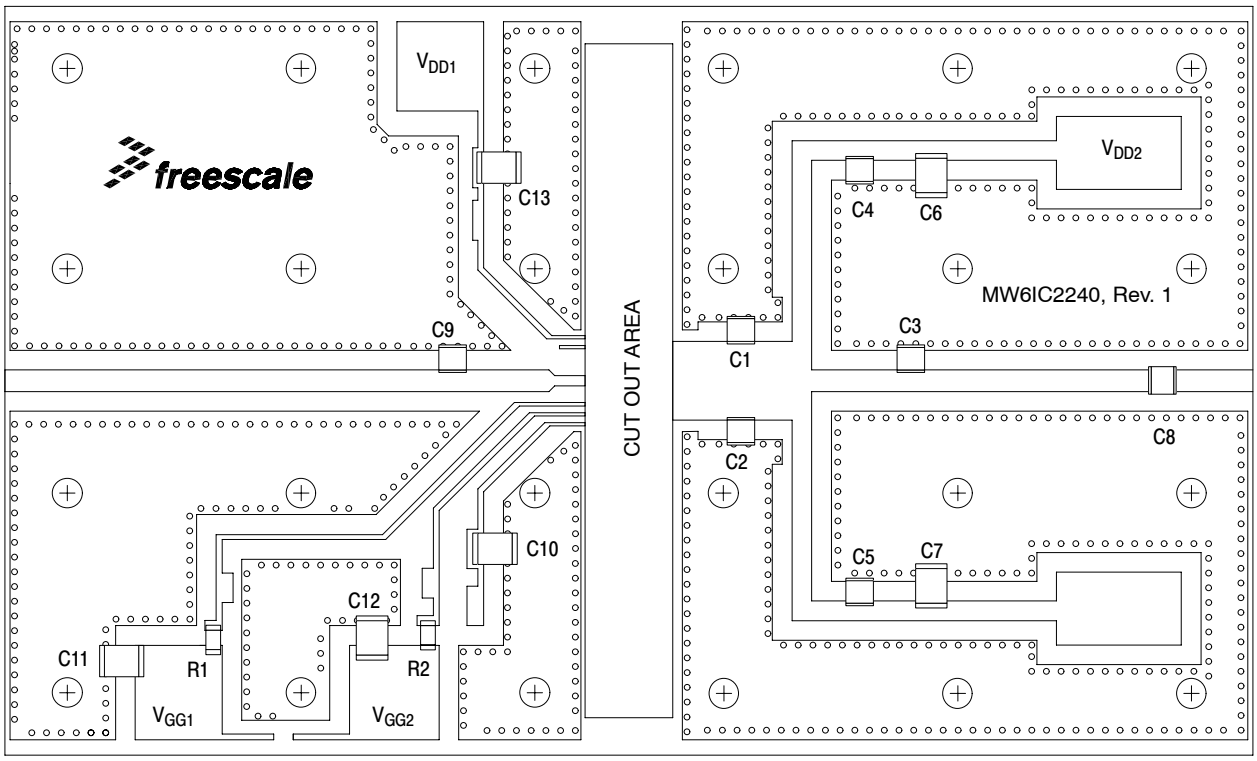


Figure 4. MW6IC2240NBR1(GNBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

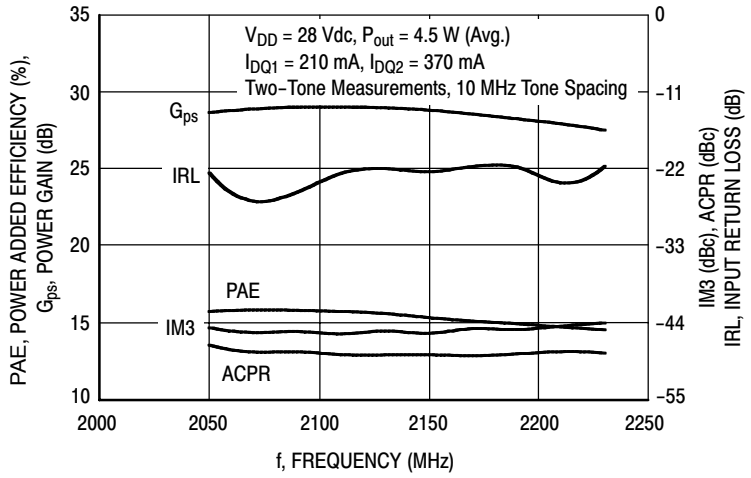


Figure 5. 2-Carrier W-CDMA Wideband Performance @ P_{out} = 4.5 Watts Avg.

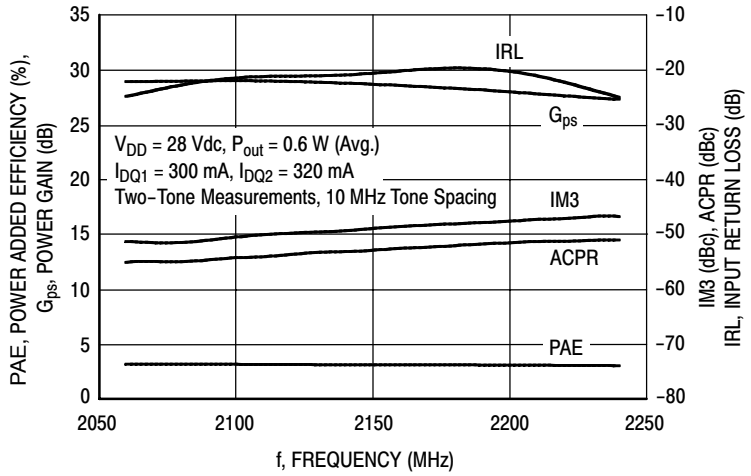


Figure 6. 2-Carrier W-CDMA Wideband Performance @ P_{out} = 0.6 Watts Avg.

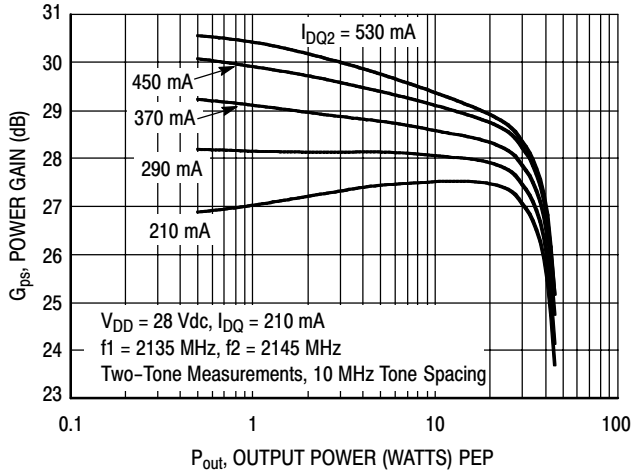


Figure 7. Two-Tone Power Gain versus Output Power

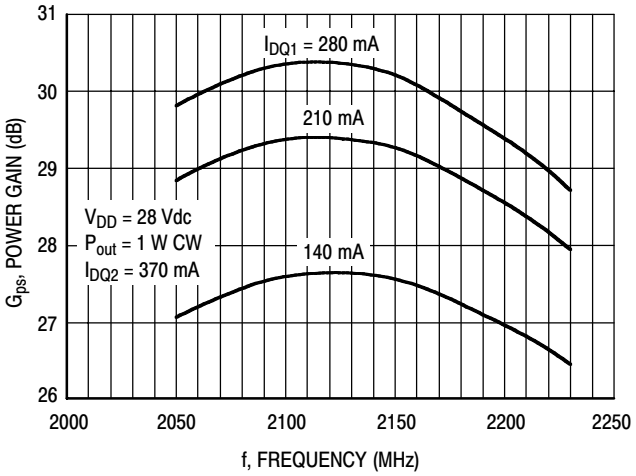


Figure 8. Frequency Response versus Current

TYPICAL CHARACTERISTICS

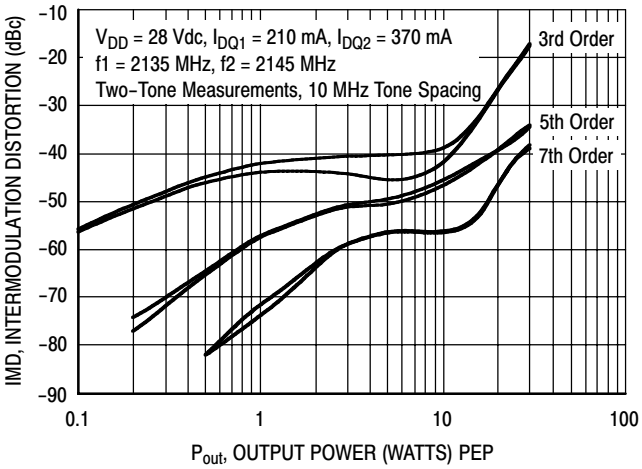


Figure 9. Intermodulation Distortion Products versus Output Power

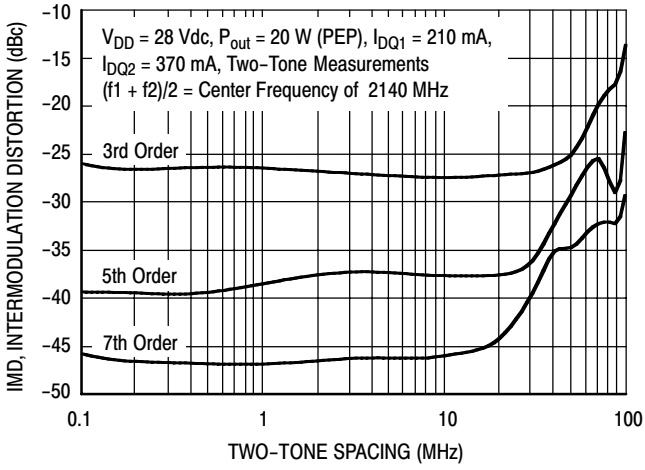


Figure 10. Intermodulation Distortion Products versus Tone Spacing

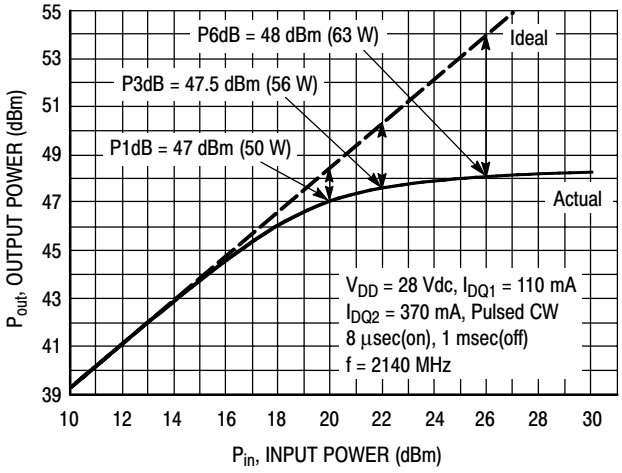


Figure 11. Pulsed CW Output Power versus Input Power

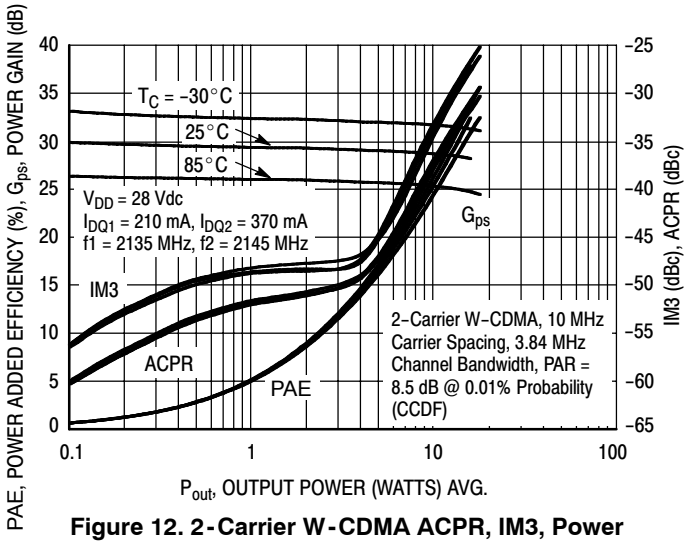


Figure 12. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Power Added Efficiency versus Output Power

TYPICAL CHARACTERISTICS

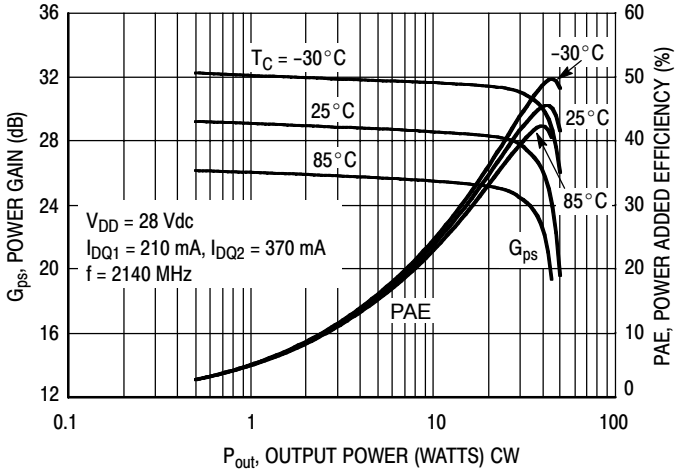


Figure 13. Power Gain and Power Added Efficiency versus Output Power

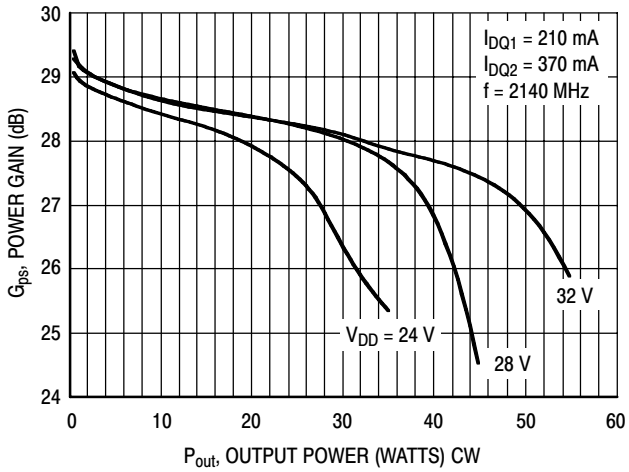
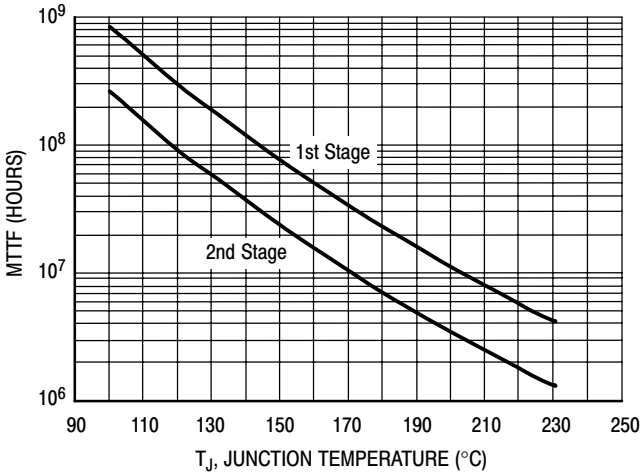


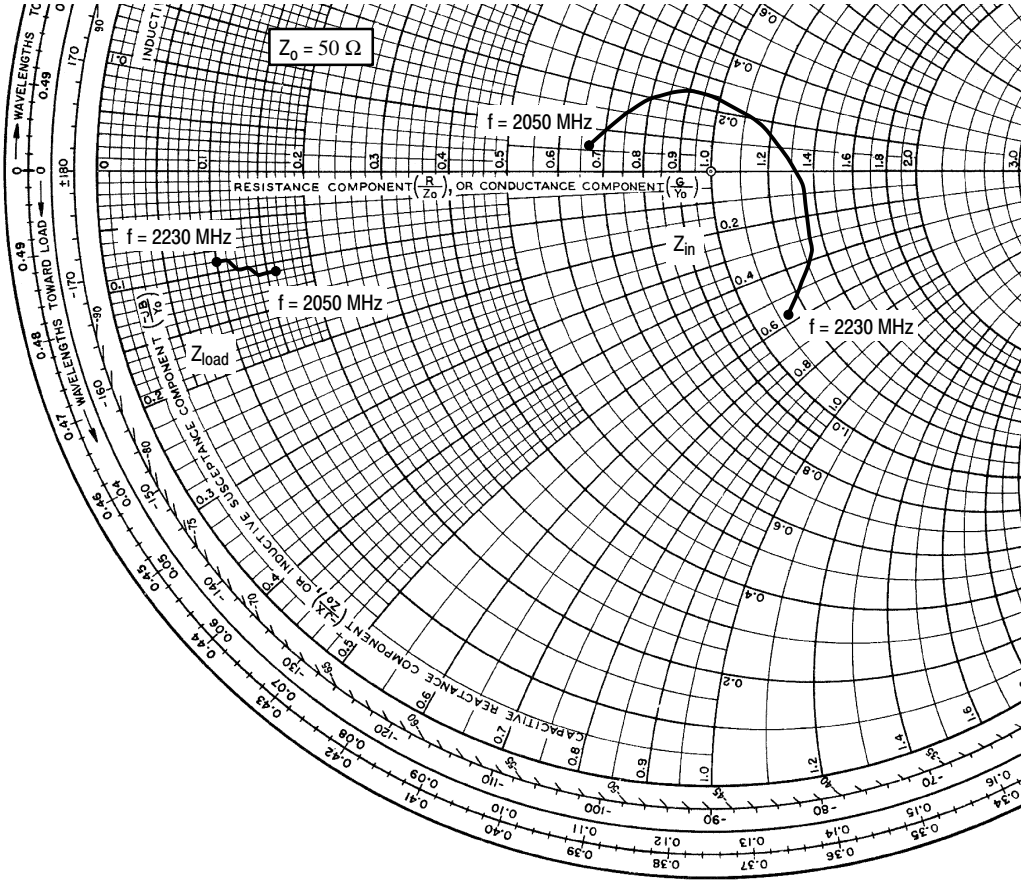
Figure 14. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 4.5 W Avg., and PAE = 15%.

MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 15. MTTF versus Junction Temperature



V_{DD} = 28 Vdc, I_{DQ1} = 210 mA, I_{DQ2} = 370 mA, P_{out} = 4.5 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
2050	33.723 + j3.048	7.971 - j5.705
2080	38.052 + j8.201	7.559 - j5.532
2110	45.972 + j12.306	7.117 - j5.345
2140	59.075 + j9.272	6.642 - j5.119
2170	68.368 - j3.227	6.132 - j4.891
2200	67.177 - j19.071	5.626 - j4.619
2230	58.213 - j28.879	5.118 - j4.305

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

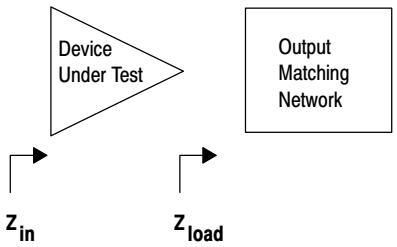
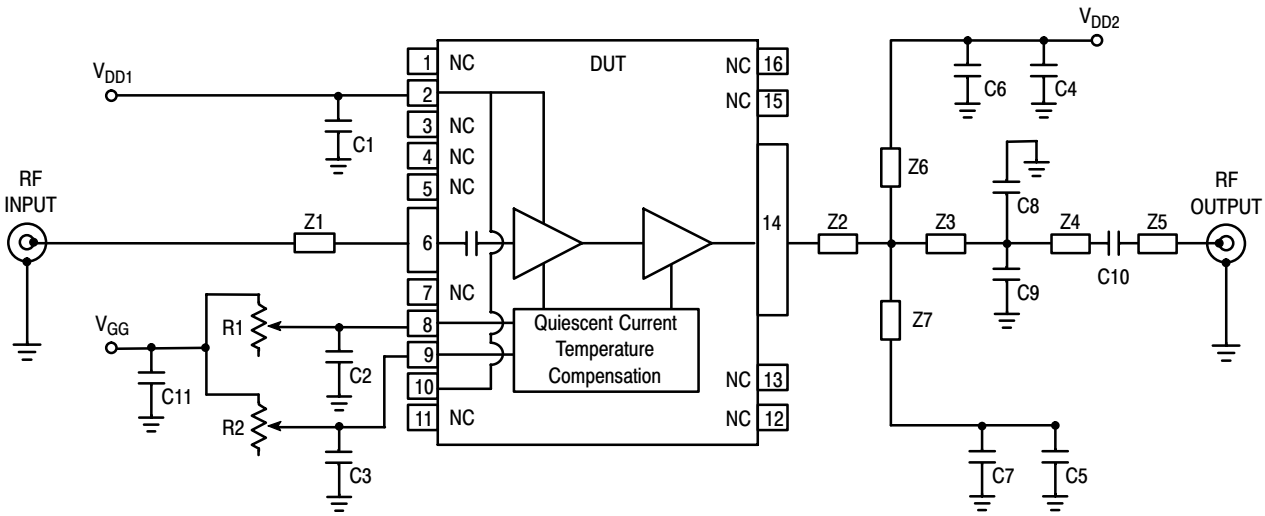


Figure 16. Series Equivalent Input and Load Impedance

Table 8. Common Source Scattering Parameters (V_{DD} = 28 V, I_{DQ1} = 210 mA, I_{DQ2} = 370 mA, 50 Ohm System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
1000	0.788	131.360	0.0013	63.602	0.0020	25.353	0.9940	172.664
1200	0.713	113.326	0.0012	42.219	0.0094	10.742	0.9910	169.954
1400	0.584	86.885	0.0007	55.210	0.1180	-39.325	0.9850	166.452
1600	0.389	41.593	0.0006	117.726	0.6690	-92.822	0.9780	161.752
1800	0.239	-54.753	0.0022	122.409	4.9300	-164.584	0.9310	152.388
2000	0.221	-162.180	0.0036	118.178	21.396	49.432	0.6120	151.441
2200	0.216	-38.746	0.0057	68.626	19.739	-105.946	0.7530	-177.800
2400	0.467	-113.440	0.0043	64.758	7.8281	166.887	0.9010	171.868
2600	0.539	-153.020	0.0044	48.498	3.8868	113.310	0.9350	167.252
2800	0.635	-171.630	0.0044	52.829	2.4331	69.460	0.9480	164.137
3000	0.716	169.263	0.0049	56.398	1.6119	29.135	0.9570	161.593



Z1	1.180″ x 0.056″ Microstrip	Z5	0.727″ x 0.056″ Microstrip
Z2	0.136″ x 0.237″ Microstrip	Z6, Z7	1.066″ x 0.078″ Microstrip
Z3	0.096″ x 0.237″ Microstrip	PCB	Taconic TLX8, 0.020″, ε_r = 2.55
Z4	0.181″ x 0.237″ Microstrip		

Figure 17. MW6IC2240NBR1(GNBR1) Test Circuit Schematic — TD-SCDMA

Table 9. MW6IC2240NBR1(GNBR1) Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1, C4, C5, C11	2.2 μF Chip Capacitors	C3225X5R1H225MT	TDK
C2, C3	100 nF Chip Capacitors	C1206CK104K5RC	Kemet
C8, C9	1.2 pF Chip Capacitors	08051J1R2BBS	AVX
C10	6.8 pF Chip Capacitor	08051J6R8CBS	AVX
C6, C7	5.6 pF Chip Capacitors	08051J5R6CBS	AVX
R1, R2	5 kΩ Potentiometer CMS Cermet Multi-turn	3224W	Bourns

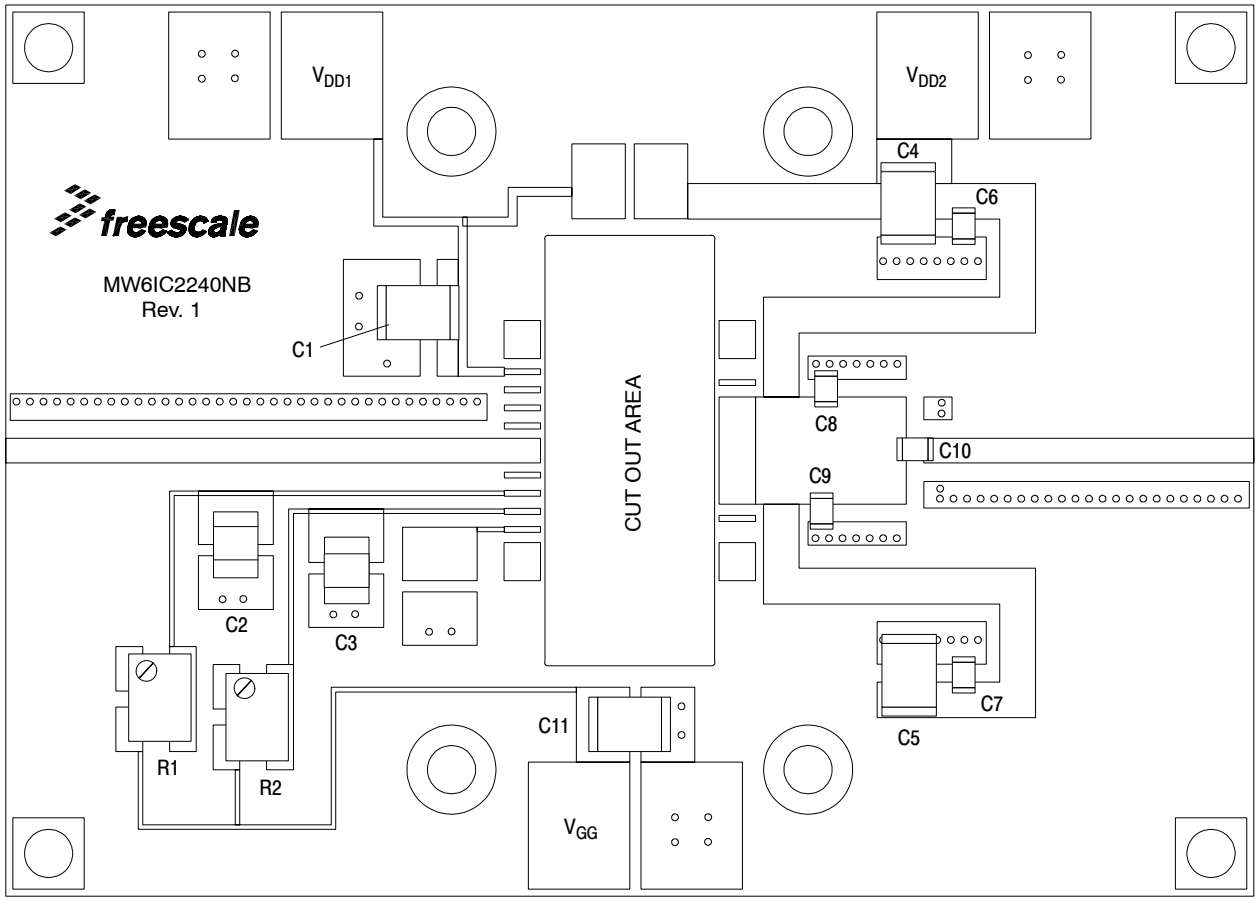


Figure 18. MW6IC2240NBR1(GNBR1) Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

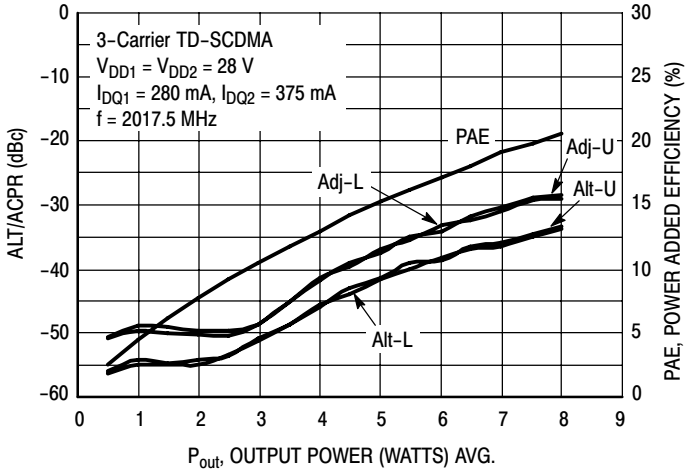


Figure 19. 3-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

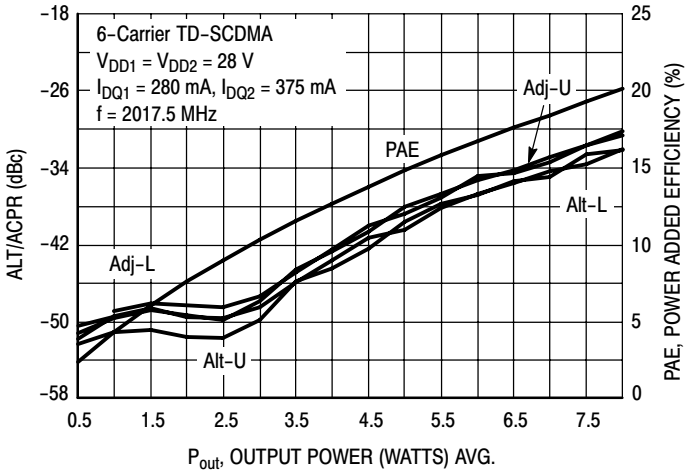


Figure 20. 6-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

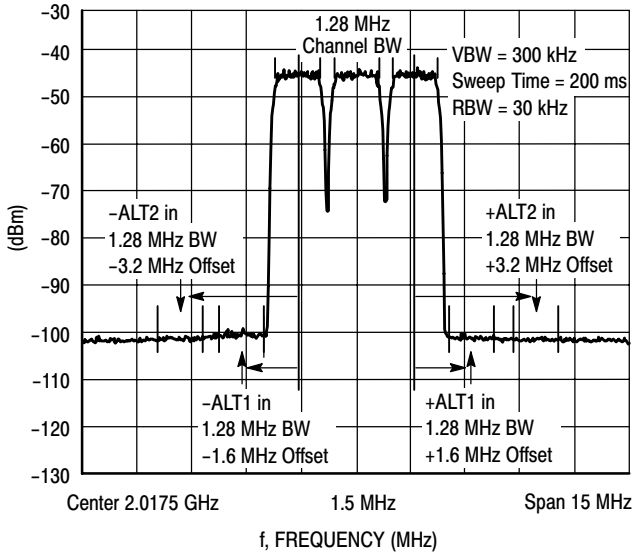


Figure 21. 3-Carrier TD-SCDMA Spectrum

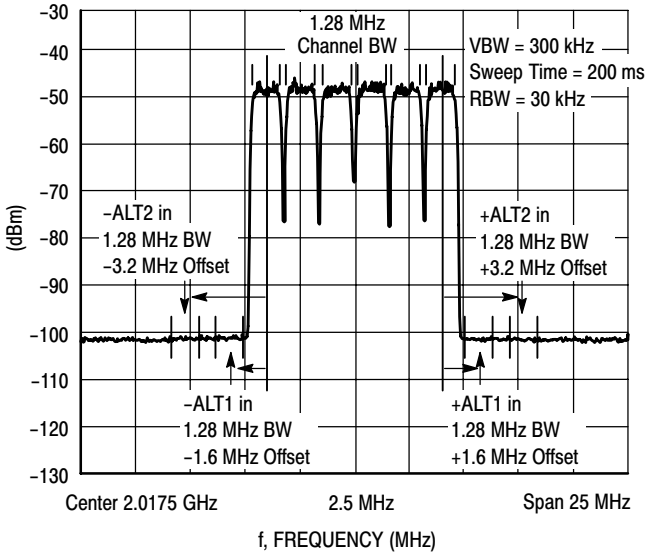
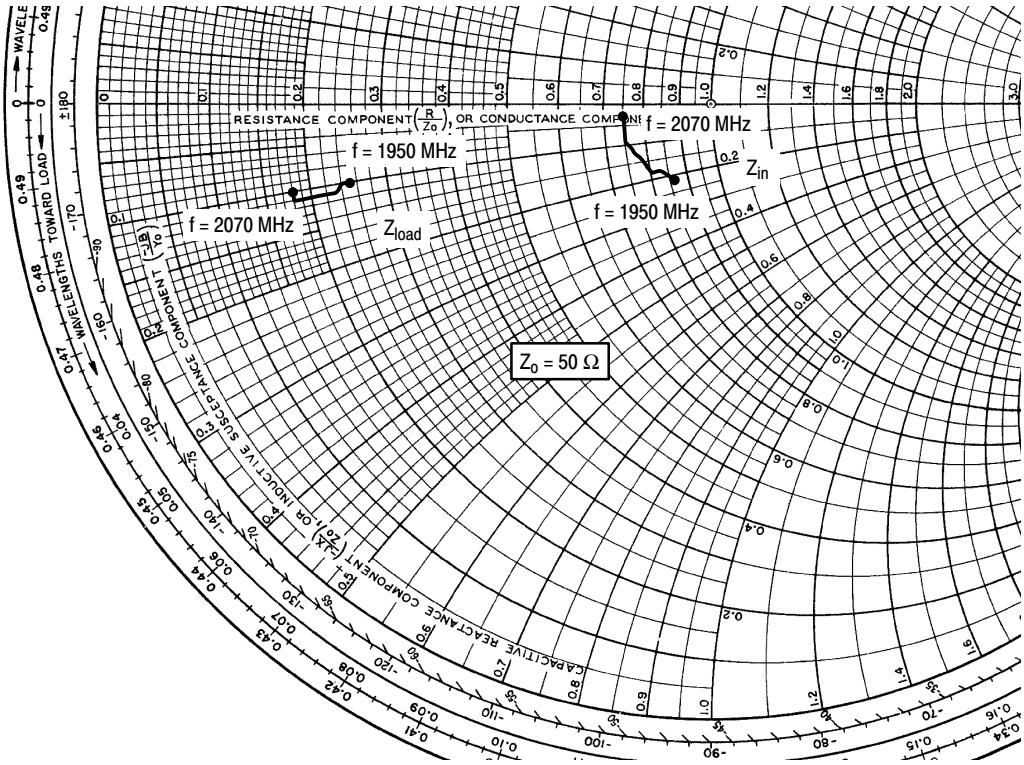


Figure 22. 6-Carrier TD-SCDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ1} = 280 mA, I_{DQ2} = 375 mA

f MHz	Z_{in} Ω	Z_{load} Ω
1950	42.975 - j10.510	12.419 - j4.771
1960	41.871 - j9.592	12.233 - j5.001
1970	40.898 - j9.050	11.983 - j5.104
1980	40.084 - j8.816	11.683 - j5.368
1990	39.463 - j7.496	11.334 - j5.499
2000	38.859 - j6.587	10.959 - j5.585
2010	38.434 - j6.117	10.578 - j5.631
2020	38.096 - j4.972	10.212 - j5.635
2030	37.748 - j4.486	9.877 - j5.596
2040	37.553 - j3.046	9.575 - j5.536
2050	37.414 - j2.586	9.302 - j5.439
2060	37.369 - j1.918	9.053 - j5.319
2070	37.420 - j1.654	8.831 - j5.185

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

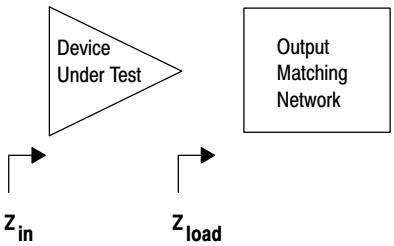
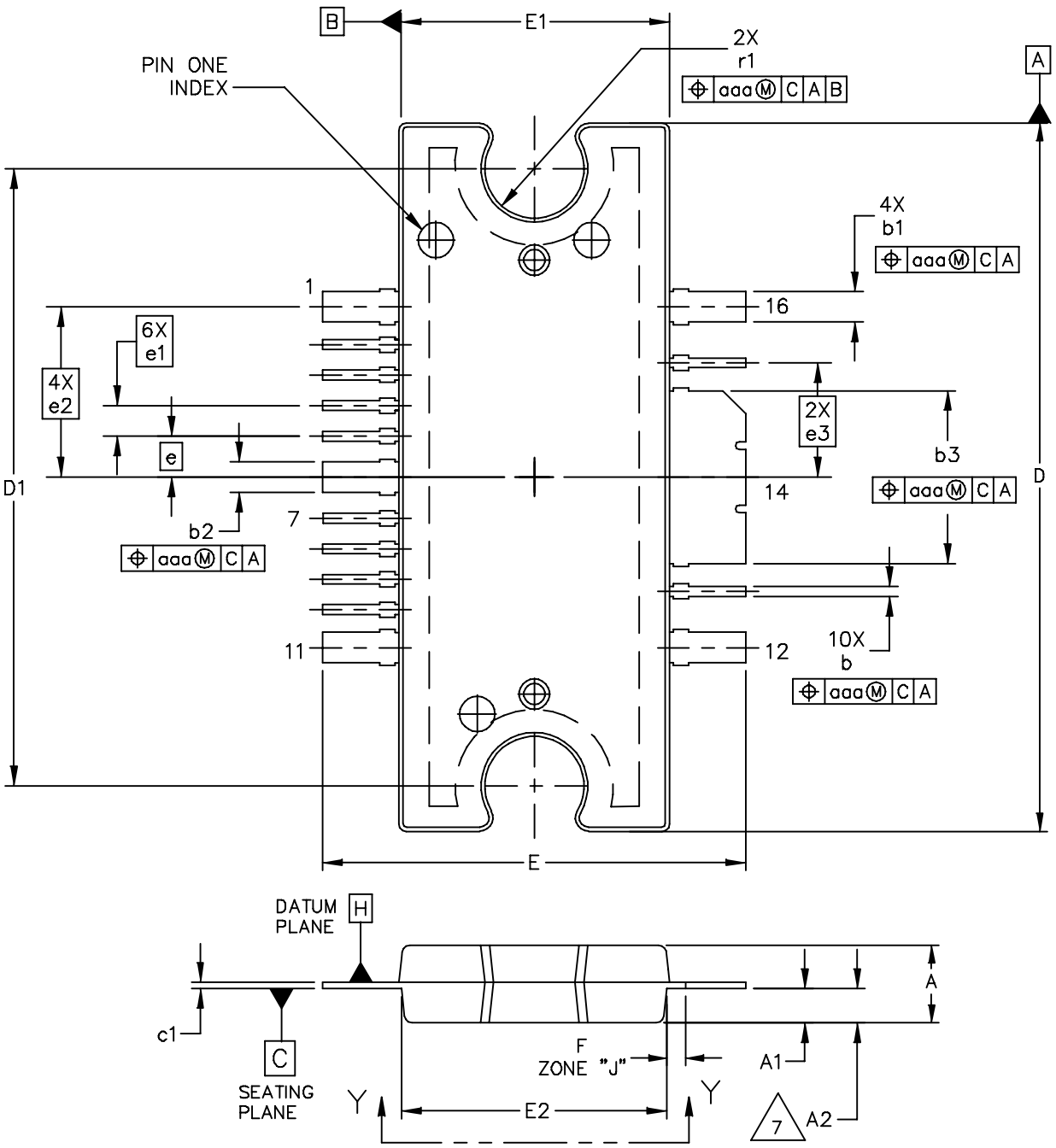


Figure 23. Series Equivalent Input and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS



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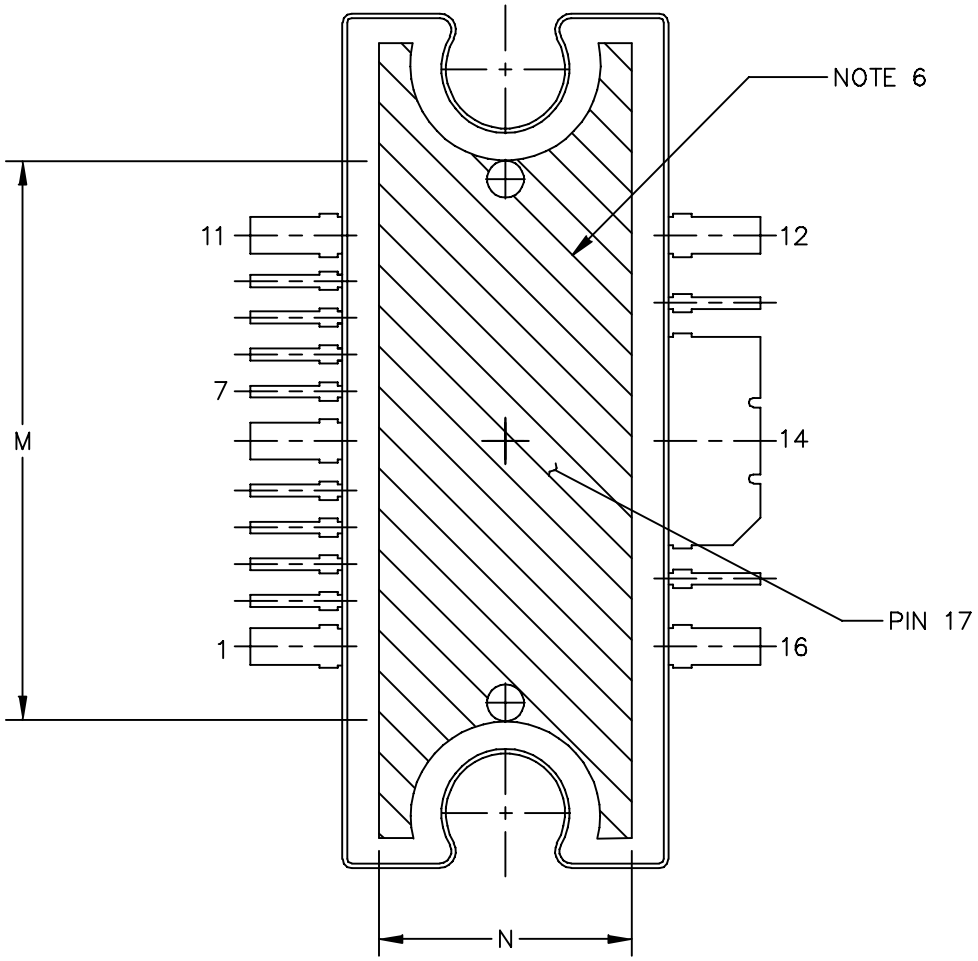

VIEW Y–Y

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	CASE NUMBER: 1329–09	23 AUG 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

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DOCUMENT NO: 98ARH99164A | REV: M

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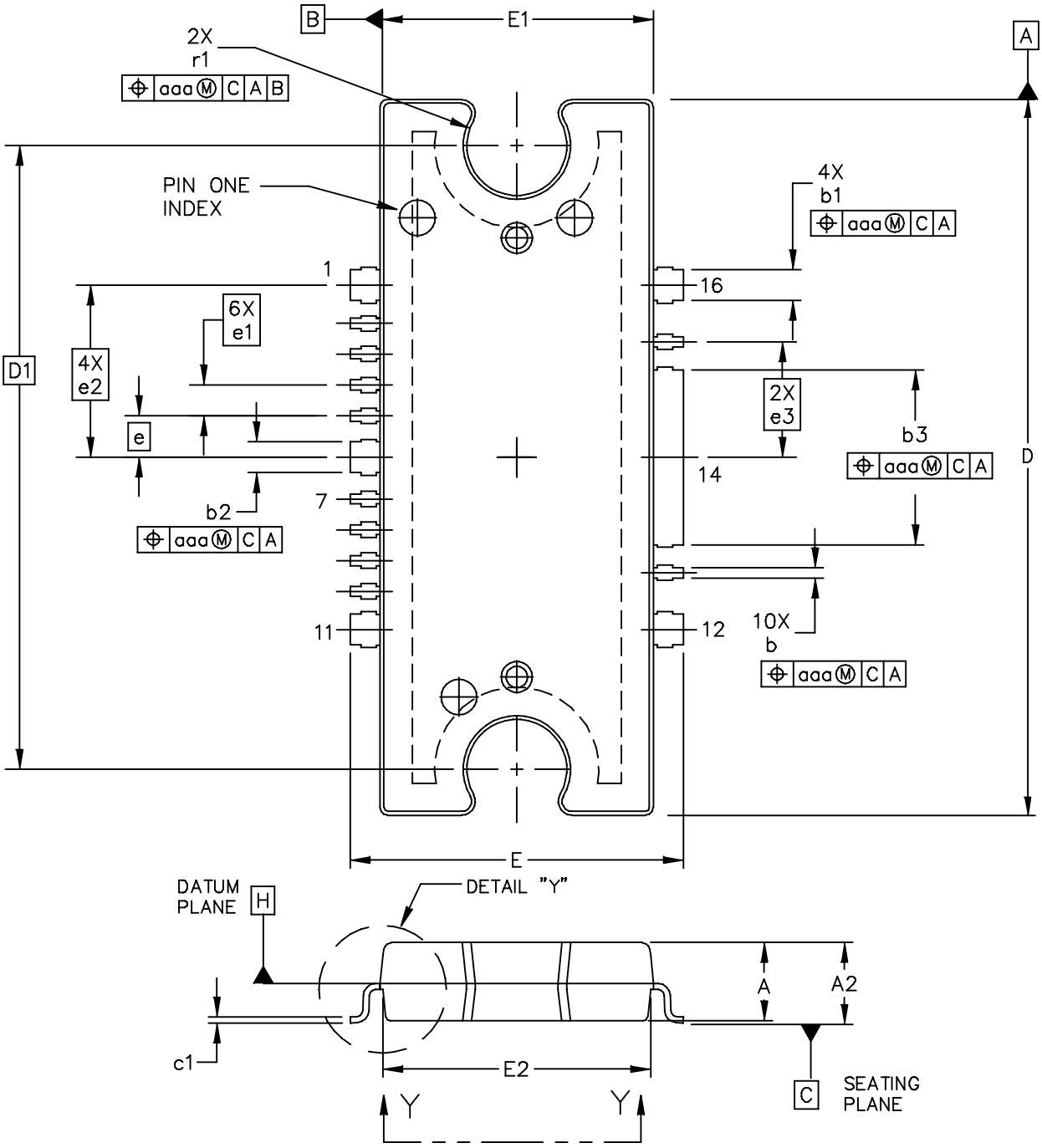
STANDARD: NON−JEDEC



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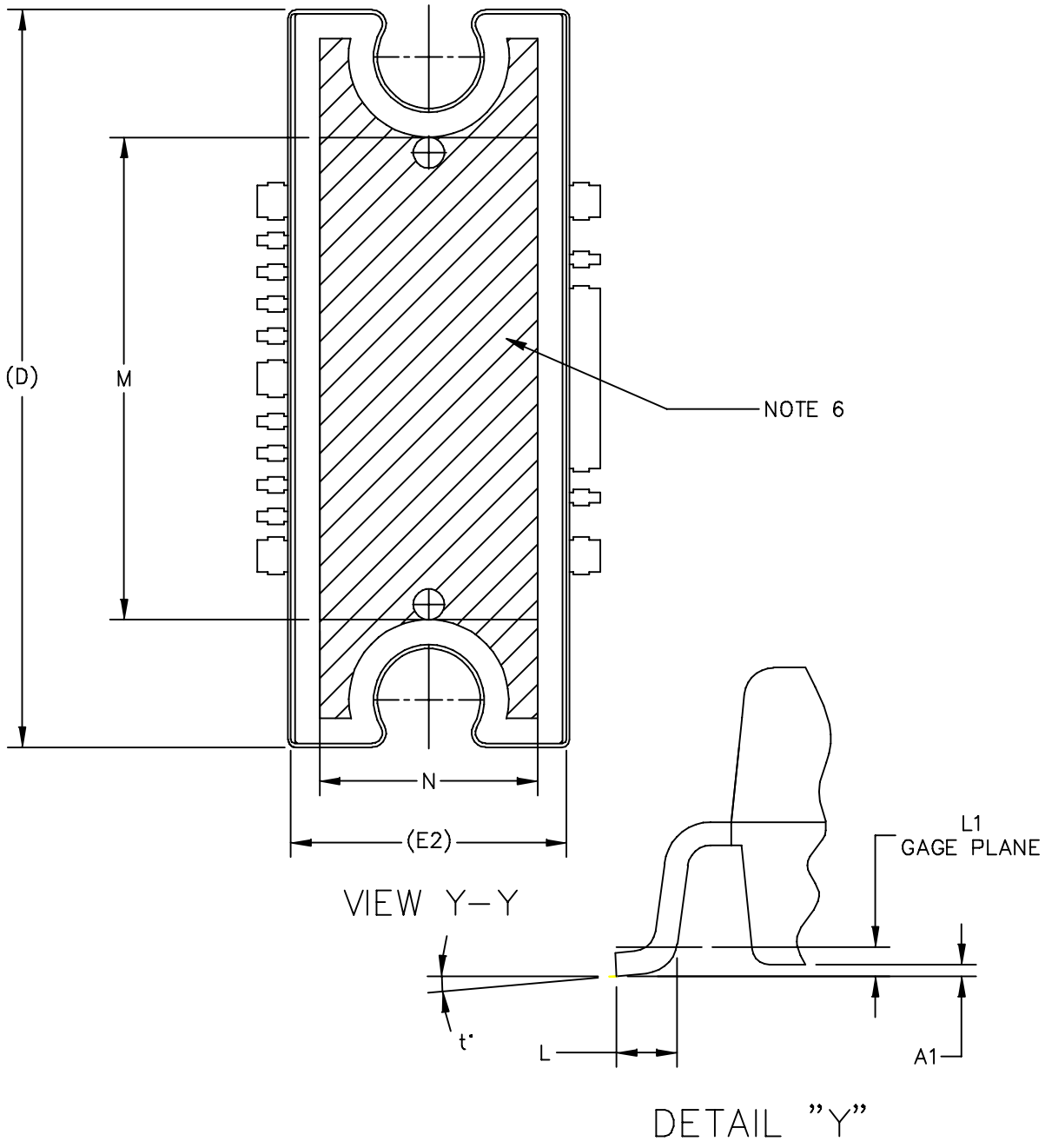
	CASE NUMBER: 1329A-04	20 JUN 2007
	STANDARD: JEDEC MO-253 BA	



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TITLE: TO–272WB, 16 LEAD GULL WING PLASTIC	DOCUMENT NO: 98ASA10532D	REV: F
	CASE NUMBER: 1329A–04	20 JUN 2007
	STANDARD: JEDEC MO–253 BA	

NOTES:

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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.001	.004	0.02	0.10	b1	.037	.043	0.94	1.09
A2	.099	.110	2.51	2.79	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
L	.018	.024	0.46	0.61	e3	.150 BSC		3.81 BSC	
L1	.01 BSC		0.25 BSC		r1	.063	.068	1.6	1.73
M	.600	----	15.24	----	t	2°	8°	2°	8°
N	.270	----	6.86	----					
					aaa	.004		.10	

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
3	Oct. 2006	• Added “including TD-SCDMA” to data sheet description, p. 1 • Added Part Number and Manufacturer to Resistors in Table 7, Component Designations and Values, p. 4 • Added TD-SCDMA test circuit schematic, component designations and values, component layout, typical characteristic curves, test signal and series impedance, p. 11-14 • Added Product Documentation and Revision History, p. 21
4	Dec. 2006	• Updated Part Numbers in Table 7, Component Designations and Values, to RoHS compliant part numbers, p. 4
5	Feb. 2007	• Corrected V_{BIAS} and V_{SUPPLY} callouts, Fig. 3, Test Circuit Schematic, p. 4, Fig. 4, Test Circuit Component Layout, p. 5 • Updated Part Numbers in Tables 7 and 9, Component Designations and Values, to latest RoHS compliant part numbers, p. 4, 11 • Removed lower voltage tests from Fig. 14, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 8 • Replaced Fig. 15, MTTF versus Junction Temperature with updated graph. Removed $Amps^2$ and listed operating characteristics and location of MTTF calculator for device, p. 8 • Changed callout η_D to PAE (Power Added Efficiency) for Figs. 19 and 20, 3-Carrier and 6-Carrier TD-SCDMA ACPR, ALT and Power Added Efficiency versus Output Power, p. 13 • Corrected Z_{in} data and plot in Fig. 23, Series Impedance, p. 14
6	Dec. 2008	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2 • Changed 220°C to 225°C in Capable Plastic Package bullet, p. 1 • Added Footnote 1 to Quiescent Current Temperature bullet under Features section and to callout in Figure 1, Functional Block Diagram, p. 1 • Changed Storage Temperature Range in Max Ratings table from -65 to +200 to -65 to +150 for standardization across products, p. 2 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 2 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table and related “Continuous use at maximum temperature will affect MTTF” footnote added, p. 2 • Updated Part Numbers in Table 7, Component Designations and Values, to latest RoHS compliant part numbers, p. 4

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