

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)} (\Omega)_{max}$	$I_D (A)_{max}$ $T_A = +25^\circ C$
Q1	100V	0.230 @ $V_{GS} = 10V$	2.1
		0.300 @ $V_{GS} = 4.5V$	1.9
Q2	-100V	0.235 @ $V_{GS} = -10V$	-2.2
		0.320 @ $V_{GS} = -4.5V$	-1.9

Description

This new generation complementary dual MOSFET features low on-resistance achievable with low gate drive.

Applications

- DC Motor Control
- Backlighting

Features

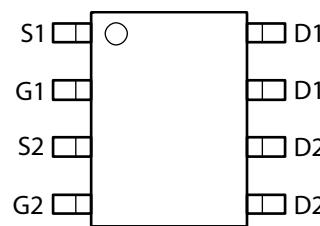
- 100V Complementary in SOIC package
- Low On-Resistance
- Fast Switching Speed
- Low Voltage ($V_{GS} = 4.5V$) gate drive
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

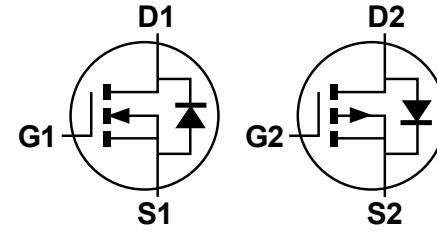
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (approximate)



Top View



Top View



Q1 N-Channel

Q2 P-Channel

Equivalent Circuit

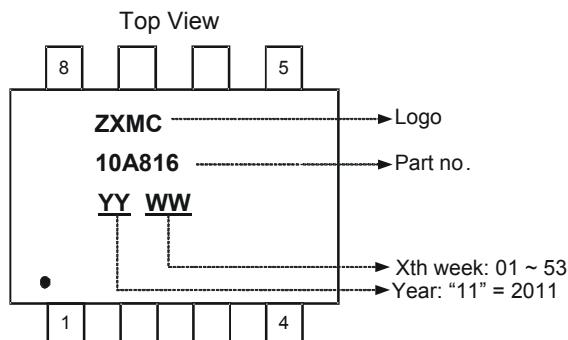
Ordering Information (Note 4)

Product	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC10A816N8	13	12	2,500

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source Voltage	V_{DSS}	100	-100	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current @ $V_{GS} = 10\text{V}$; $T_A = +25^\circ\text{C}$ @ $V_{GS} = 10\text{V}$; $T_A = +70^\circ\text{C}$ @ $V_{GS} = 10\text{V}$; $T_A = +25^\circ\text{C}$ @ $V_{GS} = 10\text{V}$; $T_A = +25^\circ\text{C}$ @ $V_{GS} = 10\text{V}$; $T_L = +25^\circ\text{C}$	I_D	2.1	-2.2	
		1.7	-1.8	
		1.7	-1.7	
		2.0	-2.0	
		2.3	-2.4	A
Pulsed Drain Current @ $V_{GS} = 10\text{V}$; $T_A = +25^\circ\text{C}$	I_{DM}	9.4	-10.5	A
Continuous Source Current (Body Diode) at $T_A = +25^\circ\text{C}$	I_S	3.0	-3.1	A
Pulsed Source Current (Body Diode) at $T_A = +25^\circ\text{C}$	I_{SM}	9.4	-10.5	A
Avalanche Current (g) $L = 0.1\text{ mH}$	I_{AS}	1.2	12	A
Power Dissipation at $T_A = +25^\circ\text{C}$	P_D	1.3 10.0		W mW/°C
Linear Derating Factor				
Power Dissipation at $T_A = +25^\circ\text{C}$	P_D	1.8 14.2		W mW/°C
Linear Derating Factor				
Power Dissipation at $T_A = +25^\circ\text{C}$	P_D	2.1 16.7		W mW/°C
Linear Derating Factor				
Power Dissipation at $T_L = +25^\circ\text{C}$	P_D	2.4 18.9	2.6 20.4	W mW/°C
Linear Derating Factor				
Operating and Storage Temperature Range	T_j, T_{stg}	-55 to +150		°C

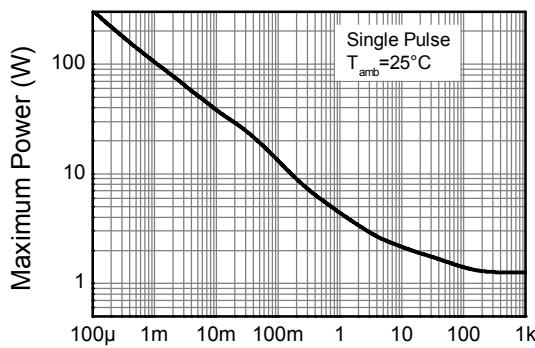
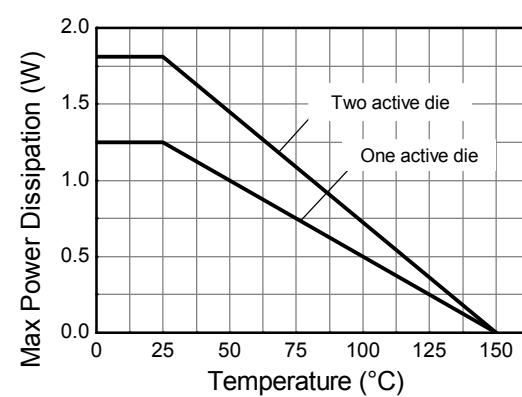
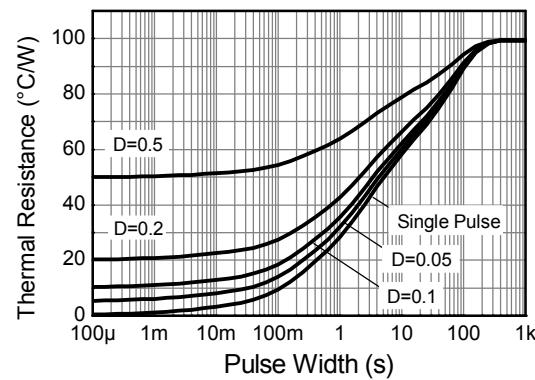
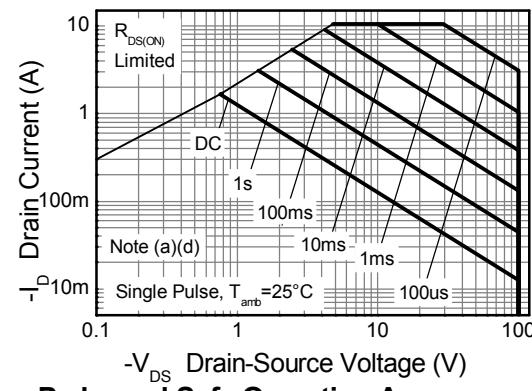
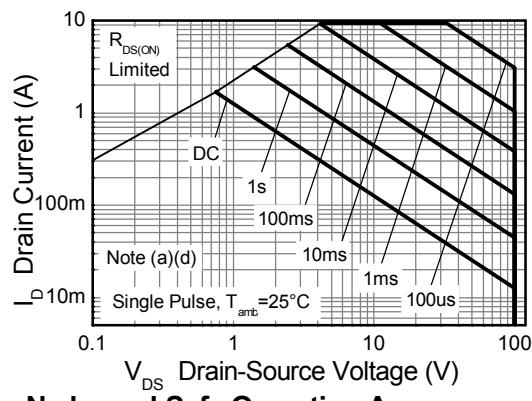
Thermal Characteristics

Parameter	Symbol	Value		Unit
Junction to Ambient ^{(a)(d)}	$R_{\theta JA}$	100		°C/W
Junction to Ambient ^{(a)(e)}	$R_{\theta JA}$	70		°C/W
Junction to Ambient ^{(b)(d)}	$R_{\theta JA}$	60		°C/W
Junction to Lead ^{(f)(d)}	$R_{\theta JL}$	53	49	°C/W

Notes:

- (a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
- (b) Same as note (a), except the device is measured at $t \leq 10$ sec.
- (c) Same as note (a), except the device is pulsed with $D = 0.02$ and pulse width 300μs. The pulse current is limited by the maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead); the device is operating in a steady-state condition.
- (g) IAS rating are based on low frequency and duty cycles to keep $T_j = +25^\circ\text{C}$.

Thermal Characteristics

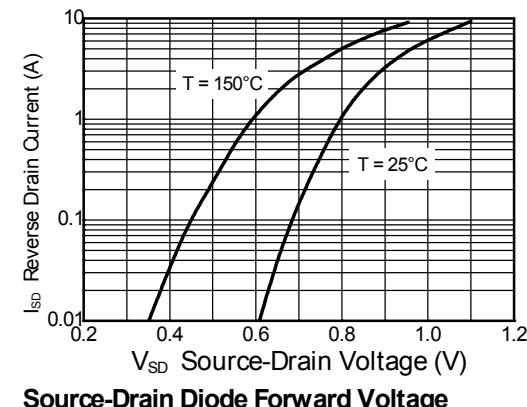
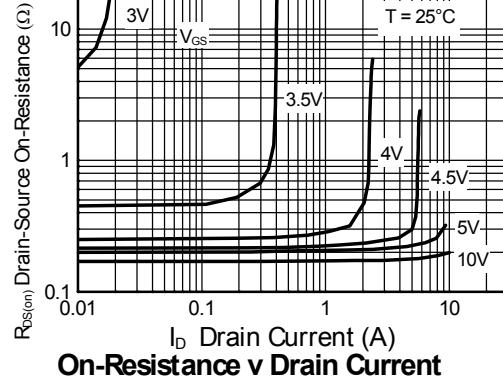
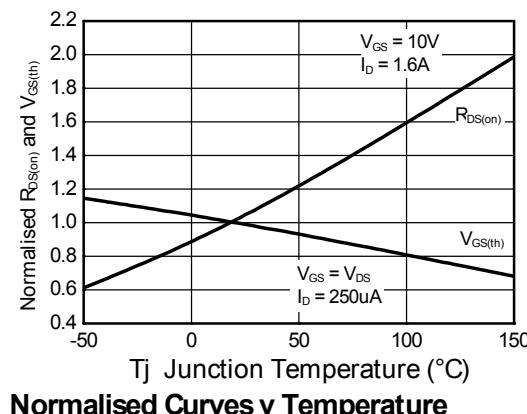
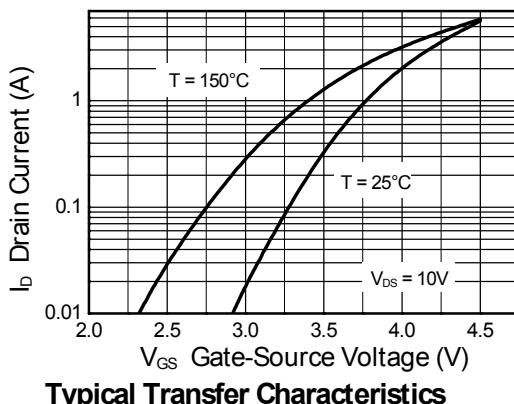
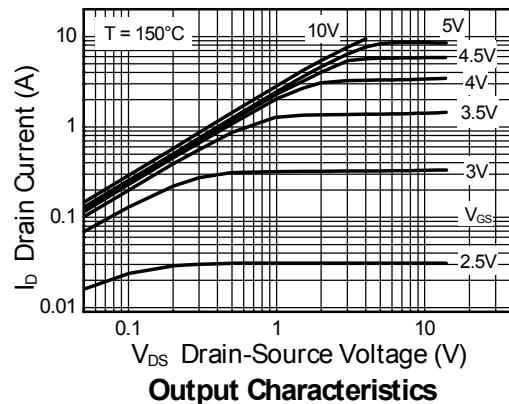
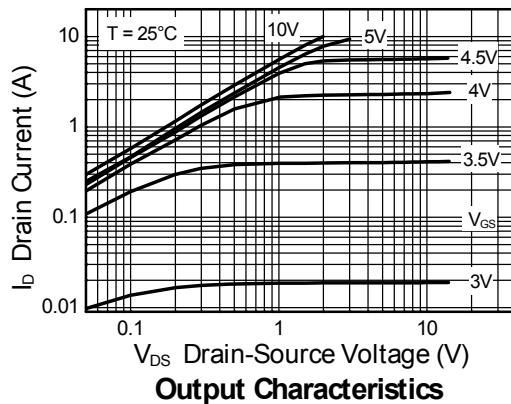


Electrical Characteristics Q1 N-Channel (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

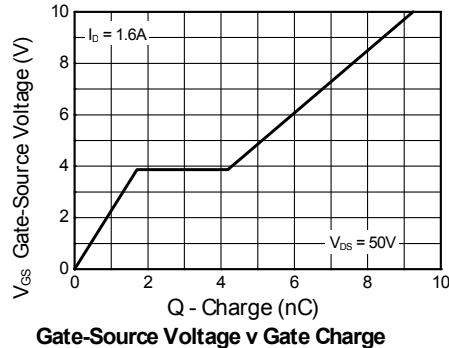
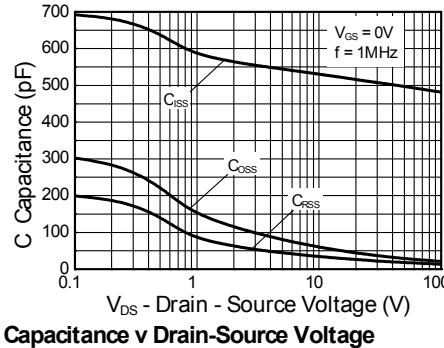
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	100	—	—	V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	0.5	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body Leakage	I_{GSS}	—	—	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	1.7	—	2.4	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source On-State Resistance ^(a)	$R_{\text{DS}(\text{ON})}$	—	0.170 0.210	0.230 0.300	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.0\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 0.5\text{A}$
Forward Transconductance ^{(a) (c)}	g_{fs}	—	4.8	—	S	$V_{DS} = 15\text{V}$, $I_D = 1.6\text{A}$
Dynamic Capacitance ^(c)						
Input Capacitance	C_{iss}	—	497	—	pF	$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}	—	29	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	18	—	pF	
Switching ^{(b) (c)}						
Turn-On-Delay Time	$t_{\text{d}(\text{ON})}$	—	2.9	—	ns	$V_{DD} = 50\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1.0\text{A}$ $R_G \geq 6.0\Omega$,
Rise Time	t_r	—	2.1	—	ns	
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$	—	12.1	—	ns	
Fall Time	t_f	—	5.0	—	ns	
Gate Charge ^(c)						
Total Gate Charge	Q_g	—	9.2	—	nC	$V_{DS} = 50\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 1.6\text{A}$
Gate-Source Charge	Q_{gs}	—	1.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	2.5	—	nC	
Source-Drain Diode						
Diode Forward Voltage ^(a)	V_{SD}	—	0.85	0.95	V	$I_S = 1.7\text{A}$, $V_{GS} = 0\text{V}$
Reverse Recovery Time ^(c)	t_{rr}	—	32	—	ns	$I_S = 1.7\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge ^(c)	Q_{rr}	—	40	—	nC	
Gate Resistance						
Gate Resistance	R_G	0	—	3	Ω	$V_{DS} = 0\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$

Notes: (a) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing.

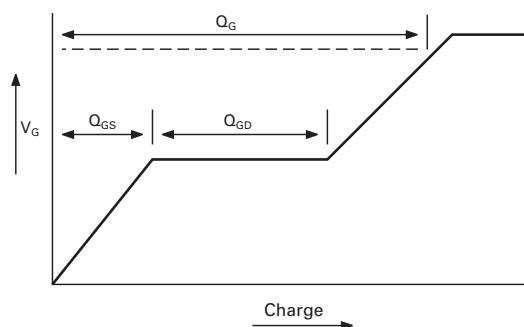
Typical Characteristics Q1 N-Channel



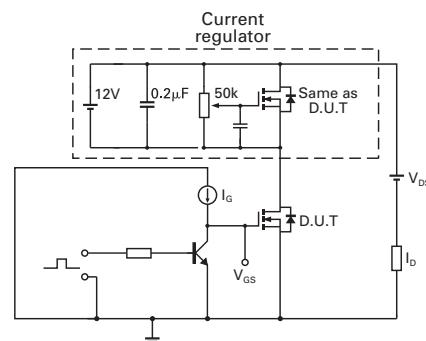
Typical Characteristics Q1 N-Channel (cont.)



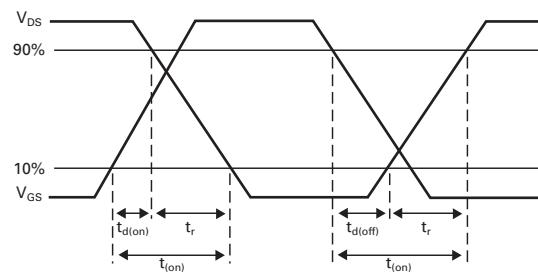
Test Circuits



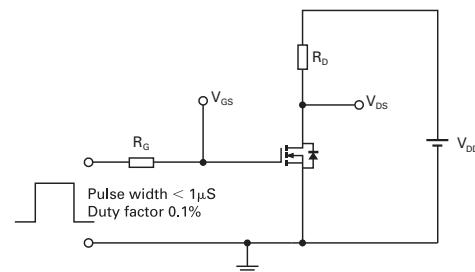
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



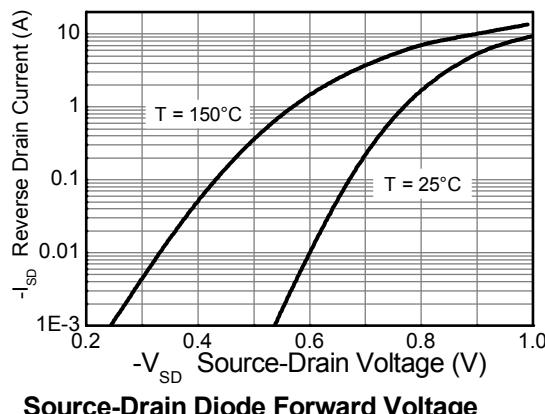
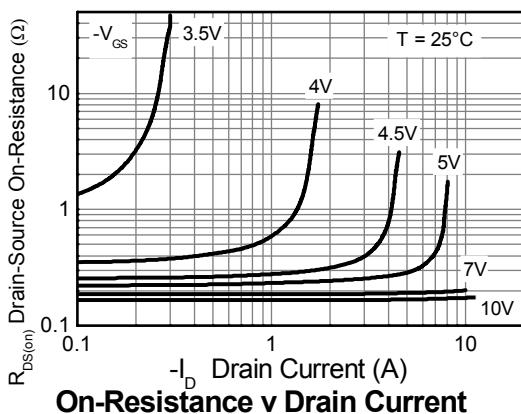
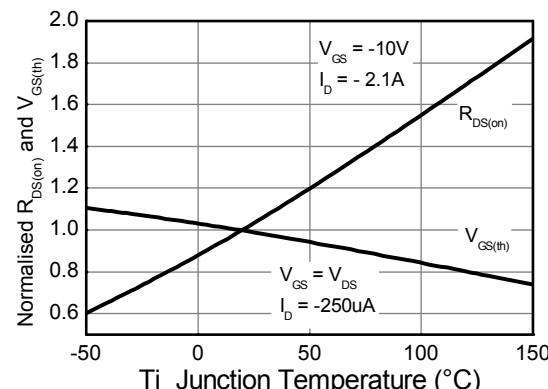
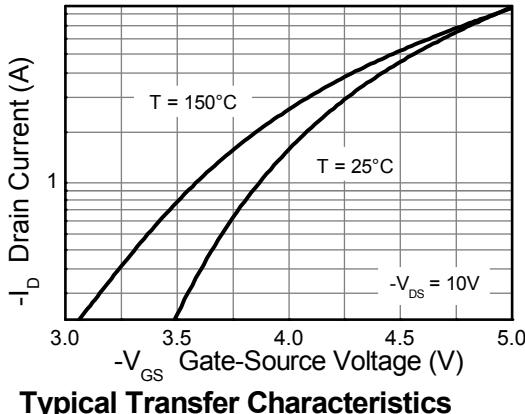
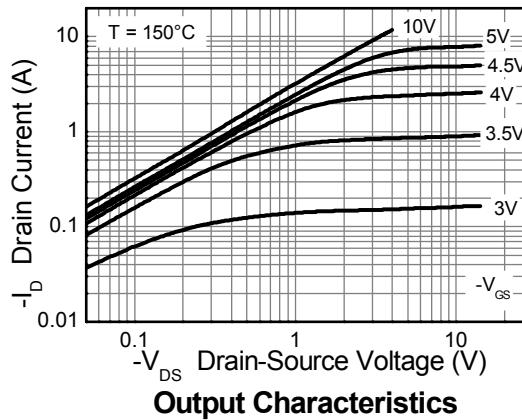
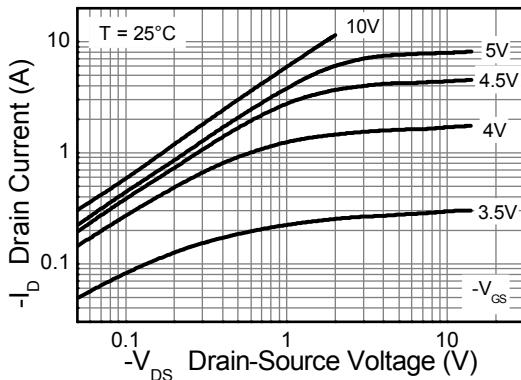
Switching time test circuit

Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

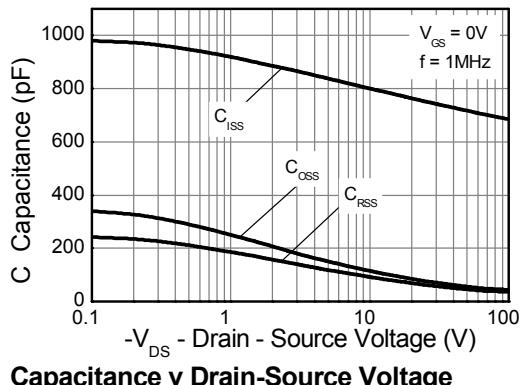
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	-100	—	—	V	I _D = -250µA, V _{GS} = 0V
Zero Gate Voltage Drain current	I _{DSS}	—	—	-0.5	µA	V _{DS} = -100V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	100	nA	V _{GS} = ±20V, V _{DS} = 0V
Gate-Source Threshold Voltage	V _{GS(th)}	-2.0	—	-3.0	V	I _D = -250µA, V _{DS} = V _{GS}
Static Drain-Source On-State Resistance ^(a)	R _{DSS(ON)}	—	0.170 0.250	0.235 0.320	Ω	V _{GS} = -10V, I _D = -1.0A V _{GS} = -4.5V, I _D = -0.5A
Forward Transconductance ^{(a) (c)}	g _{fs}	—	4.7	—	S	V _{DS} = -15V, I _D = -2.1A
Dynamic Capacitance ^(c)						
Input Capacitance	C _{iss}	—	717	—	pF	V _{DS} = -50V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	55	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	46	—	pF	
Switching ^{(b) (c)}						
Turn-On-Delay Time	t _{d(ON)}	—	4.3	—	ns	V _{DD} = -50V, V _{GS} = -10V I _D = -1A R _G ≥ 6.0Ω,
Rise Time	t _r	—	5.2	—	ns	
Turn-Off Delay Time	t _{d(OFF)}	—	20	—	ns	
Fall Time	t _f	—	12	—	ns	
Gate Charge ^(c)						
Total Gate Charge	Q _g	—	16.5	—	nC	V _{DS} = -50V, V _{GS} = -10V I _D = -2.1A
Gate-Source Charge	Q _{gs}	—	2.5	—	nC	
Gate-Drain Charge	Q _{gd}	—	5.4	—	nC	
Source-Drain Diode						
Diode Forward Voltage ^(a)	V _{SD}	—	-0.85	-0.95	V	I _S = -1.7A, V _{GS} = 0V
Reverse Recovery Time ^(c)	t _{rr}	—	43	—	ns	I _S = -1.7A, di/dt = 100A/µs
Reverse Recovery Charge ^(c)	Q _{rr}	—	77	—	nC	
Gate Resistance						
Gate Resistance	R _G	0	—	100	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz

Notes: (a) Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
 (b) Switching characteristics are independent of operating junction temperature.
 (c) For design aid only, not subject to production testing.

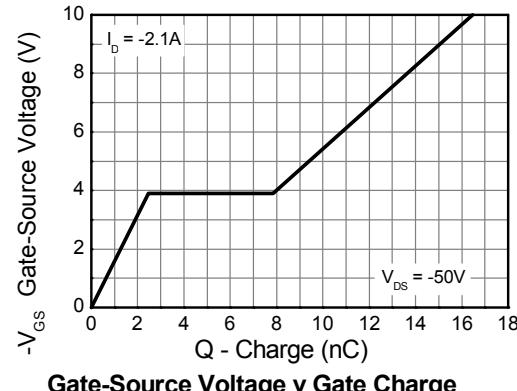
Typical Characteristics Q2 P-Channel



Typical Characteristics Q2 P-Channel (cont.)

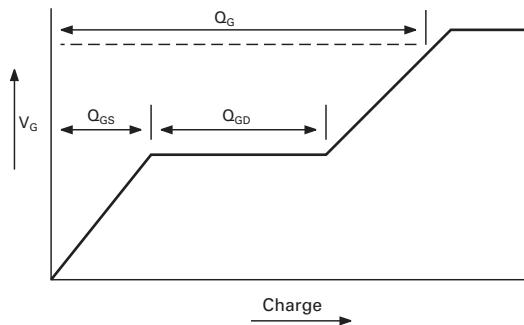


Capacitance v Drain-Source Voltage

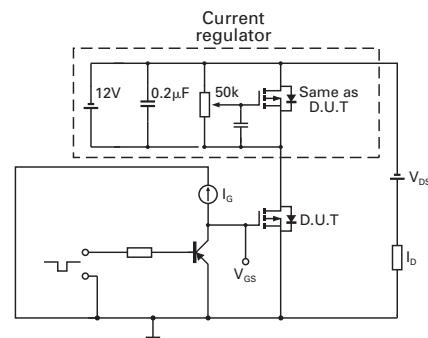


Gate-Source Voltage v Gate Charge

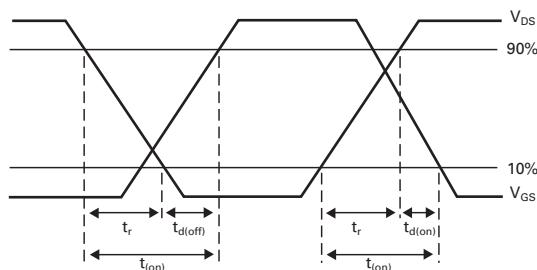
Test Circuits



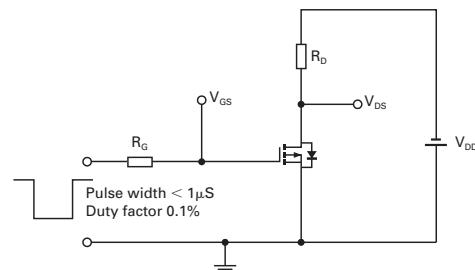
Basic gate charge waveform



Gate charge test circuit



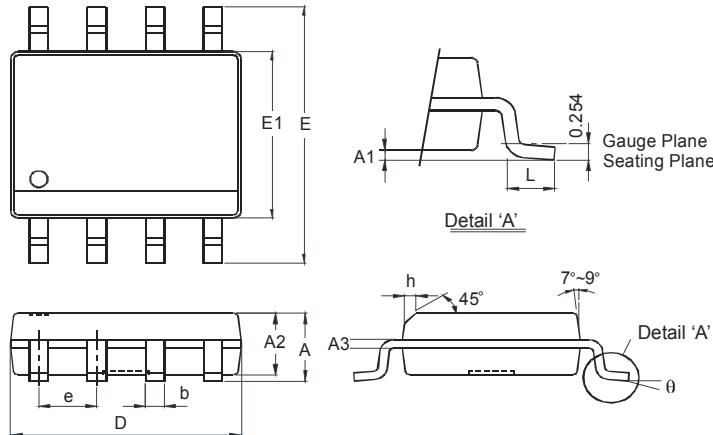
Switching time waveforms



Switching time test circuit

Package Outline Dimensions

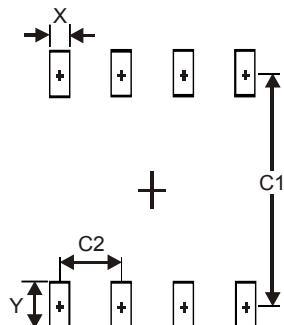
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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