

**LOGIC LEVEL
HEXFET® POWER MOSFET
SURFACE MOUNT (SMD-0.5)**

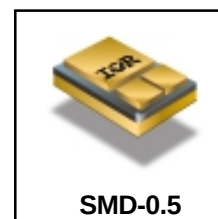
**IRL5NJ024
55V, N-CHANNEL**

Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRL5NJ024	55V	0.06Ω	17A

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.



SMD-0.5

Features:

- Logic Level Gate Drive
- Low R_{DS(on)}
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I _D @ V _{GS} = 10V, T _C = 25°C	Continuous Drain Current	17	A
I _D @ V _{GS} = 10V, T _C = 100°C	Continuous Drain Current	11	
I _{DM}	Pulsed Drain Current ①	68	
P _D @ T _C = 25°C	Max. Power Dissipation	35	W
	Linear Derating Factor	0.28	W/°C
V _{GS}	Gate-to-Source Voltage	±16	V
E _{AS}	Single Pulse Avalanche Energy ②	56	mJ
I _{AR}	Avalanche Current ①	11	A
E _{AR}	Repetitive Avalanche Energy ①	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.3	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Package Mounting Surface Temperature	300 (for 5 s)	
	Weight	2.6	g

For footnotes refer to the last page

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.060	Ω	V _{GS} = 10V, I _D = 11A ④
		—	—	0.075		V _{GS} = 5.0V, I _D = 11A ④
		—	—	0.105		V _{GS} = 4.0V, I _D = 9.0A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	6.5	—	—	S	V _{DS} = 25V, I _D = 11 A
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 44V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
Q _g	Total Gate Charge	—	—	15	nC	I _D = 11A
Q _{gs}	Gate-to-Source Charge	—	—	3.7		V _{DS} = 44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.5		V _{GS} = 5.0V
t _{d(on)}	Turn-On Delay Time	—	—	11	ns	V _{DD} = 28V
t _r	Rise Time	—	—	133		I _D = 11A
t _{d(off)}	Turn-Off Delay Time	—	—	35		R _G = 12 Ω
t _f	Fall Time	—	—	66		V _{GS} = 5.0V
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	514	—	pF	V _{GS} = 0V, V _{DS} = 25V
C _{oss}	Output Capacitance	—	137	—		f = 1.0MHz
C _{rss}	Reverse Transfer Capacitance	—	51	—		

Source-Drain Diode Ratings and Characteristics

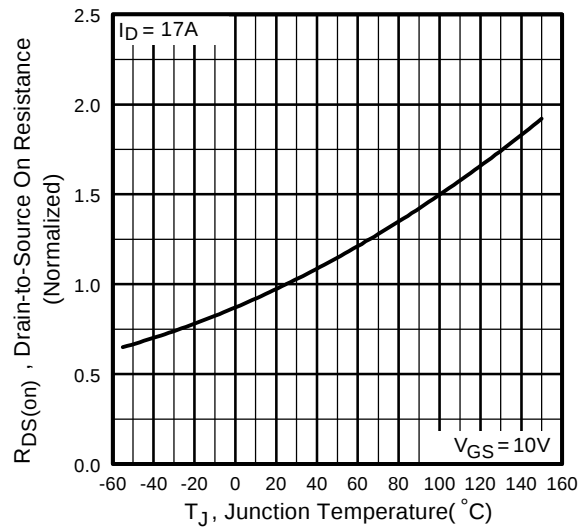
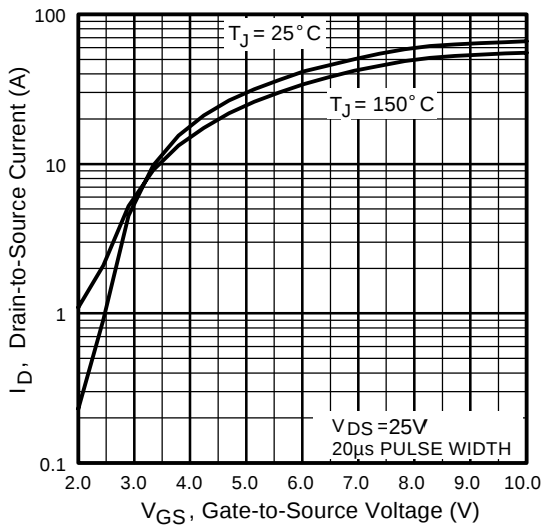
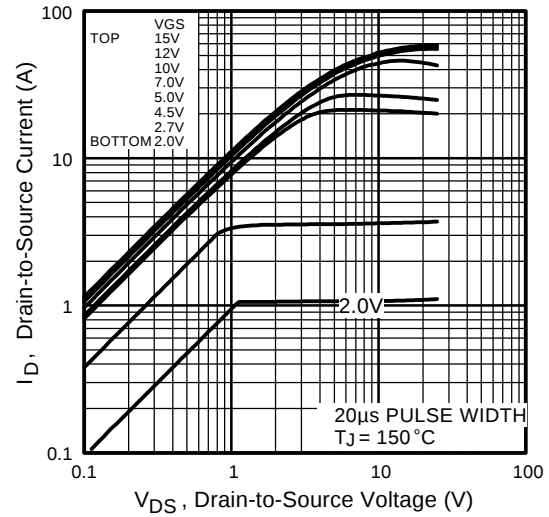
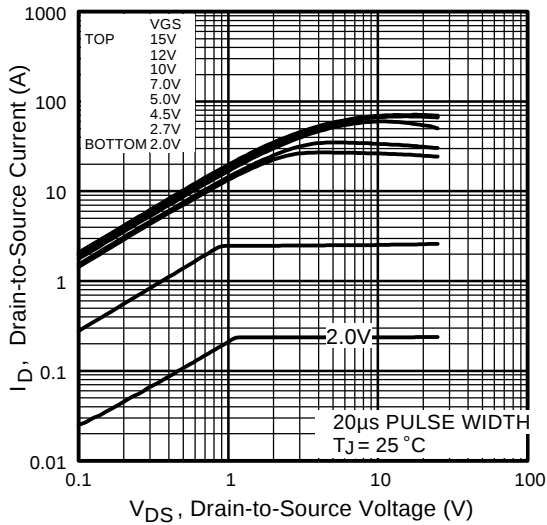
	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	17	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	68		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 11A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	90	nS	T _J = 25°C, I _F = 11A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	200	nC	V _{DD} ≤ 25V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	3.57	°C/W	

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page



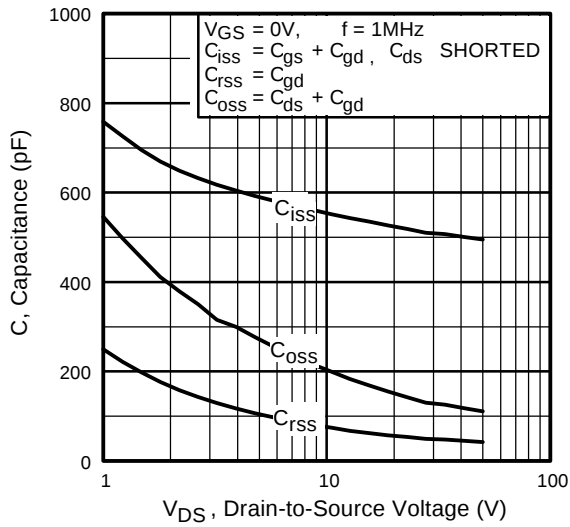


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

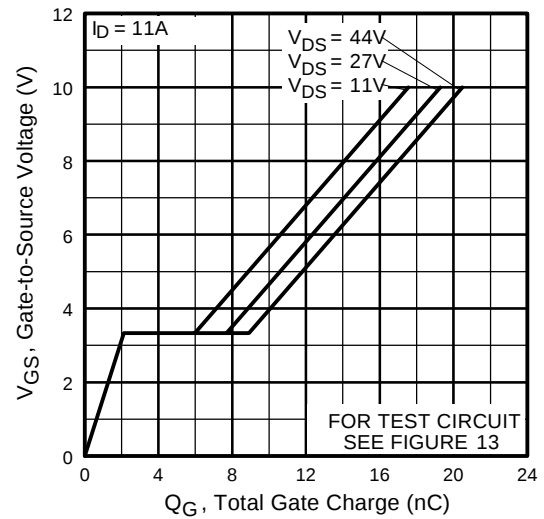


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

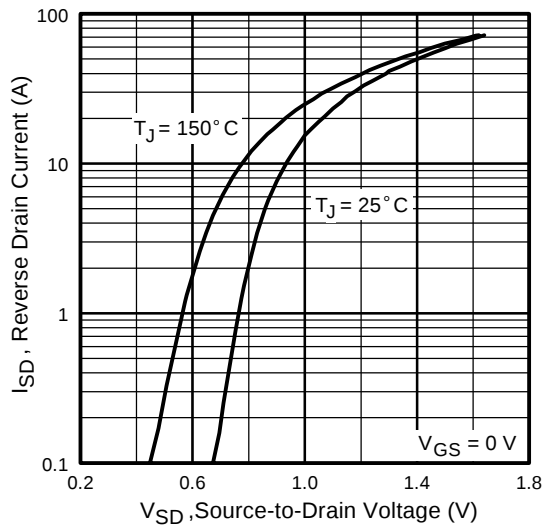


Fig 7. Typical Source-Drain Diode Forward Voltage

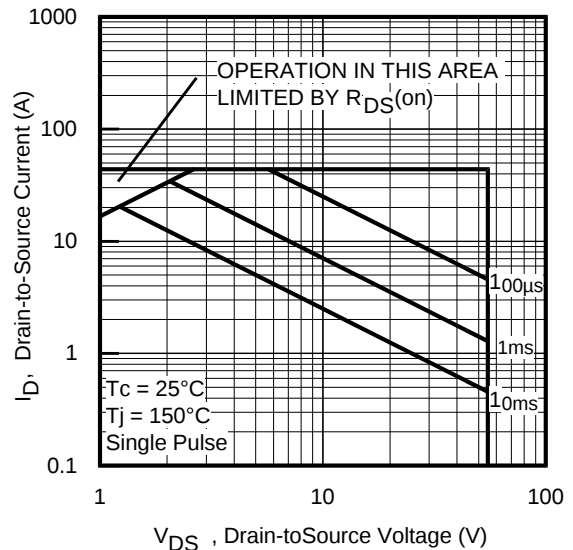


Fig 8. Maximum Safe Operating Area

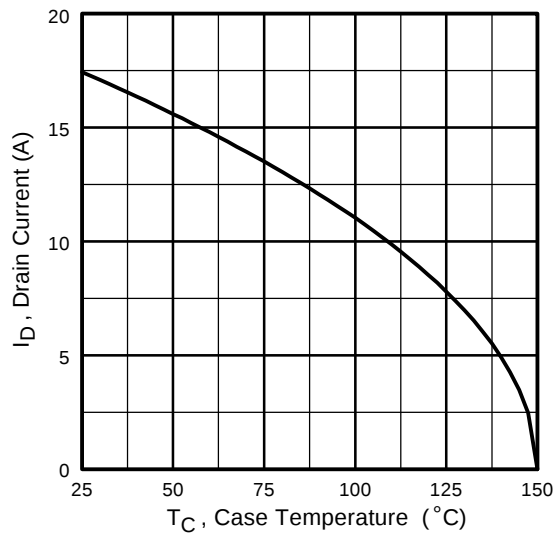


Fig 9. Maximum Drain Current Vs. Case Temperature

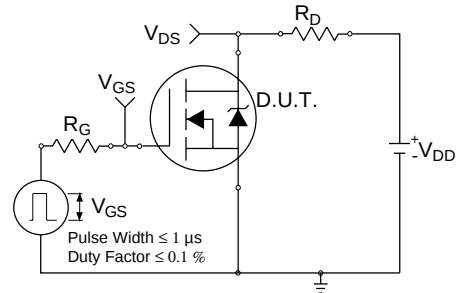


Fig 10a. Switching Time Test Circuit

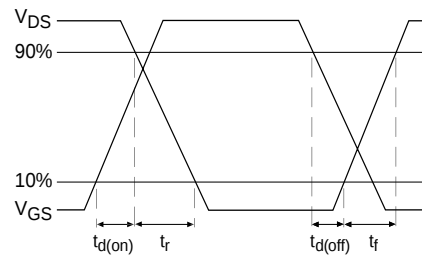


Fig 10b. Switching Time Waveforms

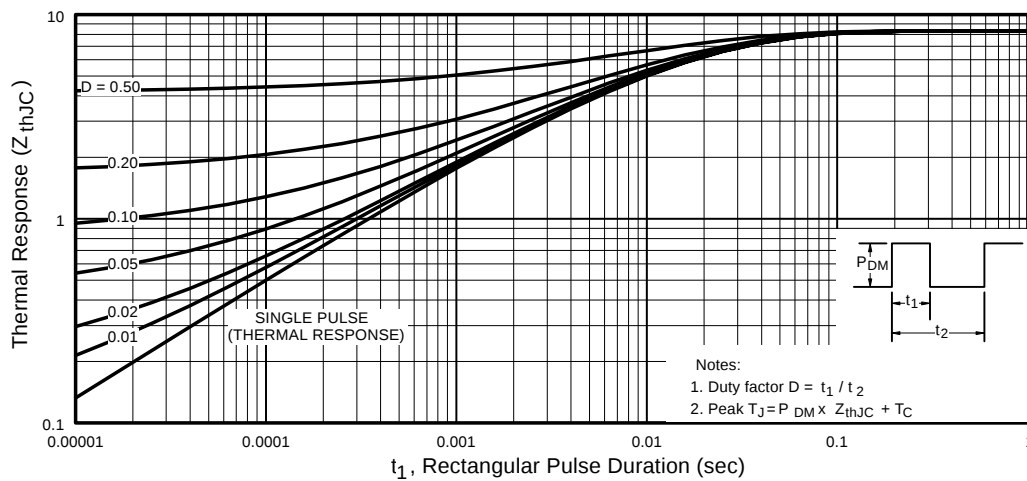


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

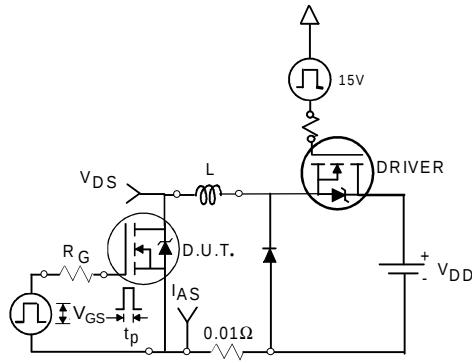


Fig 12a. Unclamped Inductive Test Circuit

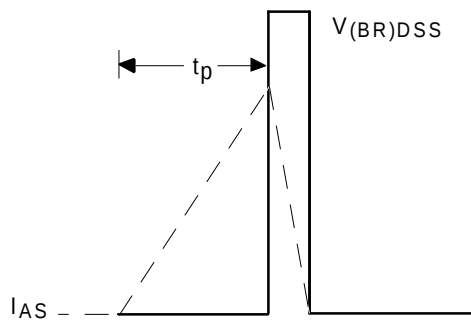


Fig 12b. Unclamped Inductive Waveforms

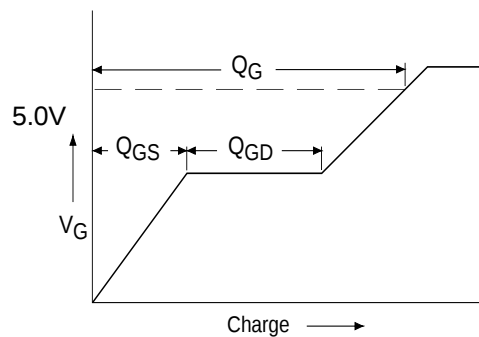


Fig 13a. Basic Gate Charge Waveform

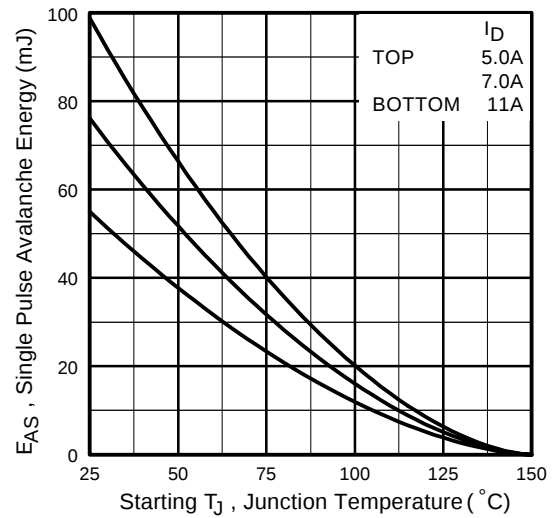


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

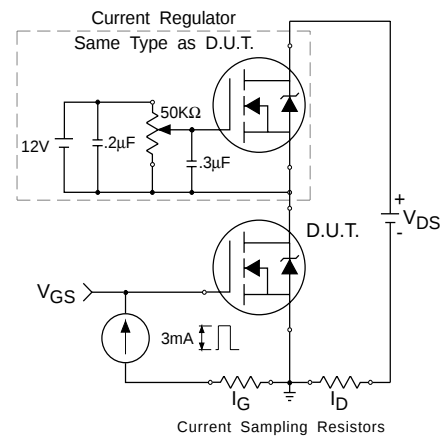
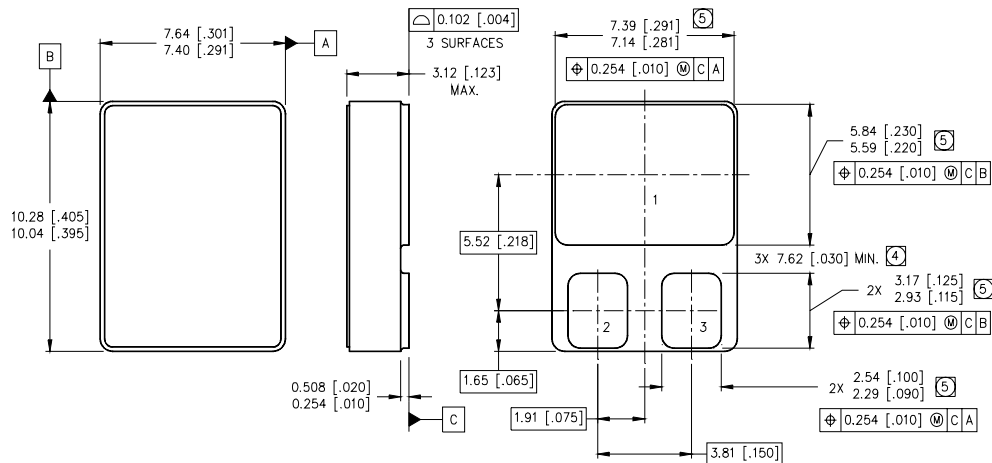


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25\text{ V}$, Starting $T_J = 25^\circ\text{C}$, $L=0.9\text{mH}$
Peak $I_{AS} = 11\text{A}$, $V_{GS} = 5.0\text{ V}$, $R_G = 25\Omega$
- ③ $I_{SD} \leq 11\text{A}$, $di/dt \leq 230\text{ A}/\mu\text{s}$,
 $V_{DD} \leq 55\text{V}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\text{ }\mu\text{s}$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — SMD-0.5



NOTES:

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE