

# IP4305CX4/LF (/P)

Integrated dual Schottky diode array with ESD protection to  
IEC61000-4-2, level 4

20 August 2009

Product data sheet

## 1. Product profile

### 1.1 General description

IP4305CX4/LF (/P) is a dual Schottky diode – one back-2-back diode array in a 2 x 2 pin CSP with 0.4 mm pitch. In addition to two Schottky diodes with a common Cathode connection, a integrated bi-directional diode supports the realisation of a high level ESD-protection. IP4305CX4/LF (/P) is fabricated using monolithic silicon technology and integrates Schottky and standard silicon Zener diodes in a single *Wafer-Level* chip-scale package. These features make the IP4305CX4/LF (/P) ideal for use in applications requiring component miniaturization, such as mobile phone handsets. For mechanically demanding applications the option /P as IP4305CX4/LF/P is offering improved mechanical stability by using advanced solder joints.

### 1.2 Features

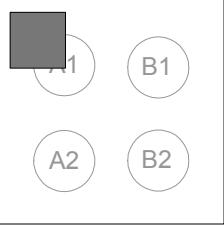
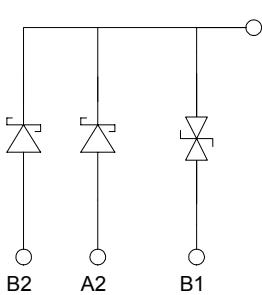
- Pb-free, RoHS compliant and free of Halogen and Antimony (dark green compliant)
- 2 Schottky diodes with common Cathode
- One back-to-back diode
- Back to back diodes to provide downstream ESD protection up to  $\pm 15$  kV (contact)
- Wafer-Level chip-scale package with 0.4 mm pitch only

### 1.3 Applications

General purpose ESD-protection and voltage detection in mobile appliances such as:

- Cellular and PCS mobile handsets
- Wireless data (WAN/LAN) systems

## 2. Pinning Information

	 <p>Fig 2. IP4305CX4/LF (/P) schematic diagram</p>
<p>Fig 1. Transparent package view, balls facing down</p>	

### 3. Limiting values

Table 1. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	DC input voltage range for A1 to A2, B2		0	+5.5	V
$V_{I/O}$	DC input voltage range for A1 to B1		-5.5	+5.5	V
ESD	Electrostatic Discharge				
	Pins A1 to B1 (B2, A2 connected to an 2kV compliant IC I/O)	IEC 61000-4-2, Level 4			
		Contact	-8 (-15) <sup>1</sup>	+8 (+15) <sup>1</sup>	kV
		Air Discharge	-15	+15	kV
	Pins to B2, A2 to A1 or B1 <sup>(2)</sup> or A1 to A2 or B2 with B1 unconnected	IEC 61000-4-2, Level 1			
		Contact & Air Discharge	-2	+2	kV
$P_{D-ch}$	Maximum continuous power dissipation per channel	@ 70°C		5	mW
$T_{stg}$	storage temperature range		-55	+150	°C
$T_{pk}$	Peak solder reflow temperature	10 seconds max.		+260	°C
$T_{amb}$	Ambient operating temperature		-30	+85	°C

### 4. Electrical Characteristics

Table 2. Characteristics

 $T_{amb} = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{jo-Schottky}$	Schottky diode junction capacitance	$V = 0$ V; $f = 1$ MHz	-	19	-	pF
$C_{jo-Si}$	Back-to-back diode junction capacitance	$V = 0$ V; $f = 1$ MHz	-	7	-	pF
$V_{BR-Si}$	Back-to-back diode breakdown voltage	$I_{test} = +1$ mA	5.5	-	10	V
		$I_{test} = -1$ mA	-10	-	-5.5	V
$V_{BR-Schottky}$	Schottky diode breakdown voltage	$I_{test} = +1$ mA	15	-	-	V
$V_{Schottky}$	Schottky diode forward voltage	$I_{test} = +10$ $\mu$ A	-	-	0.25	V
		$I_{test} = +100$ $\mu$ A	-	-	0.35	V
		$I_{test} = +10$ mA	-	-	0.45	V
$I_{Ikg-Si}$	Back-to-back diode leakage current	$V = +3$ V	-	-	+50	nA
		$V = -3$ V	-50	-	-	nA
$I_{Ikg-Schottky}$	Schottky diode leakage current	$V = +5$ V, $T_{amb} = +25$ °C	-	-	1	$\mu$ A
		$V = +5$ V, $T_{amb} = +50$ °C	-	-	8	$\mu$ A
		$V = +5$ V, $T_{amb} = +85$ °C	-	-	80	$\mu$ A

<sup>1</sup> Device is tested with 1000 pulses of  $\pm 15$  kV contact discharges each, according the IEC61000-4-2 model<sup>2</sup> The two Schottky diodes are **neither** build for ESD protection **nor** to survive ESD discharges when connected directly to GND.

## 5. Design/Assembly Recommendations

### 5.1 PCB Design Guidelines

For the optimum performance, a Non-Solder Mask PCB design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer is recommended. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, the following are the recommended PCB design parameters:

- PCB pad size: 0.20 mm diameter
- Micro-Via diameter: 0.1 mm (0.004")
- Solder Mask opening: 0.37 mm diameter
- Copper thickness: 20-40  $\mu$ m
- Copper finish: AuNi
- PCB material: FR4

### 5.2 PCB Assembly Guidelines for Pb-free soldering

The following are recommendations for the assembly of this device:

- Solder Screen Aperture size: 0.33 mm diameter
- Solder Screen thickness: 100  $\mu$ m (0.004")
- Solder Paste: Pb-free: Sn Ag(3-4) Cu(0.5-0.9)
- Solder/Flux ratio: 50 / 50
- Solder Reflow Profile: see below

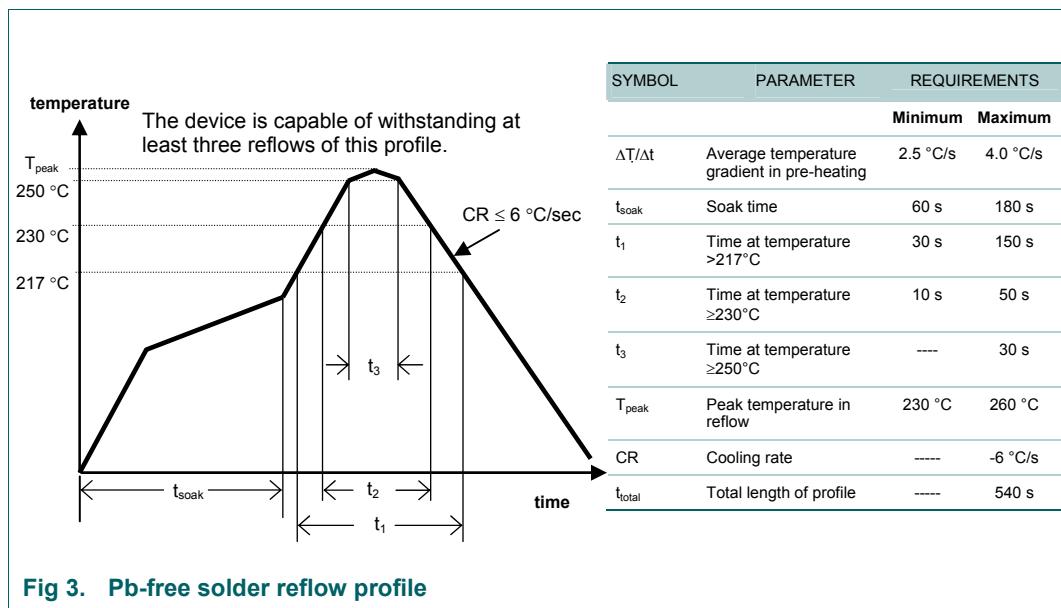


Fig 3. Pb-free solder reflow profile

## 6. Package outline

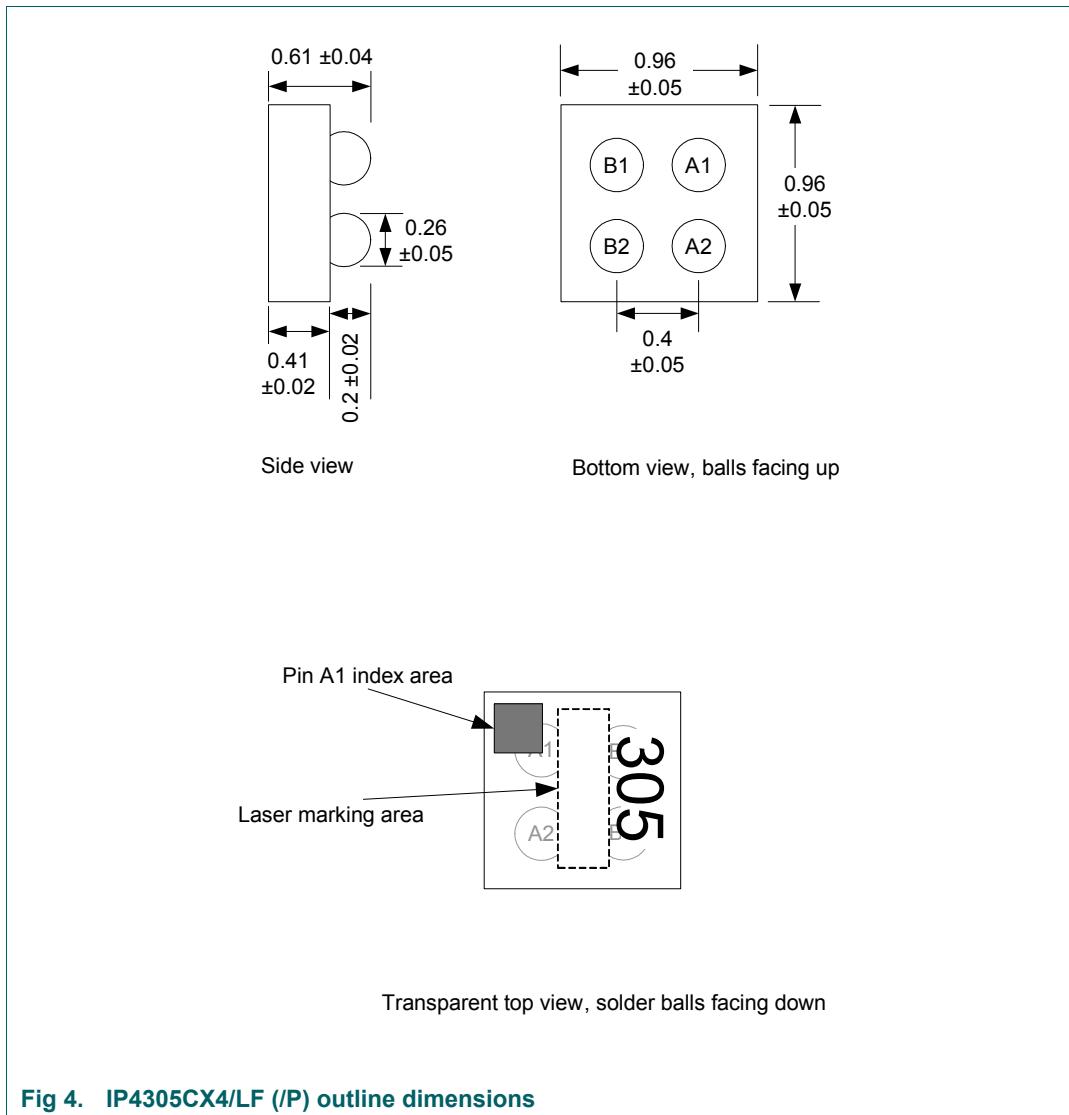
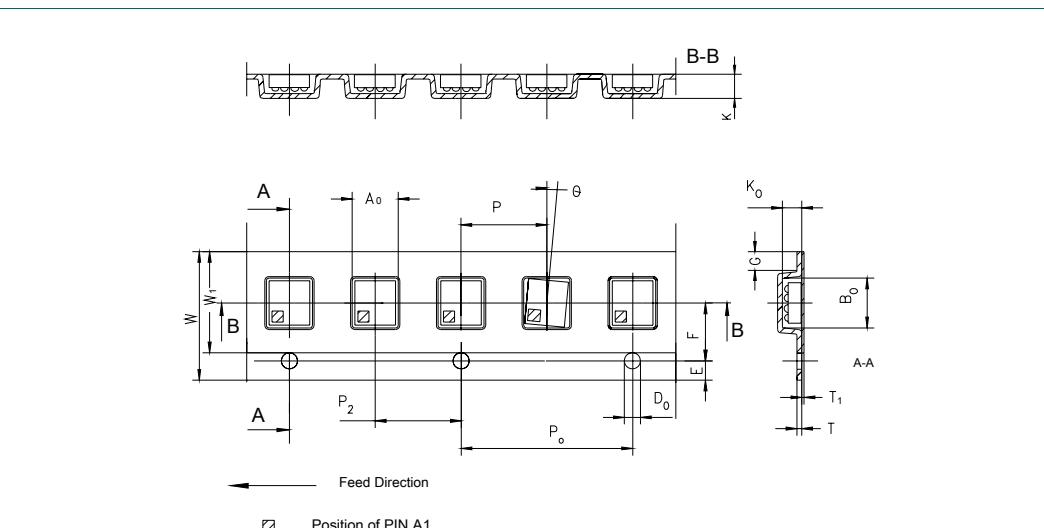


Fig 4. IP4305CX4/LF (/P) outline dimensions

## 7. Tape & Reel information



ITEM	SYMBOL	SPECIFICATIONS		NOTE
		DIMENSION	TOLERANCE	
OVERALL DIMENSIONS	TAPE WIDTH	W	8.00	$\pm 0.1$
	THICKNESS	K	1.20	MAX
	DISTANCE	G	0.75	MIN
SPROCKET HOLES	DIAMETER	D <sub>0</sub>	1.50	$+0.1/-0.0$
	DISTANCE	E	1.75	$\pm 0.1$
	PITCH	P <sub>0</sub>	4.00	$\pm 0.1$
DISTANCE BETWEEN CENTRE LINES	LENGTH DIRECTION	P <sub>2</sub>	2.00	$\pm 0.05$
	WIDTH DIRECTION	F	3.50	$\pm 0.05$
COMPARTMENTS	LENGTH	A <sub>0</sub>	1.06	$\pm 0.05$
	WIDTH	B <sub>0</sub>	1.06	$\pm 0.05$
	DEPTH	K <sub>0</sub>	0.70	$\pm 0.05$
	PITCH	P	2.00	$\pm 0.1$
DEVICE	OUTLINE	IP4305CX4/LF (/P)		
	ROTATION	$\Theta$	20°	MAX
CARRIER TAPE ANTISTATIC	FILM THICKNESS	T	0.25	$\pm 0.07$
	BEND		0.25	$\pm 0.07$
COVER TAPE	WIDTH	W <sub>1</sub>	5.75	MAX
	FILM THICKNESS	T <sub>1</sub>	0.1	MAX
BENDING RAD	IN WINDING DIRECTION	R	30	MIN

Fig 5. IP4305CX4/LF (/P) Tape & Reel information

## 8. Legal information

### 8.1 Data sheet status

Document status <sup>[1,2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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