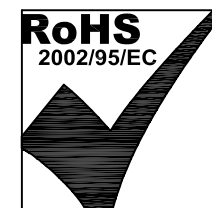


ELECTRICAL SPECIFICATIONS:

- | | | |
|-------------------------------|------------------------------|------------------------------------------|
| 1.0 TURNS RATIO: | (P6-P5-P4) : (J6-J3) | : 1CT : 1CT± 3% |
| | (P3-P2-P1) : (J2-J1) | : 1CT : 1CT ± 3% |
| 2.0 INDUCTANCE: | (P6-P4) | : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias |
| | (P3-P1) | : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias |
| 3.0 LEAKAGE INDUCTANCE: | P6-P4 (WITH J6 AND J3 SHORT) | : 0.3 MAX. @ 1MHz |
| | P3-P1 (WITH J2 AND J1 SHORT) | : 0.3 MAX. @ 1MHz |
| 4.0 INTERWINDING CAPACITANCE: | (P6,P5,P4) TO (J6,J3) | : 30pf MAX @ 1MHz |
| | (P3,P2,P1) TO (J2,J1) | : 30pf MAX. @ 1MHz |
| 5.0 DC RESISTANCE: | (J6-J3)=(J2-J1) | : 1.2 ohms Max. |

NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.



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SHEET
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DRAWING NO. SI-60091-F REV. 17

RECEIVE

6.0 RETURN LOSS: 1MHz TO 30MHz : 18dB MIN.
60MHz TO 80MHz : 12dB MIN.

NOTE: 100 OHMS CONNECTED TO (J2-J1) OR (J6-J3).

7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P3) : 1500 VAC
(J3, J6) TO (P4, P6) : 1500 VAC

8.0 INSERTION LOSS: RS=RL=100 ohms :
100KHz TO 100MHz : 1.1 dB TYP

9.0 RISE TIME: RS=100 OHMS AND RL = 100 OHMS :
OUTPUT VOLTAGE = 1 V peak : 3.0 nS MAX
PULSE WIDTH= 112nS : 3.0 nS MAX

10.0 CROSS TALK: 1MHz TO 100MHz : 40 dB TYP

11.0 COMMON TO COMMON MODE ATTENUATION: 30MHz TO 100MHz : 35dB TYP

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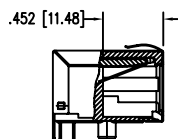
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SHEET
2 OF 4

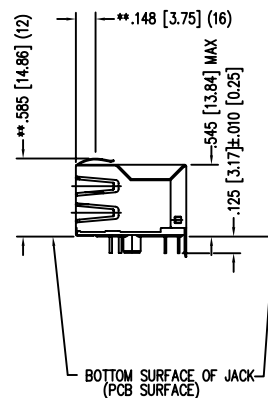
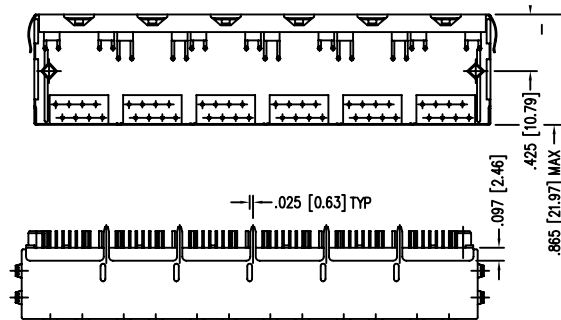
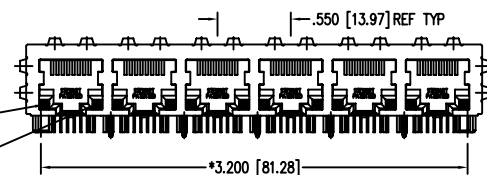
DRAWING NO. SI-60091-F

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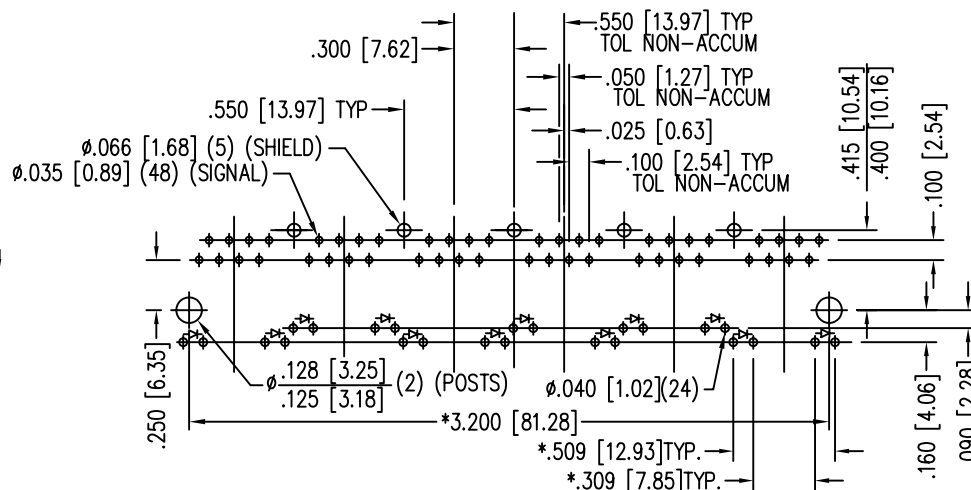
* WITH A FORWARD CURRENT OF 20 mA

[illegible]

LED GRN —
(6 PLACES)



1. CONNECTOR MATERIALS:
HOUSING: THERMOPLASTIC UL94 V-0
CONTACT/SHIELD: COPPER ALLOY
SHIELD PLATING: NICKEL OR TIN
CONTACT PLATING: SELECTIVE GOLD,
50 MICRO-INCHES MIN. IN CONTACT AREA.
2. PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED.
SEE ELECTRICAL DRAWING FOR OMITTED PINS.
3. TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
4. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE ± 0.005 [0.1
5. WAVE SOLDER COMPATIBLE - PREHEAT 125°C/90SECS.



RoHS
2002/95/EC

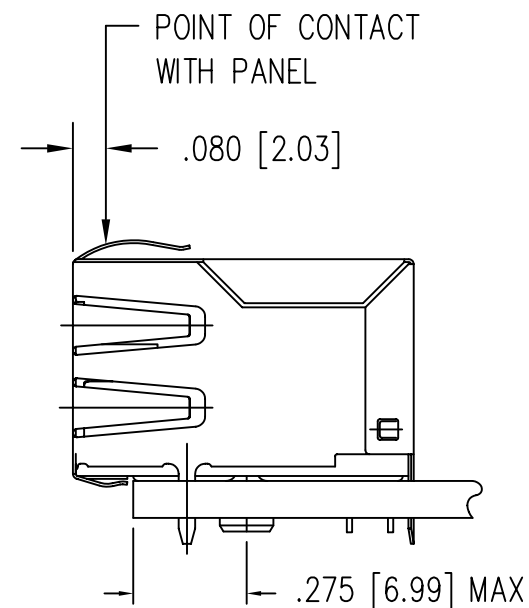
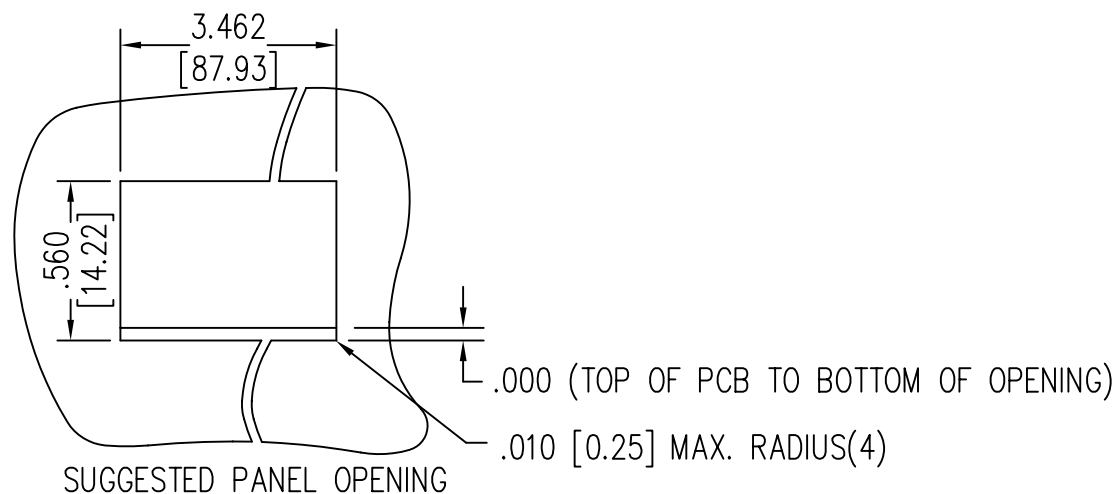
A circuit diagram of a differential amplifier. It consists of two input nodes, each marked with a circle and a cross, indicating they are to be connected to a signal source. The inputs are connected to the bases of two transistors in a differential pair configuration. The emitters are connected to a common point, which is then connected to ground. The collectors are connected to a common load resistor, which is also connected to a positive supply voltage. The output is taken from the collector of one of the transistors.

SINGLE COLOR LED

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REV. 05



1. THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.
2. ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE $\pm .005$ [0.13]

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4 OF 4

DRAWING NO. SI-60091-F REV. 05