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SWRS031A–OCTOBER 2005–REVISED DECEMBER 2005

Fully Integrated Analog Front-End Dual Receiver Base Unit for 27-MHz Wireless Mouse and Keyboard Systems

FEATURES

- **23 Discrete Components Intgrated Into One Chip**
  - **Only External Components are Bypass and Filter Capacitors, and One Crystal**
- **RF Tuner, Mixer, Transistors, Passives, Coils, and SAW Filter Functionality All on One Chip**
- **Integrated Phase Locked Loop**
- **8 User-Selectable Frequencies**
  - **Each Channel (Mouse and Keyboard) Can Independently Select Any of the Available Frequencies**
- **Internally Generated 6-MHz Clock to Drive USB Microcontroller**
- **High Data Throughput Rate**
  - **5-kHz Square Wave Simultaneously per Channel**
  - **10 kbps Miller Encoded Data**
- **I^2C Control Interface**
- **Received Signal Strength Indicator (4-Blt)**
- **5-V, 52 mA Supply**
- **Available in 28-Pin TSSOP (PW) Package**

APPLICATIONS

- **27-MHz Wireless Mouse and Keyboard Systems**
- **Human Interface Devices**
- **Wireless Control**
- **Remote Control Toys**
- **Wireless Headset**
- **Remote instrumentation**

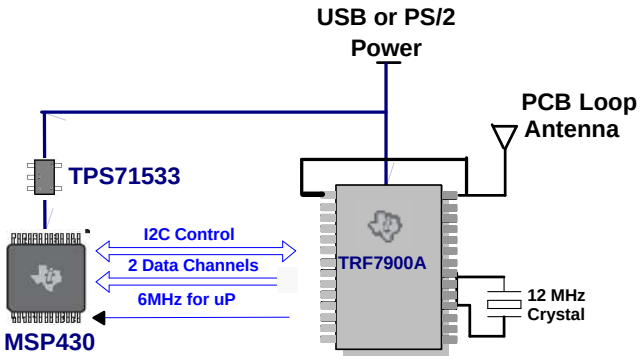
DESCRIPTION

The TRF7900A is a dual integrated RF transceiver designed for Human Interface Devices (HID). Operating at 27 MHz, it integrates multiple components (PLL, RF mixer, simulated SAW filter, tuning circuit, and miscellaneous passive components) to provide frequency selection from 8 discrete channels. This integration lowers component, manufacturing and system costs.

The TRF7900A simplifies system design by reducing system component count and manual circuit tuning. By integrating the PLL, SAW filter, and RF mixer, the TRF7900A eliminates the manual tuning of RLC circuits required in traditional implementations.

The receiver also generates 8 frequencies that can be programmatically selected via the I^2C interface bus for both the mouse channel and/or the keyboard channel. Another 6-MHz clock is internally generated to clock the USB microcontroller; this enables a single crystal to be used to supply the clock needs for the receiver channels and the microcontroller.

The optimized receiver design enables simultaneous reception on both parallel channels up to 5 kHz (10 kbps Miller encoding) per channel. A receive strength signal indicator register can be read via the I^2C bus to determine if the transmit signal is too weak (weak battery or too far), or if there is too much noise on the selected channel in the user's area.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
TRF7900APW	TSSOP - 28	Rails, 50
TRF7900APWR		Tape and Reel, 2000

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
V_{S-} to V_{S+}	Supply voltage	5.5	V
V_I	Input voltage	$\pm V_S \pm$ 0.5	V
V_{ID}	Differential input voltage	±2	V
	Continuous power dissipation	See Dissipation Rating Table	
T_J	Maximum junction temperature, any condition(2)	150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(2)	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300	°C
	ESD ratings: Human Body Model	4000	V
	ESD ratings: Charged Device Model	1500	V
	ESD ratings: Machine Model	200	V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC}	θ_{JA}(1)	POWER RATING(2)	
			$T_A \leq 25°C$	$T_A = 85°C$
PW (28)	13.7	56.5	1.77 W	708 mW

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S-} to V_{S+}	Suppy voltage, analog	4.0		5.5	V

ELECTRICAL CHARACTERISTICS

V_S = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF SPECIFICATIONS(1)(2)(3)							
	Precision of required external 12-MHz crystal	T_A = -40°C to 85°C				50	ppm
	Channel spacing				50		kHz
	Communication spacing	T_A = 25°C			26.995		MHz
					27.045		MHz
					27.095		MHz
					27.145		MHz
					27.195		MHz
					27.295		MHz
		Optional channel			27.245		MHz
		Optional channel			26.945		MHz
	Carrier stability of the transmitter and receiver				±120		ppm
	Antenna input resistance	DC Differential			<100		kΩ
		27 MHz			5		kΩ
	Antenna input capacitance	T_A = 25°C			5		pF
R_O	Output resistance, Out_1 and Out_2	T_A = 25°C			1.2	2.0	kΩ
		T_A = 0°C to 70°C				2.0	
		T_A = -40°C to 85°C				2.0	
	Sensitivity(1)	Differential voltage on antenna inputs 50 Ω to input 5 kΩ Impedance-transform	T_A = 25°C	20	14		µV
				-98	-102		dBm
			T_A = 0°C to 70°C	-98			dBm
			T_A = -40°C to 85°C	-98			dBm
	Adjacent channel rejection (2)	Offset = 50 kHz	T_A = 25°C	30	34		dB
			T_A = 0°C to 70°C	30			dB
			T_A = -40°C to 85°C	30			dB
		Offset = 100 kHz or 150 kHz	T_A = 25°C	43	38		dB
			T_A = 0°C to 70°C	43			dB
			T_A = -40°C to 85°C	43			dB
	Co-channel rejection (3)	2.5 kbaud	T_A = 25°C	5	5		dB
			T_A = 0°C to 70°C	5			dB
			T_A = -40°C to 85°C	5			dB
		5 kbaud	T_A = 25°C	9	7		dB
			T_A = 0°C to 70°C	9			dB
			T_A = -40°C to 85°C	9			dB
	Spurious rejection	T_A = 25°C			25		dB
		T_A = 0°C to 70°C		25			dB
		T_A = -40°C to 85°C		25			dB
	Dynamic range	T_A = 25°C			60		dB
	Number of bits on RSSI	T_A = 25°C			4		bits
	RSSI update time	T_A = 25°C			100		ms

(1) FM deviation = ±3.2 kHz, Data rate = 2.5 kbaud, PER < 0.08%.
(2) FM deviation = ±3.2 kHz, Data rate = 2.5 kbaud, PER < 0.08%. Unwanted signal is FM modulated using sine wave 1 kHz and ±3.2 kHz FM modulation depth.
(3) FM deviation = ±3.2 kHz, Data rate = 2.5 kbaud, PER < 0.08%. Co-channel signal is FM modulated using sine wave 1 kHz and ±3.2 kHz FM modulation depth.

ELECTRICAL CHARACTERISTICS (continued)

V_S = 5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FSK MODULATION							
	Frequency deviation	T_A = 25°C			3.2		kHz
	Data rate				5000		bit/s
	Preamble length				6		ms
POWER SUPPLY							
	Operating voltage	Analog	T_A = 25°C	4.0	5	5.5	V
			T_A = 0°C to 70°C	4.0		5.5	
			T_A = -40°C to 85°C	4.0		5.5	
		Digital (SCL and SDA input logic HIGH)	T_A = 25°C		5	3.6	V
			T_A = 0°C to 70°C			3.6	
			T_A = -40°C to 85°C			3.6	
		Digital (SCL and SDA input logic LOW)	T_A = 25°C	3.1	5		V
			T_A = 0°C to 70°C	3.1			
			T_A = -40°C to 85°C	3.1			
	Normal mode supply current	T_A = 25°C		38	50	65	mA
		T_A = 0°C to 70°C		38		65	
		T_A = -40°C to 85°C		38		65	
	Power-down supply current	Both receivers powered down, oscillator active, and CLO not loaded	T_A = 25°C		0.9	1.2	mA
			T_A = 0°C to 70°C			1.2	
			T_A = -40°C to 85°C			1.2	
	Internal supply volltage references	VPOS1, VPOS2, VDIG, VPOS_LO1, VPOS_LO2	T_A = 25°C		3.3	3.6	V
			T_A = 0°C to 70°C			3.6	
			T_A = -40°C to 85°C			3.6	
	Internal Mid-rail reference	MDR	T_A = 25°C		1.6	1.7	V
			T_A = 0°C to 70°C			1.7	
			T_A = -40°C to 85°C			1.7	
QUARTZ XTAL AND PROGRAMMING							
	Frequency	Fundimental mode operation	T_A = 25°C		12.000000		MHz
	Frequency tolerance		T_A = 25°C		±50		ppm
	Shunt capacitance		T_A = 25°C		7.0		pF
	Aging		T_A = 25°C		<5		ppm/yr
	Power-up settling time	Time prior to I^2C programming command	T_A = 25°C		20		ms

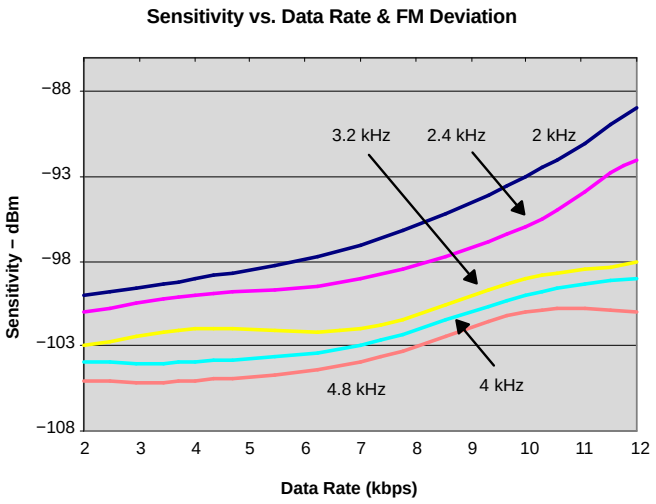


Figure 1.

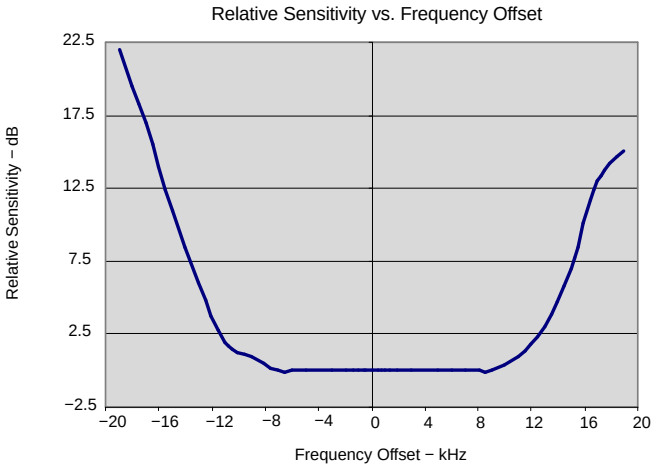


Figure 2.

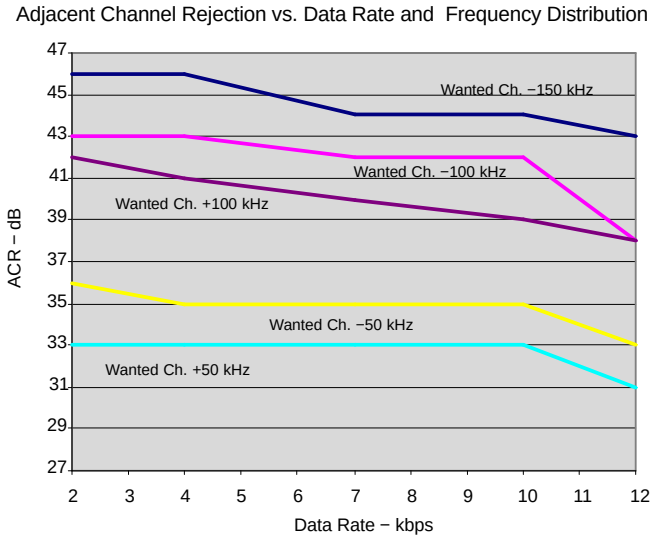


Figure 3.

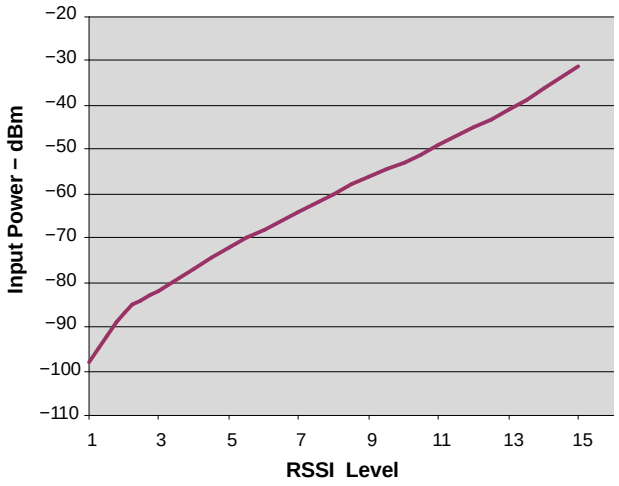


Figure 4.

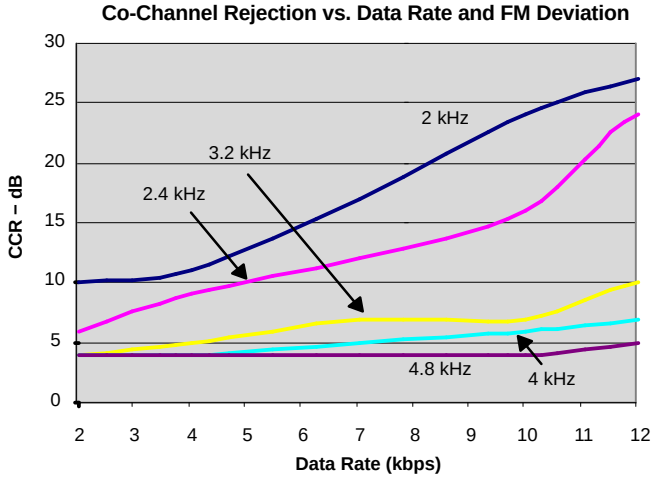
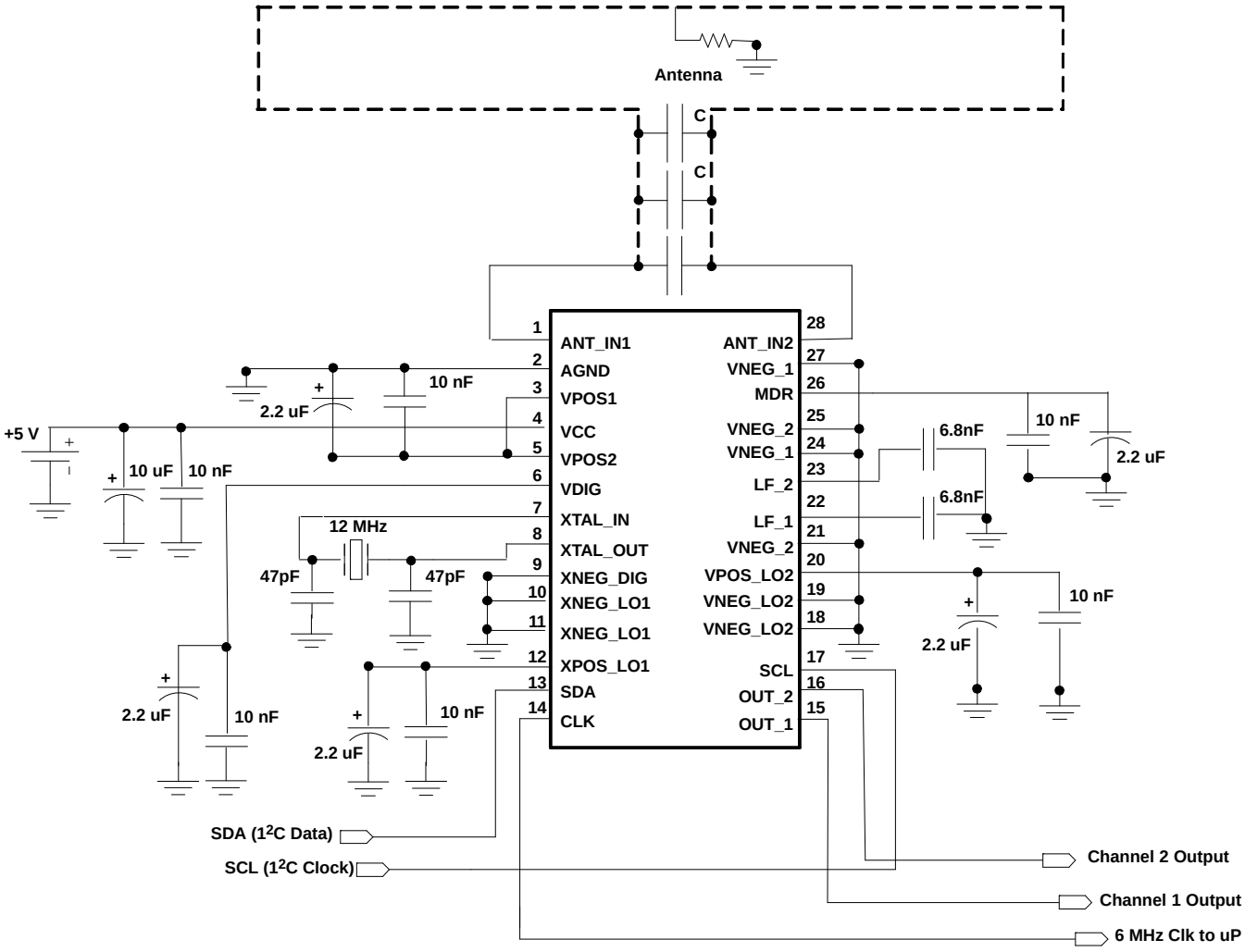


Figure 5.

APPLICATION SCHEMATIC



DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION	RECOMMENDED EXTERNAL COMPONENTS
NAME	NO.			
ANT_IN1	1	I	Antenna input #1	Antenna input
AGND	2		Analog ground	
VPOS1	3		Positive internal analog supply #1	Cap. 2.2 µF and 10 nF to AGND
VCC	4		External positive supply	Cap. 10 µF and 10 nF to AGND
VPOS2	5		Positive internal analog supply #2	Cap. 2.2 µF and 10 nF to AGND
VDIG	6		Positive internal digital supply	Cap. 2.2 µF and 10 nF to AGND
XTAL_IN	7	I	12-MHz quartz oscillator input	Xtal input and 47 pF load capacitor
XTAL_OUT	8	O	12-MHz quartz oscillator output	Xtal output and 47 pF load capacitor
VNEG_DIG	9		Negative internal digital supply	
VNEG_LO1	10		Negative internal supply LO 1	
VNEG_LO1	11		Negative internal supply LO 1	
VPOS_LO1	12		Positive internal supply LO 1	Cap. 2.2 µF and 10 nF to AGND
SDA	13	I	I^2C data	
CLK	14	O	6-MHz clock output	
OUT_1	15	O	Channel #1 output	
OUT_2	16	O	Channel #2 output	
SCL	17	I	I^2C clock	
VNEG_LO2	18		Negative internal supply LO 2	
VNEG_LO2	19		Negative internal supply LO 2	
VPOS_LO2	20		Positive internal supply LO 2	Cap. 2.2 µF and 10 nF to AGND
VNEG_2	21		Negative internal analog supply #2	
LF_1	22	I	Loop filter input for local oscillator #1	Cap. 6.8 nF to AGND
LF_2	23	I	Loop filter input for local oscillator #2	Cap. 6.8 nF to AGND
VNEWG_1	24		Negative internal supply FM demod. #1	
VNEG_2	25		Negative internal supply FM demod. #2	
MDR	26		Mid rail reference voltage	Cap. 2.2 µF and 10 nF to AGND
VNEG_1	27		Negative internal analog #1 supply	
ANT_IN2	28	I	Antenna input #2	Antenna input

FUNCTIONAL DESCRIPTION

Reference and Supply Block

The REFERNCE block generates the reference voltage MDR. The MDR voltage is an internally generated voltage reference and has nominal level of 1.6 V. The MDR voltage output requires external capacitors for RF filtering and noise reduction. In low power mode the current supply of this block is reduced so that the reference maintains its functionality.

The five internal supply regulators (VPOS1, VPOS2, VDIG, VPOS_LO1, VPOS_LO2) use the MDR as a reference for supply voltage regulation. The regulated supply voltages are nominally 3.4V. The recommended filter capacitors are 10 μF in parallel with 10 nF for VCC (pin 4). However, the 5 internal supply regulator filter capacitors can be decreased to 2.2 μF in parallel with 10nF and still maintain functionality. In low power mode, the current requirements for these blocks are reduced but they still maintain functionality.

Crystal Oscillator and Internal Divider

The TRF7900 utilizes an external 12 MHz quartz crystal oscillator to generate the system clock and ensure proper synchronization between the components of the system. The 12 MHz clock is utilized by the local oscillator PLL system for internal reference frequency generation. This clock is also divided by 2 within the TRF7900 to provide a 6MHz output (CLK) that can be utilized by the external micro-controller. This ensures that all aspects of the system are continuously synchronized and eliminates the need for added external components. The internal oscillator and the divider blocks are constantly active, even when in power down mode.

PLL and VCO

The internal LO/PLL is capable of providing two LO signals for the receiver mixers. The desired frequency is synthesized from the 12MHz signal reference generated within the crystal oscillator. The desired channel is defined by a three-bit code for each of the two channels. The channel selection data is sent via the I^2C protocol.

The TRF7900 incorporates two fully integrated voltage controlled oscillators. The only external components required in the two PLL and VCO systems are the shunt loop filter capacitors. Theses capacitors are connected to LF_1 and LF_2 pins on the TRF7900A. They should be placed in close proximity to the pins of the device.

Since the LO signals are not present at any of the output pins of the device, the possibility of LO leakage to the antenna is minimized. This simplifies board design and eases concerns relating to ECM emissions.

The table below presents the programmable channels that can be selected via the I^2C code.

I2C CODE	CHANNEL FREQUENCY	UNIT
000	26.995	MHz
001	27.045	MHz
010	27.095	MHz
011	27.145	MHz
100	27.195	MHz
101	27.245	MHz
110	27.295	MHz
111	26.945	MHz

RECEIVER

Two separate receivers are utilized within the TRF7900 for the two output channels. They are super heterodyne receivers composed of low noise amplifiers, mixers, IF filters and IF amplifiers followed by two FSK demodulators. This down conversion process converts the dual 27 MHz signals to two individual output data streams for the micro controller for processing.

LNA and Mixer

The integrated low noise amplifier is a multi stage amplifier operating at 27 MHz. The differential antenna input impedance of the part is greater than 5 kΩ, which allows for the utilization of a high Q antenna. The mixers are driven by the internal LO signals generated within the PLL and VCO sections.

IF Filter and Amplifier

The IF filter and amplifier stages are completely integrated in the TRF7900A. The selectivity of the IF filter allow for optimum reception and attenuation of adjacent channel interferer signals (≥50 kHz out of the center frequency).

FSK Demodulator

There are two completely integrated PLL based FSK demodulators. The analog signal generated in the receiver chain is digitized and used as the reference clock to the PLL. The FM demodulated signal is available to the PLL loop filter signal in controlling the VCO. The VCO control signal is digitized and results in a digital signal which is displayed at the output (OUT_1 and OUT_2). The demodulator is designed for a nominal frequency deviation of 3.2 kHz and data rate of 5 kbps (Miller coded).

RSSI Block

The signal level before and after the IF filters is measured. Signal levels on both sides of the filter are used to calculate actual RSSI level. The RSSI levels are indicated by a 4 bit representation each with a 4dB step size. The dynamic range is 64 dB. The RSSI level for both channels can be read via the I^{2}C interface.

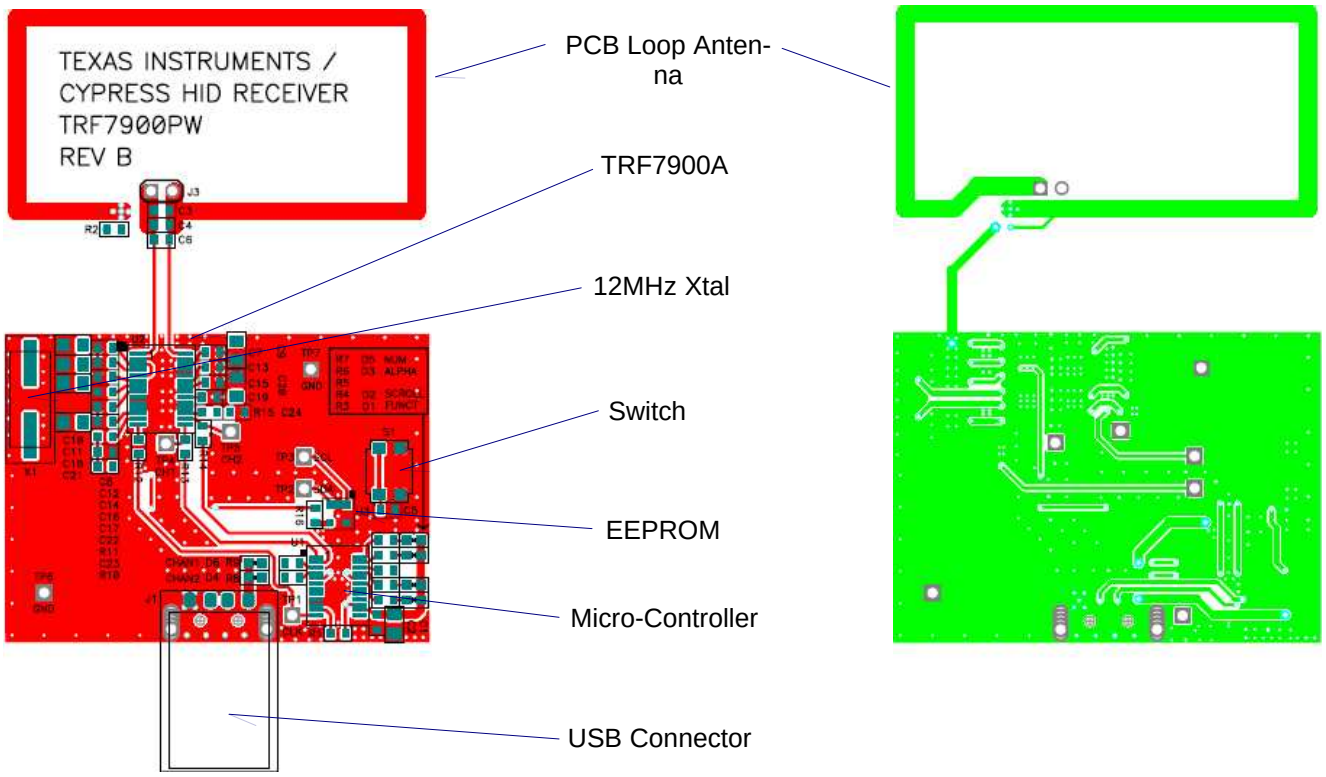


Figure 6. TI Desktop Reference Design

I^{2}C INTERFACE DESCRIPTION AND PROGRAMMING

The TRF7900A IC communicates with the micro-controller using a standard I^{2}C interface. It receives commands (channel selection and power-down) from the micro-controller and sends the RSSI information back to the controller. The micro-controller behaves as the master and the TRF7900A behaves as the slave in this aspect of operation. The I^{2}C interface on the board uses 7-bit addressing mode and single byte write and read operation. The 7-bit I^{2}C address used for the TRF7900A is 1101100. The TRF7900A is capable of communication with

normal speeds up to 100kbps and in Fast I2C mode with transfer rates of up to 400 kbps. However, the maximum speed of the I^2C communication in the TRF7900A is externally limited to 30kbps by the filters on the SDA and SCL lines. This is to help minimize the high-frequency overtones from the signals which could couple to the antenna and degrade the system sensitivity. With proper considerations in the PCB layout, the transfer rate could be increased.

NOTE:

At initial startup/reset, the micro-controller should allow a minimum of 20 ms for the quartz crystal to stabilize prior to programming the TRF7900A via the I^2C.

I^2C Write Operation

The *write* command can be utilized to set the receiving frequencies for both channels of the TRF7900A. The SDA data stream should be as follows with respect to the clock or SCL.

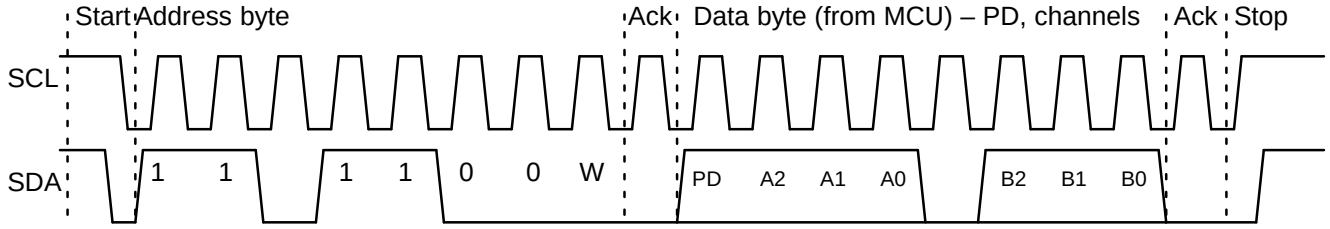


Figure 7. I^2C Communication - Write Command

Where:

Start = Start bit

Address byte = Address of TRF7900A (1101100)

W = Write command (logic level LOW)

Ack = acknowledge bit from the slave (slave pulls SDA low)

PD =Power Down bit (0 = normal mode, 1 = power down mode)

Data byte = Frequency selection bits for Channel 1 and 2 (see table below)

A0 to A2 = Channel 1 frequency selection

B0 to B2 = Channel 2 frequency selection

B3 =reserved bit which should be set to 0

Ack = acknowledge bit from the master (master pulls SDA low)

Stop = Stop bit

CHANNEL SELECTION BITS			CHANNEL FREQUENCY
BIT 2 (MSB)	BIT 1	BIT 0 (LSB)	
0	0	0	26.995 MHz
0	0	1	27.045 MHz
0	1	0	27.095 MHz
0	1	1	27.145 MHz
1	0	0	27.195 MHz
1	0	1	27.245 MHz
1	1	0	27.295 MHz (1)
1	1	1	26.945 MHz (1)

(1) Not used in the EVM

I²C Read Operation

The *read* command is similar to the *write* command. It is utilized to read the RSSI level from the TRF7900A and communicate it to the micro-controller for processing. The SDA data stream with respect to the clock or SCL is as follows.

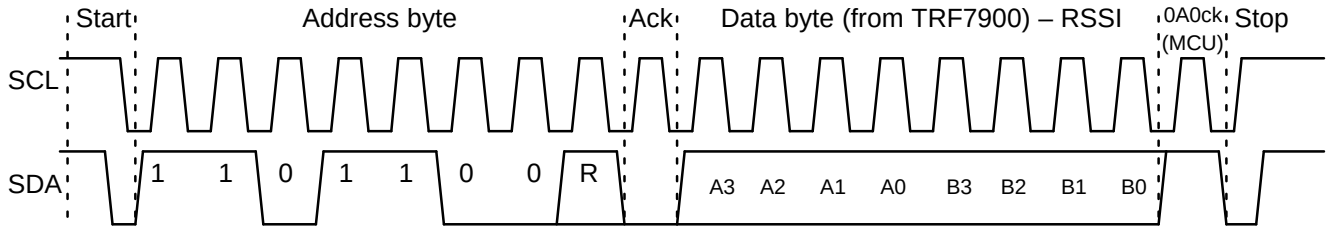


Figure 8. I²C Communication - Read Command

Where:

Start = Start bit
Address byte = Address of TRF7900A (1101100)
R = Read command (logic level HIGH)
Ack = acknowledge bit from the slave (slave pulls SDA low)
Data byte = RSSI data from TRF7900A
A0 to A3 = Channel 1 RSSI level (A3=MSB, A0=LSB)
B0 to B3 = Channel 2 RSSI level (B3=MSB, B0=LSB)
Ack (MCU) = acknowledge bit from the master (master pulls SDA low)
Stop = Stop bit

Peamble

The preamble has to be long enough to ensure proper settling of the FM demodulator in the receiver. The preamble length is typically set to 10 msec. This allows enough time for the FM demodulator to settle and prevents any loss of data from the transmitter.

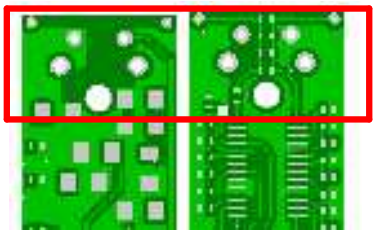
Antenna Considerations

Antennas are used as the primary method of detecting the transmit signal from the Transmit source. The type of antenna, layout, location and size of the antenna plays an important role in the reception. There are a variety of different types of antennas available but two types are commonly used for HID applications, wire wound coils and PCB etched on antennas.

The wire wound coil antennas are made of copper that is coated with a thin insulative film. The wire is wound in a rectangular or oval manner to a certain length that represents a certain inductance value. It is then connected to the differential inputs of the TRF7900A along with some parallel capacitors. The combination of the inductive coil and capacitance provide for a resonance at the desired frequency of operation which is chosen to be centered at 27.1 MHz. It is recommended that special care be taken in the selection of the antenna coil and their tuning capacitors. The antenna coil and tuning capacitors should be designed such that it will have an input impedance of 5kohm and maintain a high quality factor (Q) value between 60-80. The Q is defined as (center frequency)/(3 dB band width). If the desired impedance can not be achieved, then an impedance matching circuit should be utilized to match the antenna to the antenna inputs of theTRF7900. This will ensure sufficient antenna reception and efficient selectivity of the desired signal.

The next type of antenna is the PCB etched on antenna. This type of antenna is similar to the wire wound in functionality but differs in that it is made up of a trace that is etched into the same PCB that the receiver circuitry is on. One advantage of this method is that the manual placement of a through-hole wire-wound coil antenna is eliminated and the cost associated with the coil. The PCB etched on antenna is typically more repeatable since its tolerances are tightly maintained by the PCB manufacturer. The PCB etched on antenna behaves similarly to the coil in that it is looped around the board or at the end of the board and provides for a certain inductance.

When doing a PCB antenna, please take special care in the placement of the active circuitry and ground plane near the antenna as it will affect the performance of the antenna. It is also recommended (for multilayer boards) to place the traces on multiple layers directly on top of each other and also to follow the same direction. The items that impact the performance of the antenna include proximity of uP and active circuitry, area, width and thickness of the antenna trace. Slight improvements can also been achieved by leaving off the solder resist on the antenna traces. The user should design their antenna to maximize the available area such that the design is done to utilize area is is going to be a key in



NOTE:

When connecting the antenna to the TRF7900A and input tuning capacitors, it is important to remove all the ground directly under the input antenna traces all the way to the input of the TRF7900A. Otherwise, the trace and ground combination will create a transmission line with a specific impedance characteristics and frequency dependences. This is undesirable and will decrease the performance of the system.

TYPICAL APPLICATION AND RESULTS

The TRF7900A can be used in many applications requiring single/dual channel capabilities that utilize the 27 MHz band. One of the common applications is its use in HID designs where wireless mice and/or keyboards are used. The TRF7900A can be utilized with a programmed micro-controller, EEPROM and some passive components to receive signals transmitted by the source. Below is a sample of an evm dongle that was designed for the TRF7900A.

The TRF7900A when initially powered on, starts off in a low current mode (inactive) and each of the channel selection bits default to 000-state (26.995 MHz). The TRF7900A can be made active only when the proper commands from the micro-controller are sent to the chip. Upon power-up or reset, the micro-controller should allow a minimum of 20ms of startup time prior to sending a command to the TRF7900A. This allows the quartz oscillator enough time to settle and stabilize before the receiver is powered. This ensures optimal functionality of the receiver.

QUARTZ CRYSTAL SELECTION AND OUTPUT CLOCK (CLK)

The TRF7900A requires a 12 MHz crystal for synchronization and proper functionality. This reference is utilized by the internal VCO's and PLL's to provide a robust frequency reference for the receiver as selected by the I^2C. The reference is also used to provide the 6MHz output clock which can be utilized by the external mico-controller or USB converter for USB synchronization.

It is encouraged that the CLK output of the TRF7900A be utilized to clock the microcontroller. If not, there is a chance that the instability caused by the internal clock can degrade system sensitivity and performance. This occurs when the harmonics, generated by the microcontrollers internal reference, spread over the broad receive frequency range of the TRF7900A. This dominant mechanism is magnetic in nature and its coupling is related to the current surges on the micro controllers input supply. For this reason it is extremely important that the lengths of the input supply traces be minimized and decoupling capacitors be situated as close to the pins as possible.

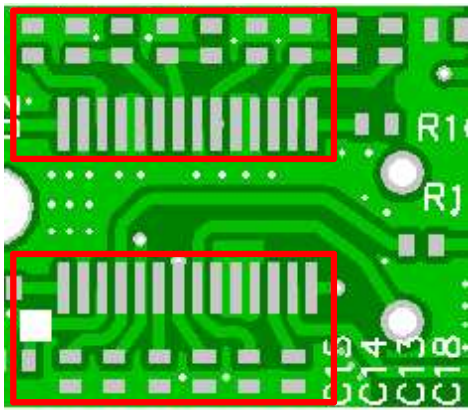
The reference crystal should have the following characteristics.

PARAMETER	SPECIFICATION
Frequency	12.000000 MHz
Mode of operation	Fundamental
Frequency Tolerance	±50ppm
Shunt Capacitance	7.0 pF max
Aging	< 5 ppm/year
Operation Temp Range	–20°C to 70°C

ELIMINATING NOISE AND INCREASING PERFORMANCE

There are many methods to reduce noise (conductive and radiated) and increase performance. This includes parts placement considerations and also layout considerations. First, is the parts placement.

The TRF7900A receiver system utilizes ceramic capacitors at key nodes to help filter out low and high frequency noise. It is recommended that the placement of these components be kept as close to pins on the device as possible on the supply pins of both the TRF7900A and the micro-controller. This is done by minimizing the trace lengths to the capacitors and also having ground vias as close to the capacitors as possible when connecting to the ground plane. This helps to minimize ground loops and conductive noise. When possible, it is also recommended that ground planes be utilized to minimize the impedance associated with the return path to ground.

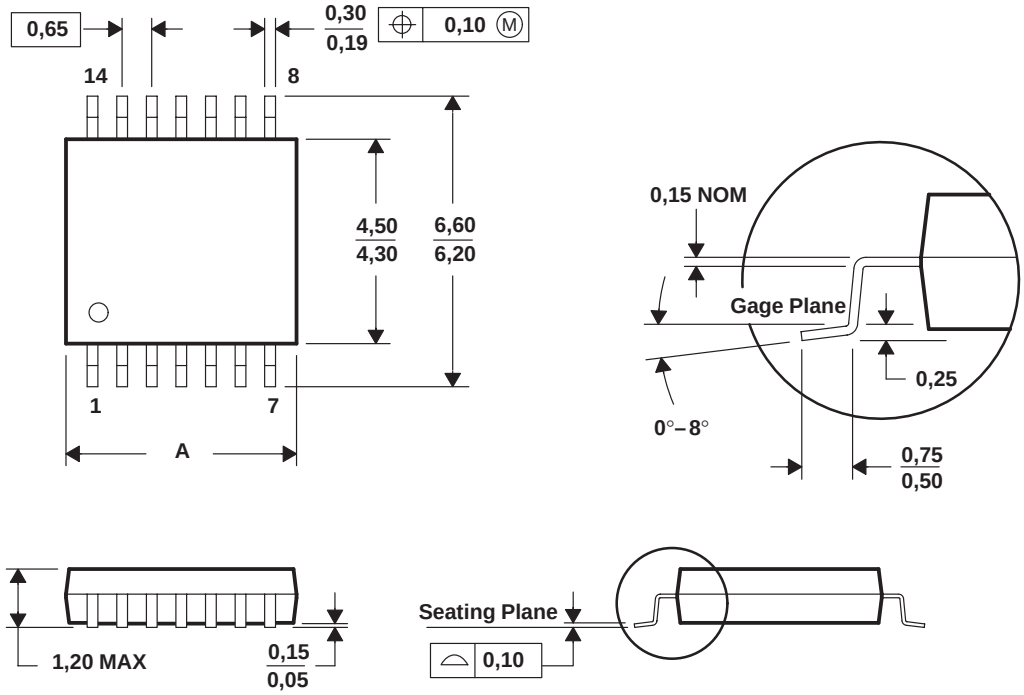


It is also recommended that a similar decoupling scheme be used for the micro controller to minimize its conducted emissions

The second type of method relates to the overall PCB layout. When doing layout, the designer is encouraged to pay close attention to the noise contributors and the sensitive circuits. The micro controller is typically considered the main noise contributor and the TRF7900A receiver as the noise sensitive circuit in this application. It is recommended that the *noisy* components not be kept in close proximity of the receiver. This can be achieved by isolating the two types by proximity. Either the components can be kept on opposite ends of the PCB (top side assembly only) or opposite sides of the PCB (top and bottom assembly). For example, the TRF7900A and quartz crystal can be placed together with minimum trace lengths and the micro controller can be placed away such that the digital signal transitions do not interfere with the receiver. It is recommended that the crossing of sensitive traces such as DC, control, crystal and data lines be kept to a minimum if at all possible during the layout process. Any crossing of these traces on different layers could cause noise to couple on the sensitive lines and in turn impact the performance of the receiver and the system.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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