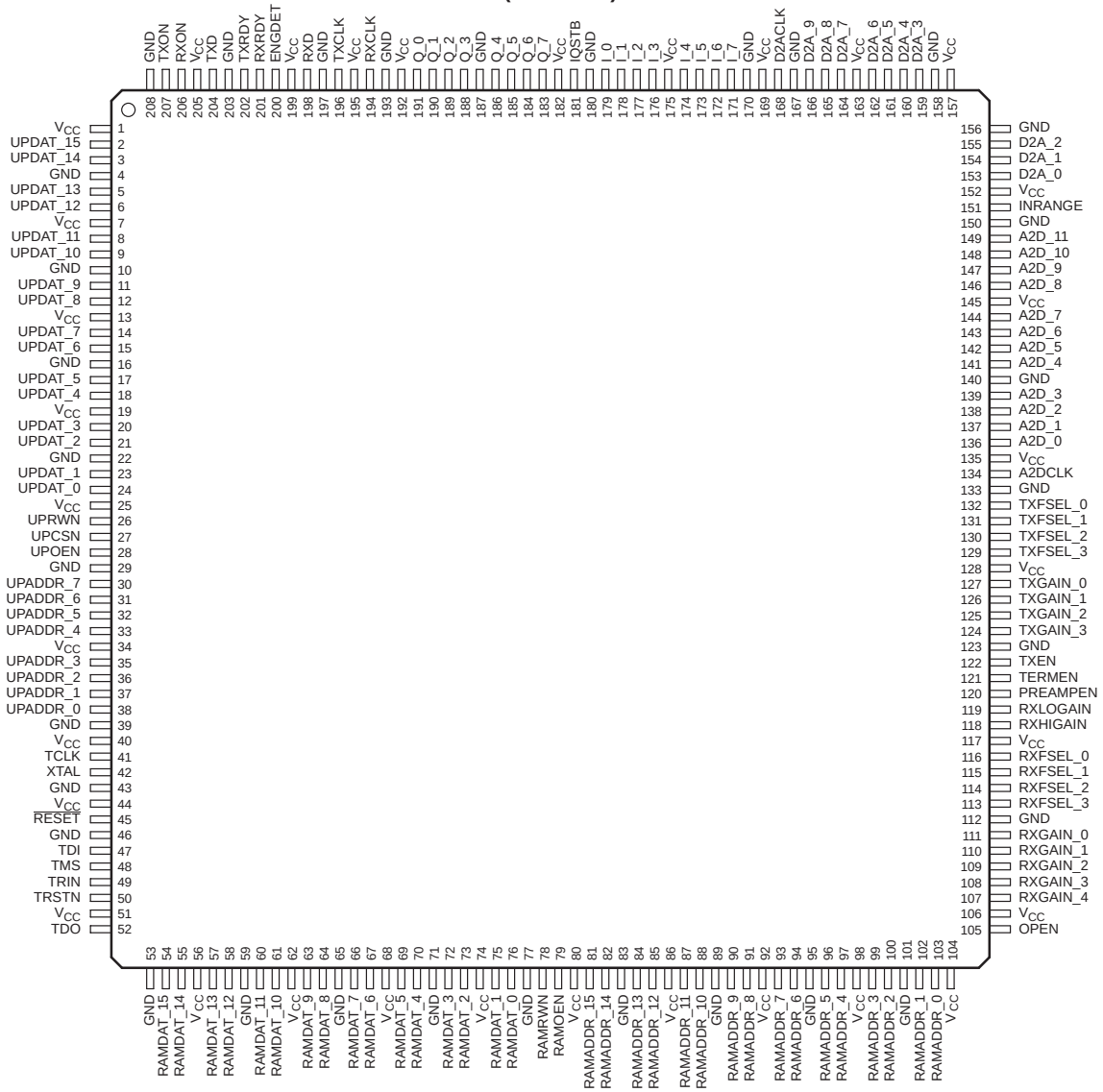
- **Single-Chip EtherLoop Modem**
- **Optimized for Client and Server Modem Applications**
- **Glueless Interface to EtherLoop Processor Interface, Analog-to-Digital Converter (ADC), and Digital-to-Analog Converter (DAC)**
- **Implements 6-Mbit/s Modem Algorithms**
- **Supports Wide Range of Symbol Rates, Allowing Adaptation to Line Conditions**
- **Operates in Presence of Bridge Taps**
- **Industrial Operating Free-Air Temperature to Support Central Office and Distributed Server Applications**
- **Packaged in 208-Pin Plastic Quad Flatpack**

PPB PACKAGE†
(TOP VIEW)



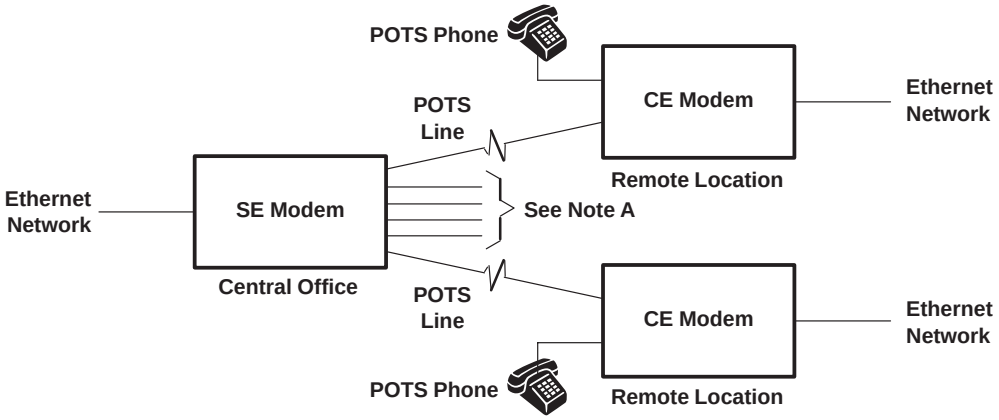
† Thermally enhanced molded plastic package with a heat slug (HSL)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EtherLoop is a trademark of Elastic Networks.

description

The TNETEL1200 is an EtherLoop modem. EtherLoop technology enables simultaneous voice and Ethernet communication over local-loop plain old telephone service (POTS) wiring. The TNETEL1200 supports data rates of up to 6 Mbit/s and POTS wire lengths of up to 21,000 feet. Figure 1 shows a typical system with an EtherLoop modem located at each end of the POTS line. Each EtherLoop modem has a 10Base-T Ethernet interface and is responsible for buffering Ethernet data before sending it over the POTS wire. The server-end (SE) EtherLoop modem is located in a central switching office and can communicate with several client-end (CE) EtherLoop modems, based on a round-robin arbitration scheme. The CE EtherLoop modem typically is located at a remote site.



NOTE A: Flexible multiplexing scheme allows one SE modem to interface with many CE modems.

Figure 1. Typical EtherLoop System

Figure 2 shows a block diagram of a typical CE EtherLoop modem. Ethernet data destined for the POTS wire is received via 10Base-T interface and presented to the EtherLoop processor. The EtherLoop processor performs Ethernet frame processing and buffer management. The EtherLoop processor sends buffered Ethernet frames to the TNETEL1200 EtherLoop modem (via an HDLC interface). The TNETEL1200 performs data modulation before passing the modulated digital data to a digital-to-analog converter (DAC). The resulting analog signal passes to the EtherLoop transceiver, which acts as the line interface. The modem uses a half-duplex communication protocol over the POTS wire, and data received from the POTS wire follows the reverse path back to the Ethernet framer.

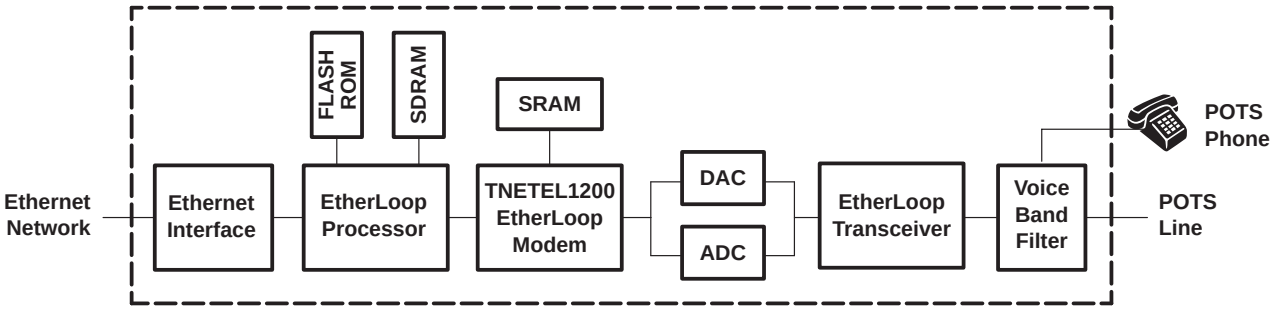


Figure 2. Typical CE EtherLoop Modem

description (continued)

Figure 3 shows a block diagram of a typical SE EtherLoop modem. Data flow follows the same path as in the CE EtherLoop modem. In the SE application, the EtherLoop processor also performs round-robin arbitration between each of the attached EtherLoop transceiver devices.

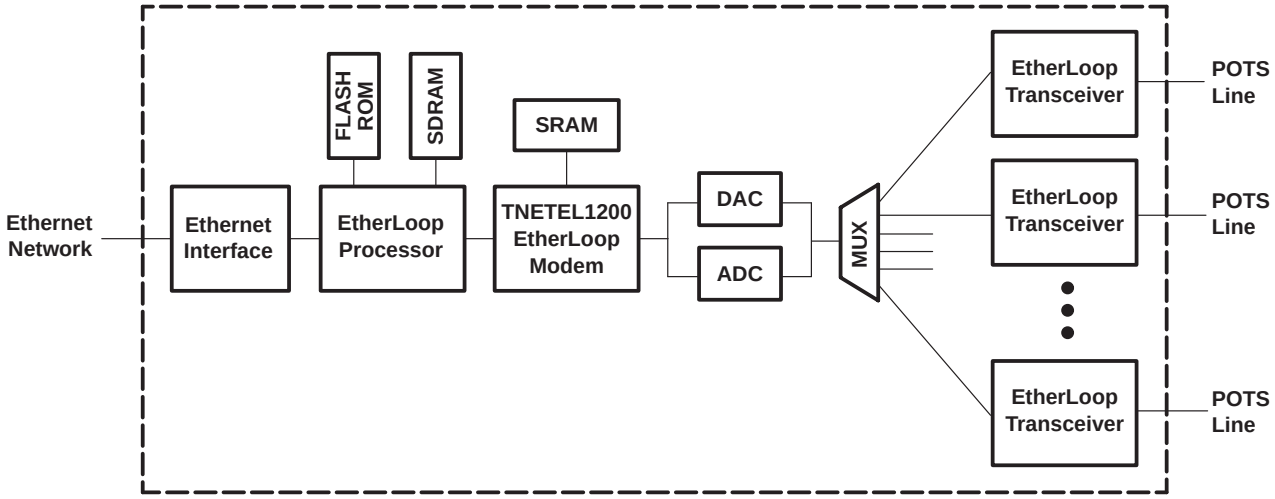


Figure 3. Typical SE EtherLoop Modem

summary of TNETEL1200 EtherLoop modem

- Modulates serial HDLC data stream and presents results to DAC
- Demodulates data from analog-to-digital converter (ADC) and presents results as an HDLC data stream
- Supports wide range of data symbol rates to accommodate a range of line conditions

transmitter and receiver

The TNETEL1200 performs modulation of the digital data stream transmitted from the EtherLoop modem and demodulation of the digital data stream received by the EtherLoop modem. The TNETEL1200 supports a variety of modulation schemes and symbol rates. This flexibility allows the modem to adapt to changing conditions on the POTS line. The modem is designed to compensate for the presence of bridge taps on the POTS line, allowing for easy service deployment.

Figure 4 shows the EtherLoop modem block diagram.

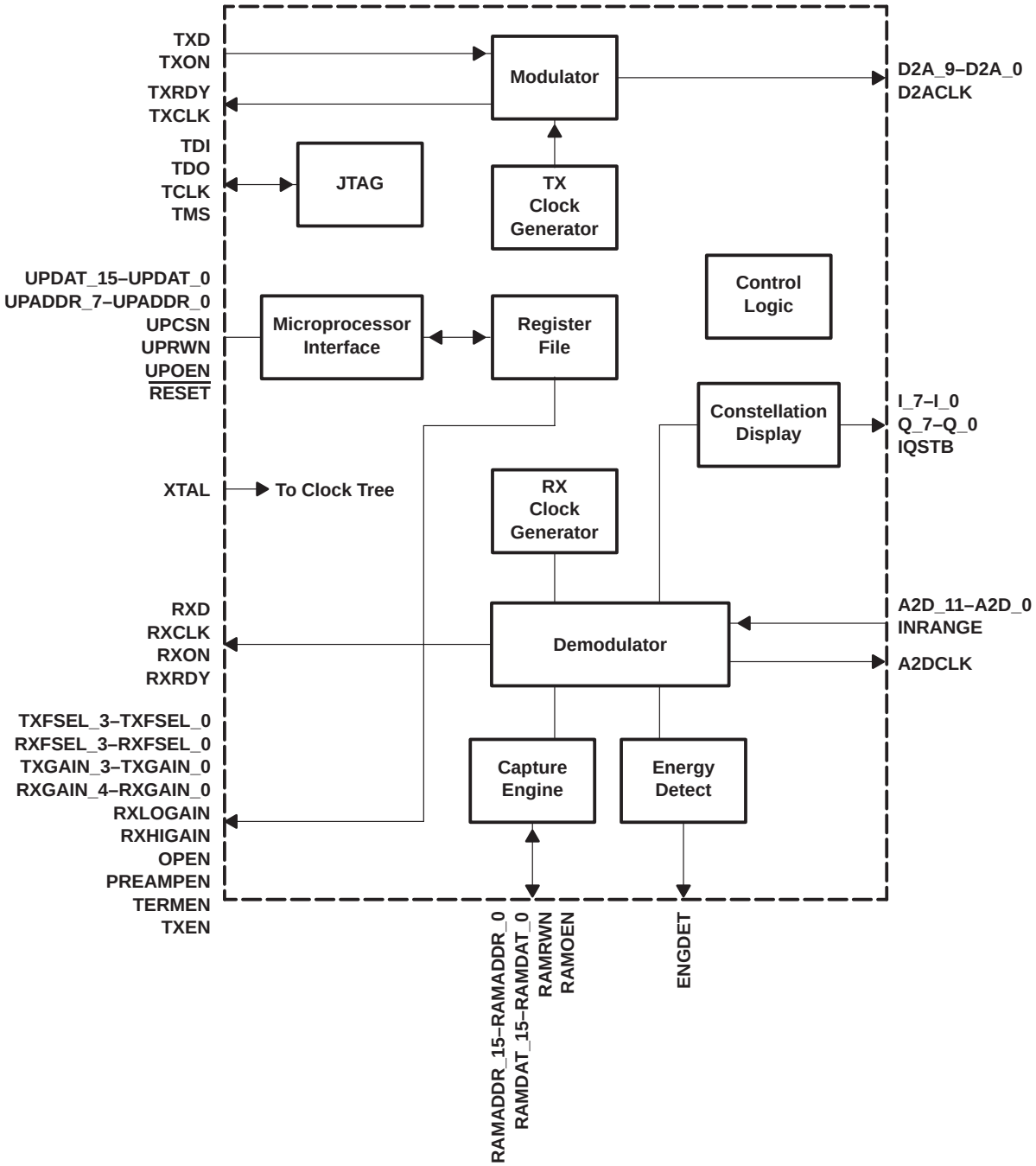


Figure 4. EtherLoop Modem Block Diagram

Terminal Functions

microprocessor

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
UPADDR_7	30	I	Bits 7–0 of the microprocessor address bus; used to address the register file.
UPADDR_6	31		
UPADDR_5	32		
UPADDR_4	33		
UPADDR_3	35		
UPADDR_2	36		
UPADDR_1	37		
UPADDR_0	38		
UPCSN	27	I	Microprocessor chip-select line (active low). UPCSN is used to initiate an access to the register file.
UPDAT_15	2	I/O	Bits 15–0 of the microprocessor data bus; used to communicate with the register file.
UPDAT_14	3		
UPDAT_13	5		
UPDAT_12	6		
UPDAT_11	8		
UPDAT_10	9		
UPDAT_9	11		
UPDAT_8	12		
UPDAT_7	14		
UPDAT_6	15		
UPDAT_5	17		
UPDAT_4	18		
UPDAT_3	20		
UPDAT_2	21		
UPDAT_1	23		
UPDAT_0	24		
UPOEN	28	I	Microprocessor output-enable line (active low). UPOEN enables the output onto the data bus.
UPRWN	26	I	Microprocessor read/write line. UPRWN is used to differentiate between reads and writes to the register file.

† I = input, O = output

system

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
$\overline{\text{RESET}}$	45	I	System reset. If RESET is set low, it sets all flip-flops to initial state.
XTAL	42	I	System clock. Frequency is 80 MHz, 50% duty cycle.

† I = input, O = output

Terminal Functions (Continued)

serial loop communications

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
RXCLK	194	O	Receive clock. RXCLK is driven by the TNETEL1200 to clock receive data into the microprocessor.
RXD	198	O	Receive data. RXD is the data from the TNETEL1200 from the loop being sent to the microprocessor.
RXON	206	I	Receive on. RXON is driven by the microprocessor to enable the TNETEL1200 loop receiver.
RXRDY	201	O	Receive ready. RXRDY is driven by the TNETEL1200 to inform the microprocessor that the TNETEL1200 is ready for receiving data from the loop.
TXCLK	196	O	Transmit clock. TXCLK is driven by the TNETEL1200 to clock transmit data out of the microprocessor.
TXD	204	I	Transmit data. TXD is the data from the microprocessor to be driven onto the loop by the TNETEL1200.
TXON	207	I	Transmit on. TXON is driven by the microprocessor to enable the TNETEL1200 loop transmitter.
TXRDY	202	O	Transmit ready. TXRDY is driven by the TNETEL1200 to inform the microprocessor that the TNETEL1200 is ready for transmitting onto the loop.

† I = input, O = output

signal data

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
A2D_11 A2D_10 A2D_9 A2D_8 A2D_7 A2D_6 A2D_5 A2D_4 A2D_3 A2D_2 A2D_1 A2D_0	149 148 147 146 144 143 142 141 139 138 137 136	I	Bits 11–0 of the data signal values sent from the ADC in the analog loop receiver
A2DCLK	134	O	Clock. A2DCLK is used to clock the data out of the ADC.
D2A_9 D2A_8 D2A_7 D2A_6 D2A_5 D2A_4 D2A_3 D2A_2 D2A_1 D2A_0	166 165 164 162 161 160 159 155 154 153	O	Bits 9–0 of the data signal values sent to the DAC in the analog loop transmitter
D2ACLK	168	O	Clock. D2ACLK is used to clock the data into the DAC.
INRANGE	151	I	Data overflow signal from the ADC

† I = input, O = output

Terminal Functions (Continued)

capture buffer

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
RAMADDR_15	81	O	Bits 15–0 of the address path from the TNETEL1200 and the capture buffer SRAM
RAMADDR_14	82		
RAMADDR_13	84		
RAMADDR_12	85		
RAMADDR_11	87		
RAMADDR_10	88		
RAMADDR_9	90		
RAMADDR_8	91		
RAMADDR_7	93		
RAMADDR_6	94		
RAMADDR_5	96		
RAMADDR_4	97		
RAMADDR_3	99		
RAMADDR_2	100		
RAMADDR_1	102		
RAMADDR_0	103		
RAMDAT_15	54	I/O	Bits15–0 of the data path between the TNETEL1200 and the capture buffer SRAM
RAMDAT_14	55		
RAMDAT_13	57		
RAMDAT_12	58		
RAMDAT_11	60		
RAMDAT_10	61		
RAMDAT_9	63		
RAMDAT_8	64		
RAMDAT_7	66		
RAMDAT_6	67		
RAMDAT_5	69		
RAMDAT_4	70		
RAMDAT_3	72		
RAMDAT_2	73		
RAMDAT_1	75		
RAMDAT_0	76		
RAMOEN	79	O	SRAM output enable (active low). RAMOEN is the output enable from the TNETEL1200 to the capture buffer SRAM.
RAMRWN	78	O	SRAM read/write. RAMRWN is the read/write signal from the TNETEL1200 to the capture buffer SRAM.

† I = input, O = output

Terminal Functions (Continued)

analog loop control

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
OPEN	105	O	Open. Control signal to open and close link between line driver and line load.
PREAMPEN	120	O	Preamplifier enable. PREAMPEN enables the preamplifier.
RXFSEL_3 RXFSEL_2 RXFSEL_1 RXFSEL_0	113 114 115 116	O	Receiver filter. Bits 3–0 enable the receiver filter sections.
RXGAIN_4 RXGAIN_3 RXGAIN_2 RXGAIN_1 RXGAIN_0	107 108 109 110 111	O	Receiver gain. Bits 4–0 enable the receiver gain sections (1, 2, 4, 8, 16 dB).
RXHIGAIN	118	O	Receiver high gain. RXHIGAIN controls a preamplifier in the receiver.
RXLOGAIN	119	O	Receiver low gain. RXHIGAIN controls a preamplifier in the receiver.
TERMEN	121	O	Termination enable. TERMEN enables the line termination.
TXEN	122	O	Transmitter enable. TXEN enables the output transmitter sections.
TXFSEL_3 TXFSEL_2 TXFSEL_1 TXFSEL_0	129 130 131 132	O	Transmitter filter. Bits 3–0 enable the transmitter filter sections.
TXGAIN_3 TXGAIN_2 TXGAIN_1 TXGAIN_0	124 125 126 127	O	Transmitter gain. Bits 3–0 enable transmitter gain sections.

† I = input, O = output

debug

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
ENGDET	200	O	Energy detect
I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0	171 172 173 174 176 177 178 179	O	Bits 7–0 of the I component of the demodulated signal (test only)
IQSTB	181	O	IQSTB is used to clock out the I and Q data (test only).
Q_7 Q_6 Q_5 Q_4 Q_3 Q_2 Q_1 Q_0	183 184 185 186 188 189 190 191	O	Bits 7–0 of the Q component of the demodulated signal (test only)

† I = input, O = output

Terminal Functions (Continued)

design for test

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
TDI	47	I	Test data input
TDO	52	O	Test data output
TCLK	41	I	Test clock
TMS	48	I	Test mode select
TRIN	49	I	Asynchronous output pad 3-state (active low)
TRSTN	50	I	Asynchronous TAP reset (active low)

† I = input, O = output

power supply

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
GND	4, 10, 16, 22, 29, 39, 43, 46, 53, 59, 65, 71, 83, 89, 95, 101, 112, 123, 133, 140, 150, 156, 158, 167, 170, 180, 187, 193, 197, 203, 208	Digital supply return
V_{CC}	1, 7, 13, 19, 25, 34, 40, 44, 51, 56, 62, 68, 74, 80, 86, 92, 98, 104, 106, 117, 128, 135, 145, 152, 157, 163, 169, 175, 182, 192, 195, 199, 205	3.3-V core and I/O power

Table 1. Processor Interface Signal List

TERMINAL NAME	I/O†	SIGNAL
UPDAT15–UPDAT0	I/O	Microprocessor data bus
UPADDR7–UPADDR0	I	Microprocessor address bus
UPRWN	I	Microprocessor read/write enable
UPCSN	I	Microprocessor chip select (active low)
UPOEN	I	Microprocessor output enable (active low)

† I = input, O = output

Table 2. Operating Conditions (I/O Terminals)

MICROPROCESSOR

TERMINAL NAME	I/O†	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
UPDAT15–UPDAT0	I/O	Y	N	Y
UPADDR7–UPADDR0	I	Y	N	N
UPRWN	I	Y	N	N
UPCSN	I	Y	N	N

† I = input, O = output

SYSTEM

TERMINAL NAME	TYPE‡	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
XTAL	I	Y	N	N
RESET	I	Y	N	N

‡ I = input

SERIAL LOOP COMMUNICATIONS

TERMINAL NAME	I/O†	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
TXRDY	O		N	
TXCLK	O		N	
TXON	I	Y	N	N
TXD	I	Y	N	N
RXRDY	O		N	
RXCLK	O		N	
RXON	I	Y	N	N
RXD	O		N	

† I = input, O = output

Table 2. Operating Conditions (I/O Terminals) (Continued)

SIGNAL DATA

TERMINAL NAME	I/O†	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
D2A9–D2A0	O		Y	
D2ACLK	O		Y	
A2D11–A2D0	I	Y	Y	
A2DCLK	O		Y	
INRANGE	I	Y	Y	

† I = input, O = output

CAPTURE BUFFER

TERMINAL NAME	I/O†	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
RAMDAT15–RAMDAT0	I/O	Y	N	Y
RAMADDR15–RAMADDR0	O		N	
RAMRDN	O		N	
RAMOEN	O		N	

† I = input, O = output

ANALOG LOOP CONTROL

TERMINAL NAME	TYPE‡	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
RXGAIN4–RXGAIN0	O		Y	
RXFSEL3–RXFSEL0	O		Y	
RXHIGAIN	O		Y	
RXLOGAIN	O		Y	
PREAMPEM	O		Y	
TERMEN	O		Y	
TXGAIN3–TXGAIN0	O		Y	
TXFSEL3–TXFSEL0	O		Y	
RXEN	O		Y	

‡ O = output

DEBUG

TERMINAL NAME	TYPE‡	HYSTERESIS	5-V TOLERANT	3.6-V FAILSAFE
I_7–I_0	O		N	
Q_7–Q_0	O		N	
IQSTB	O		N	

‡ O = output

Table 2. Operating Conditions (I/O Terminals) (Continued)

		DESIGN FOR TEST		
TERMINAL NAME	**I/O†**	**HYSTERESIS**	**5-V TOLERANT**	**3.6-V FAILSAFE**
TDI	I	Y	N	N
TDO	O		N	
TCLK	I	Y	N	N
TMS	I	Y	N	N

† I = input, O = output

Table 3. Power Consumption (V_{CC} = 3.3 V, T_A = 25°C, R_L = 500 Ω)‡

SYMBOL	DESCRIPTION	POWER (W)§
P_{total}	Total power	1.7

‡ All I/Os have a resistive load of 75 Ω, and the source and sink current is set to 0 mA.
§ DFT circuitry is inactive.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Core supply-voltage range, V_{CC} . . . . . –0.5 V to 4.0 V
Input-voltage range, V_I: Standard TTL/LVCMOS . . . . . –0.5 V to V_{CC} + 0.5 V
3.6-V fail-safe TTL/LVCMOS . . . . . –0.5 V to 3.6 V
5-V tolerant TTL/LVCMOS . . . . . .
Output-voltage range, V_O: Standard TTL/LVCMOS . . . . . –0.5 V to V_{CC} + 0.5 V
3.6-V fail-safe TTL/LVCMOS . . . . . –0.5 V to 3.6 V
5-V tolerant TTL/LVCMOS . . . . . .
Input clamp current for TTL/LVCMOS (V_I < 0 or V_I > V_{CC}) (see Note 1) . . . . . ±20 mA
Output clamp current (V_O < 0 or V_O > V_{CC}) (see Note 2) . . . . . ±20 mA
Electrostatic discharge (100 pF, 1.5 kΩ) . . . . . 4.0 kV
Latchup immunity . . . . . >250 mA at 25°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers (for 5-V tolerant, used V_I >)
2. Applies to external output and bidirectional buffers (for 5-V tolerant, used V_O >)

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_I	Input voltage	TTL/LVCMOS	0	V_{CC}	V
		5-V tolerant TTL/LVCMOS			
V_O	Output voltage	TTL/LVCMOS	0	V_{CC}	V
		5-V tolerant TTL/LVCMOS			
V_{IH}	High-level input voltage	TTL/LVCMOS	2	V_{CC}	V
		5-V tolerant TTL/LVCMOS			
V_{IL}	Low-level input voltage	TTL/LVCMOS	0	0.8	V
		5-V tolerant TTL/LVCMOS		0.8	
t_r	Input transition (t_r and t_f) time (10% to 90%)			6	ns
T_A‡	Ambient temperature		–40	85	°C
T_J	Junction temperature (commercial specification)		–40	125	°C

‡ T_A is measured at the surface of the package. No airflow or heatsink is assumed. The maximum ambient temperature is calculated considering P_{MAX}, $R_{\theta JA}$, and T_J.

electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	V_{CC}–0.6			V
V_{OL}	High-level output voltage	I_{OL} = rated			0.5	V
V_{hys}	Hysteresis ($V_{T+} – V_{T–}$)			0.4		V
I_{IL}	Low-level input current (V_{in} = V_{IL} min)	3.6-V failsafe			±1	µA
		5-V tolerant			±20	
I_{IH}	High-level input current (V_{in} = V_{IH} max)	3.6-V failsafe			±1	µA
		5-V tolerant			±20	
I_{IZ}§	3-state output high-impedance current				±20	µA

§ 3-state or open-drain output must be in high-impedance state.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

A2D interface (see Figure 5)

NO.			MIN	MAX	UNIT
1	t_w	Pulse duration, A2DCLK high	70		ns
2	t_w	Pulse duration, A2DCLK low	70		ns
3	t_c	Cycle time, A2DCLK	150		ns
4	t_{su}	Setup time, A2D data before A2DCLK↓	10		ns
5	t_h	Hold time, A2D data after A2DCLK↓	15		ns

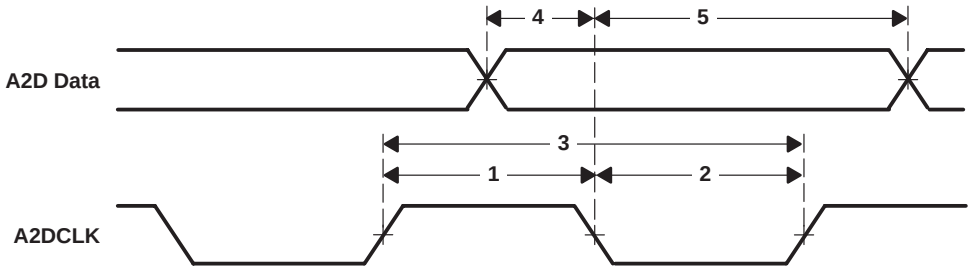


Figure 5. A2D Interface

D2A interface (see Figure 6)

NO.			MIN	MAX	UNIT
1	t_w	Pulse duration, D2ACLK high	75		ns
2	t_w	Pulse duration, D2ACLK low	25		ns
3	t_c	Cycle time, D2ACLK	100		ns
4	t_{pd}	Propagation delay time from D2ACLK↓		5	ns

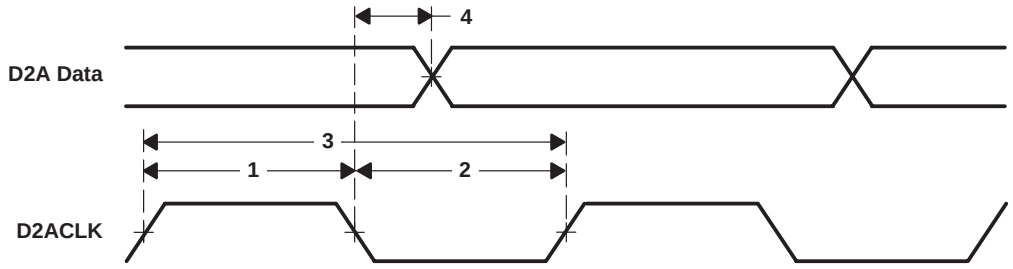


Figure 6. D2A Interface

microprocessor interface (see Figure 7)

NO.			MIN	MAX	UNIT
1	t_{su}	Setup time, UPADDR before UPCSN low – address is latched by UPCSN falling edge	2		ns
2	t_d	Delay time, read data valid after last of UPCSN and UPOEN low		20	ns
3	t_{su}	Setup time, address before UPCSN low	2		ns
4	t_{su}	Setup time, write data valid before UPWRN high	15		ns
5	t_h	Hold time, write data valid after UPWRN high	5		ns
6	t_d	Delay time, data high Z after UPOEN high		20	ns

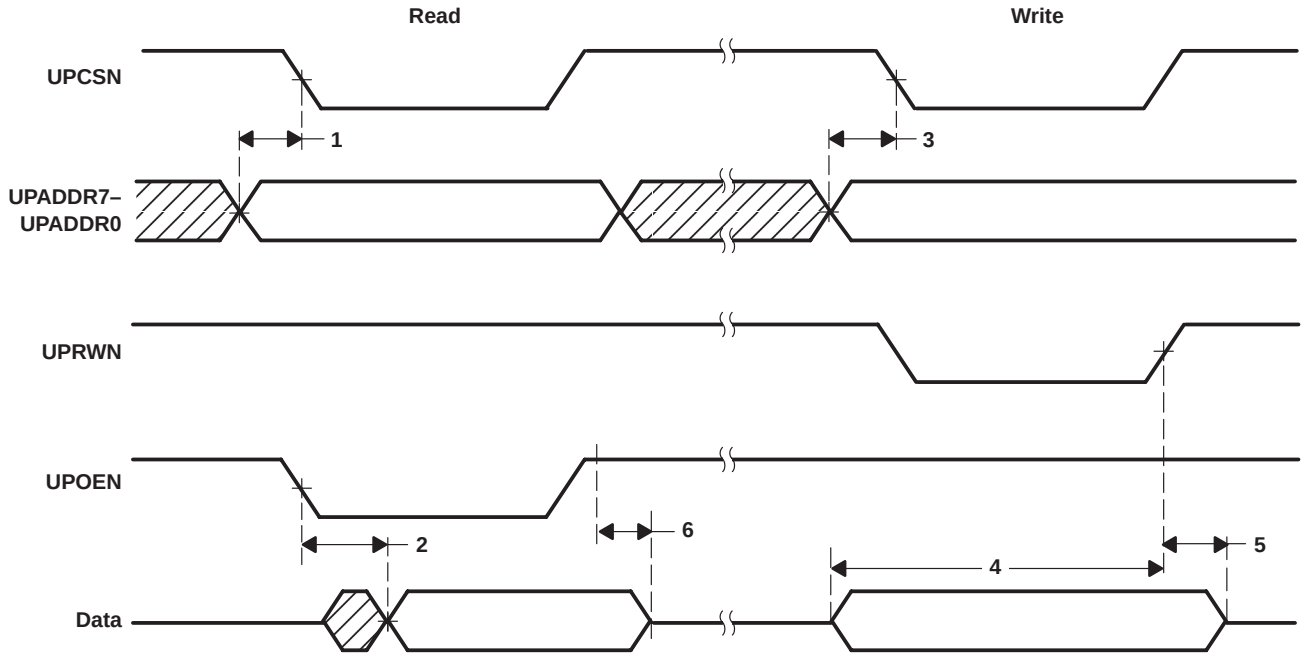


Figure 7. Microprocessor Interface

XTAL (see Figure 8)

NO.			MIN	MAX	UNIT
1	$t_{c(XTAL)}$	Cycle time, XTAL	12.5		ns
2	$t_{w(XTALH)}$	Pulse duration, XTAL high	5		ns
3	$t_{w(XTALL)}$	Pulse duration, XTAL low	5		ns

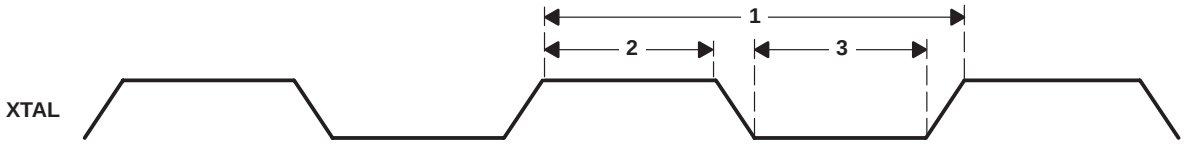


Figure 8. XTAL

HDLC INTERFACE

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

transmit and receive (see Figure 9)

NO.	PARAMETER		MIN	MAX	UNIT
1	t_h	Hold time, TXDATA after TXCLK↓	0		ns
2	t_{su}	Setup time, TXDATA before TXCLK↓	15		ns
3	t_d	Delay time, RXDATA after RXCLK		0	ns
4	t_w	Pulse duration, TXCLK high	75		ns
5	t_w	Pulse duration, TXCLK low	75		ns
6	t_w	Pulse duration, RXCLK high	100		ns
7	t_w	Pulse duration, RXCLK low	50		ns

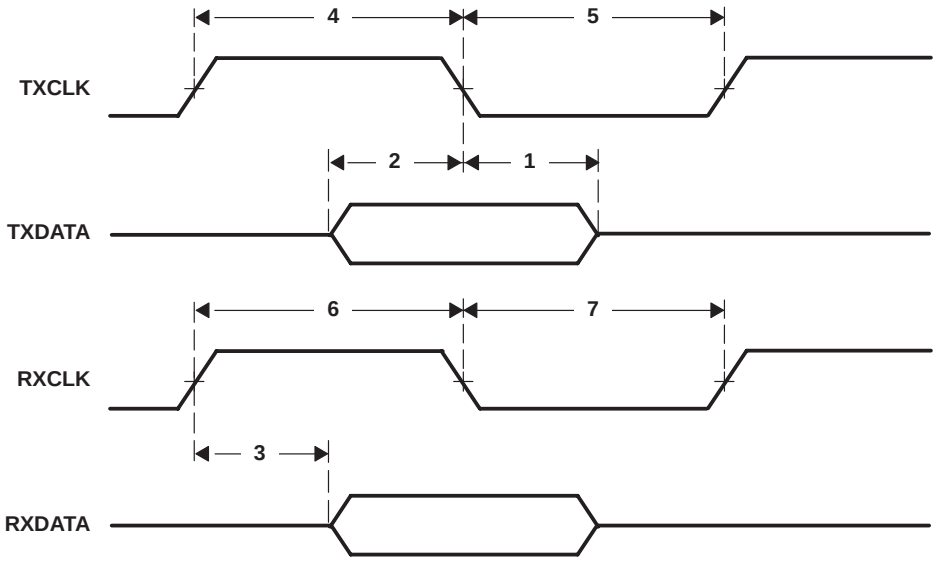


Figure 9. Transmit and Receive

CAPTURE RAM INTERFACE

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

read cycle (see Figure 10)

NO.	PARAMETER		MIN	MAX	UNIT
1	t_a	Read access time	45		ns
2	t_d	Data delay time from RAMOEN		30	ns
3	t_h	Data hold time after RAMOEN	0		ns

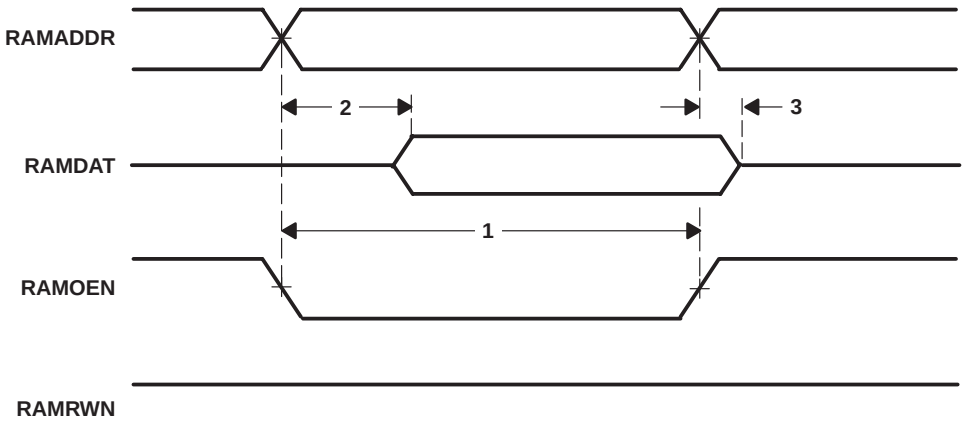


Figure 10. Read Cycle

write cycle (see Figure 11)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{su(ADDR)}$	Address setup time	70		ns
2	$t_{su(DATA)}$	Data setup time to RAMRWN	12		ns
3	t_w	Pulse width, RAMRWN low	22		ns
4	t_h	Data and address hold time after RAMRWN	30		ns

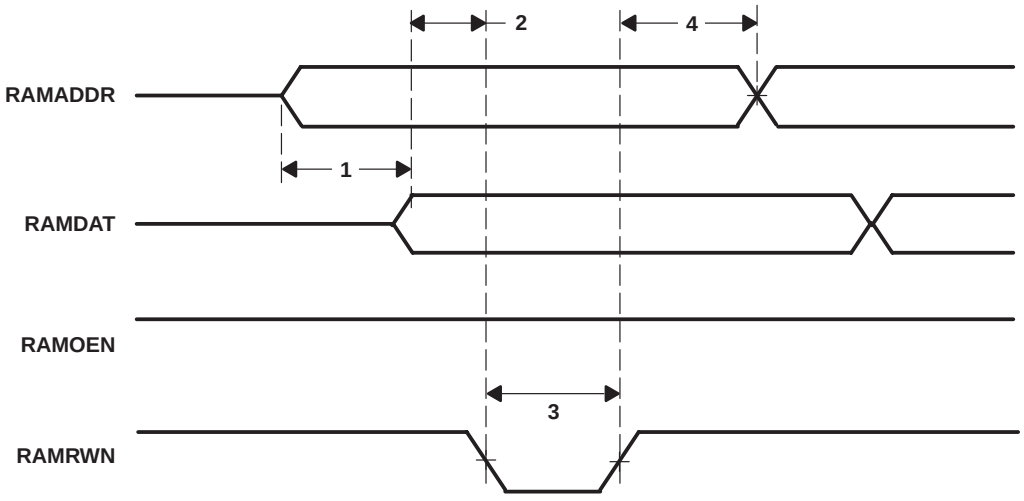
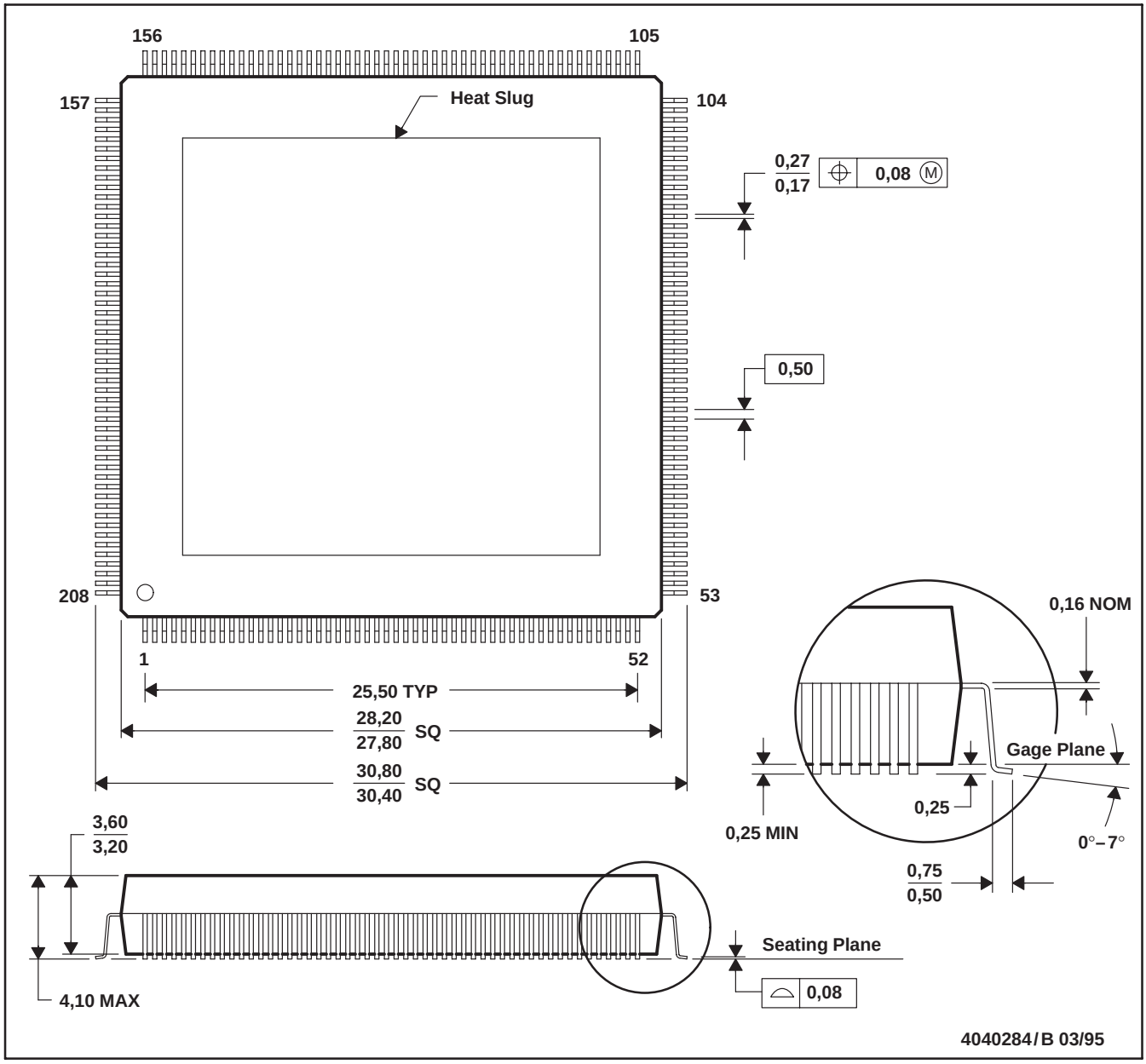


Figure 11. Write Cycle

MECHANICAL DATA

PPB (S-PQFP-G208) **PLASTIC QUAD FLATPACK (DIE-DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat slug (HSL)
D. Falls within JEDEC MO-143

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TNETEL1200PPB	OBSOLETE	HQFP	PPB	208		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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