Low noise, high drive, metastable immune, PLD — ABT22V10-7

DESCRIPTION

The ABT22V10 is a versatile PAL® device fabricated with the Philips BiCMOS process known as QUBiC. The QUBiC process produces a very high speed device (7.5ns worst case) which has excellent noise characteristics. The ground bounce, with 9 outputs switching and the 10th held low is less than 0.8V (see page 12).

The ABT22V10 is designed so the outputs can never display a metastable state due to set up and hold time violations. If set up and hold times are violated, the outputs will not glitch or display a metastable state (the propagation delays may, however, be extended).

The ABT22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-product equations. This device has a programmable AND array which drives a fixed OR array. The AND array is programmed to create custom product terms while the fixed OR array sums selected terms at the output.

The OR sum of the products feeds the "Output Macro Cell" (OMC), which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. In other words, the architecture provides maximum design flexibility by allowing the Output Macro Cell to be configured by the user.

This device is pin and JEDEC file compatible with industry standard 22V10 and can be used in all standard applications where speed is to be maximized.

FEATURES

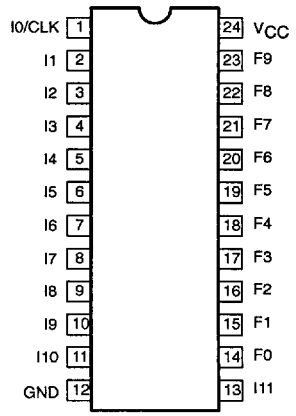
- Ultra fast 7.5ns t_{PD} and 6ns t_{CO}
- High output drive; 48mA = I_{OL} (complete specification, page 3)
- Metastable immune flip-flops, τ = 83pS (complete specification, page 9)
- Low ground bounce (<0.8V)
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Power-up reset on all registers
- Synchronous Preset/Asynchronous Reset
- Programmable on standard PAL-type device programmers
- Design support provided using SNAP software development package and other CAD tools for PLDs

APPLICATIONS

- DMA control
- State machine implementation
- High speed graphics processing
- Counters/shift registers
- SSI/MSI random logic replacement
- High speed memory decoder

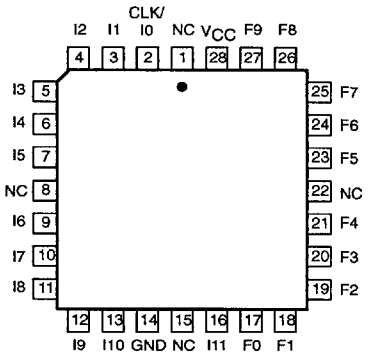
PIN CONFIGURATIONS

N Package



N = Plastic Dual In-Line Package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

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PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual-In-Line Package 300mil-wide	ABT22V10–7N	SOT222-1
28-Pin Plastic Leaded Chip Carrier	ABT22V10–7A	SOT261-3

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	–0.5	+7.0	V_{DC}
V_{IN}	Input voltage	–1.2	V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	–0.5	V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGES)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS		UNIT
			MIN	MAX	
Input voltage					
V_{IL}	Low	V_{CC} = MIN		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–1.2	V
Output voltage					
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}			
V_{OL}	Low	I_{OL} = 48mA		0.5	V
V_{OH}	High	I_{OH} = –16 mA	2.4		V
Input current					
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.40V		–10	µA
I_{IH}	High	V_{CC} = MAX, V_{IN} = 2.7V		10	µA
Output current					
		V_{CC} = MIN V_{IN} or V_{IL}			
I_{OL}	Low	V_{OL} = .5 (MAX)		48	mA
I_{OH}	High	V_{OH} = 2.4 (MIN)		–16	mA
		V_{CC} = MAX			
I_{OZH}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 2.7V		100	µA
I_{OZL}	Output leakage[2]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 0.4V		–100	µA
I_{SC}	Short circuit[3]	V_{OUT} = 0.5 V	–30	–190	mA
I_{CC}	V_{CC} supply current	V_{CC} = MAX		185	mA

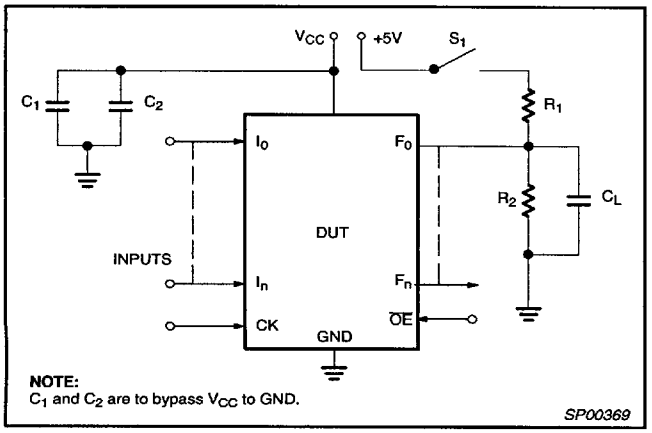
NOTES:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS[1]			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output[2, 4]	Active-LOW		3.5		7.5	
		Active-HIGH		3.5		7.5	ns
t_S	Setup time from input, feedback or SP to Clock			5.5			ns
t_H	Hold time			0			ns
t_{CO}	Clock to output4, [7]			3.0		6.0/6.5	ns
t_{CF}	Clock to feedback[3]					2.5	ns
t_{AR}	Asynchronous Reset to registered output					10.0	ns
t_{ARW}	Asynchronous Reset width			7.5			ns
t_{ARR}	Asynchronous Reset recovery time			5.5			ns
t_{SPR}	Synchronous Preset recovery time			5.0			ns
t_{WL}	Width of Clock LOW			3.0			ns
t_{WH}	Width of Clock HIGH			3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4,7]			87/83			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			125			MHz
t_{EA}	Input to Output Enable[5]					7.5	ns
t_{ER}	Input to Output Disable[5]					7.5	ns
Capacitance[6]							
C_{IN}	Input Capacitance (Pin 1)	V_{IN} = 2.0V	V_{CC} = 5.0V		6		pF
	Input Capacitance (Others)	V_{IN} = 2.0V	T_{amb} = 25°C		6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V	f = 1MHz		8		pF

NOTES:
1. Commercial Test Conditions: $R_1 = 300\Omega$, $R_2 = 390\Omega$ (see Test Load Circuit).
2. t_{PD} is tested with switch S_1 closed and C_L = 50pF (including jig capacitance). V_{IH} = 3V, V_{IL} = 0V, V_T = 1.5V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
7. For PLCC package, t_{CO} = 6.0ns; for DIP package, t_{CO} = 6.5ns

TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

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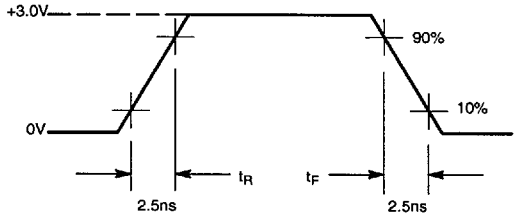
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

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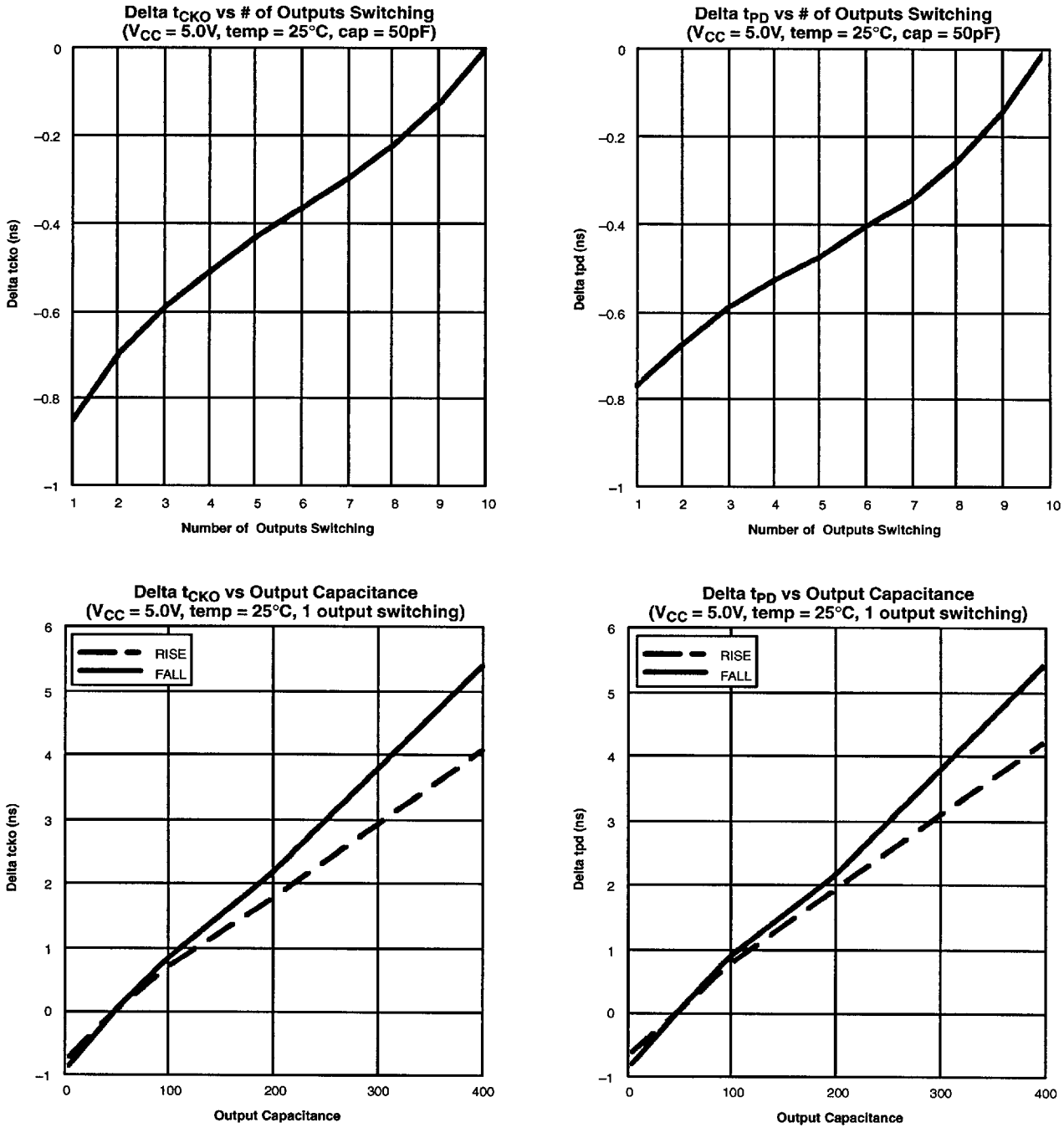
TIMING CHARACTERIZATION



The timing characterization represents the average values of a representative sample for each parameter. The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design. Philips guarantees the MAX AC CHARACTERIZATION specifications.

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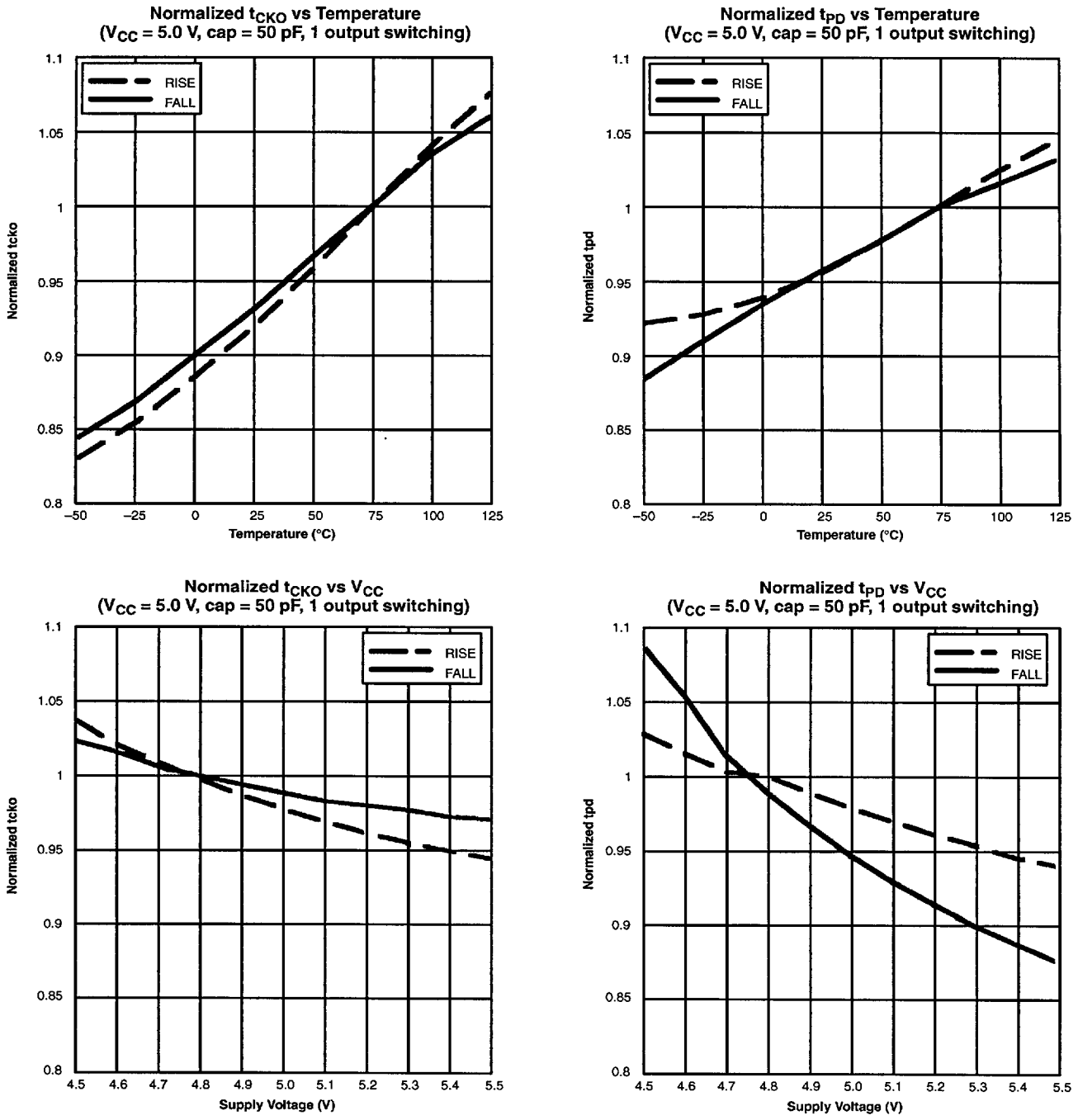
Figure 1. Device Characterization

TIMING CHARACTERIZATION



The timing characterization represents the average values of a representative sample for each parameter. The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design. Philips guarantees the MAX AC CHARACTERIZATION specifications.

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Figure 1. Device Characterization (continued)

PRODUCT FEATURES

Metastable Immune Flip-flops

The D-type flip-flops have been designed such that the outputs will not glitch or display an output anomaly if the input set up or hold times are violated. Based on a τ of 83pS, and sampling the output 8ns after the clock edge, the typical MTBF is 104 years. If the sample is taken 8.5ns after the clock, the MTBF is 43,095 years. (See page 11.)

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process produces exceptional noise immunity. The typical ground bounce, with 9 outputs simultaneously switching and the 10th output held low, is less than 0.8V. (See page 12.)

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Parity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$). (See page 15.)

Preset/Reset

For initialization, the ABT22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected. (See page 16.)

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the ABT22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10µs maximum. (See page 18.)

Security Fuse

After programming and verification, a ABT22V10 design can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The ABT22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS ABT22V10 is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0µm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The ABT22V10-7 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the ABT22V10-7 architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Support material)* of the1994 PLD data handbook for additional information.

OUTPUT REGISTER PRELOAD

The register on the ABT22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired sate. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 5.0V ± 0.25V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

PHILIPS ABT FEATURES

The ABT22V10-7 is the first in a complete family of 22V10s targeted to meet the high performance needs of the design community. In addition to the high speed characteristics of the devices, Philips has designed the devices with advanced features to ensure high system reliability.

The ABT22V10-7 is the only programmable device that guarantees metastable immunity while providing high drive and low noise.

The ABT22V10A55 and ABT22V10A7 offer high performance with live insertion capability, as well as high drive and low noise. Live insertion refers to the ability of the outputs to remain 3-Stated during power supply ramp. This is a key feature for many telecom applications, where boards are inserted into powered–up systems. System integrity is maintained as the device powers up in a well-defined manner.

	ABT22V10-7	ABT22V10A5	ABT22V10A7
Live Insertion	NO	YES	YES
Dual Verify	NO	YES	YES
Metastability	Immune	NO	NO
Source Drive Capability	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)	16mA (V_{OH} = 2.4V)
Sink Drive Capability	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)	48mA (V_{OL} = 0.5V)
Low Ground Bounce	YES	YES	YES
Package Availability:			
Plastic Dual In-line (N)	24-Pin	not available	not available
Plastic Leaded Chip Carrier (A)	28-Pin	28-Pin	28-Pin
Pinout	Standard	Evolutionary	Evolutionary

Metastable Immune Characteristics

What is metastable immunity?

Philips Semiconductors uses the term 'metastable immune' to describe a combination of two characteristic features. The first is a patented Philips circuit that prevents the outputs from glitching, oscillating, or remaining in the linear region under any circumstances, including setup and hold time violations. The second is the flip-flop's inherent ability of resolving the metastable condition.

For example, using a non-metastable immune device, a typical metastabel condition could result by running two independent signal genrators (see Figure 2) at nearly the same frequency (in this case 10MHz clock and 10.02MHz data). This device-under-test can often be driven into a metastable state. If the Q outut is used to trigger a digital scope set to infinite persistence, the $\overline{Q}$ output will build a waveform.

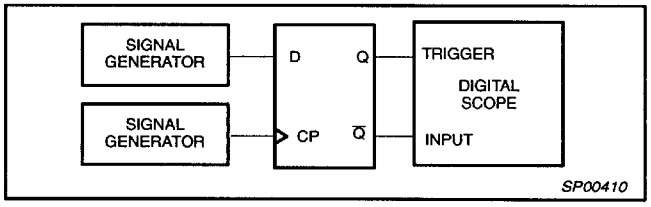


Figure 2. Test Set-up

Figure 3 shows that for a non-metastable immune device, the $\overline{Q}$ output can vay in time with respect to the Q trigger point. this also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be erified on an analog scope with a charge plate CRT. Of even greater interest are the dots running along the 3.5V volt line in the upper right-hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, the waveform will appear as in Figure 4. The output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flip-flop, the only outward manifestation of the event will be an increased clock-to-Q delay. This delay is a function of the metastability characteristics of the device, defined by τ and T_0 as described in the Design Example that follows. Since the outputs never glitch, oscillate, or remain in the linear region, the only metastable failure that can propagate further into the system is when the next flip-flop in the system samples the ABT22V10-7's outut at recisely the same time it is making a logic transition. By allowing sufficient time for any increased clock-to-Q delay, propagation of metastable failures can be avoided. The following design example illustrates this concept.

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS

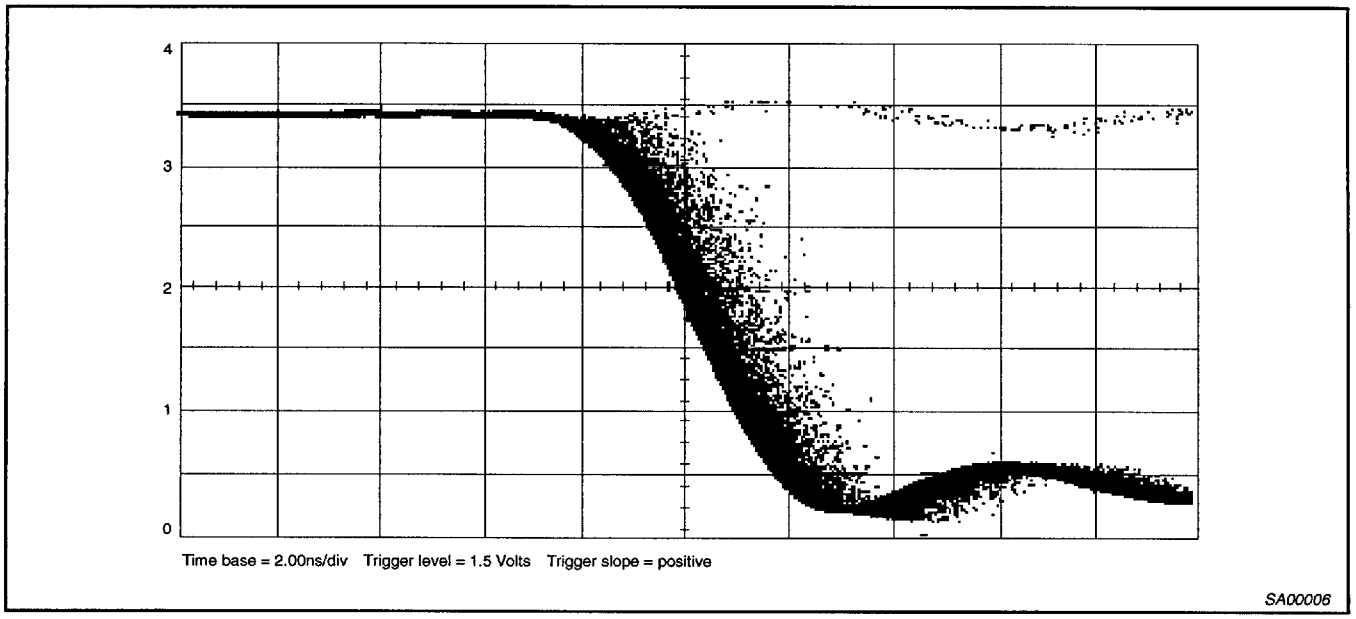


Figure 3. Non-immune $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

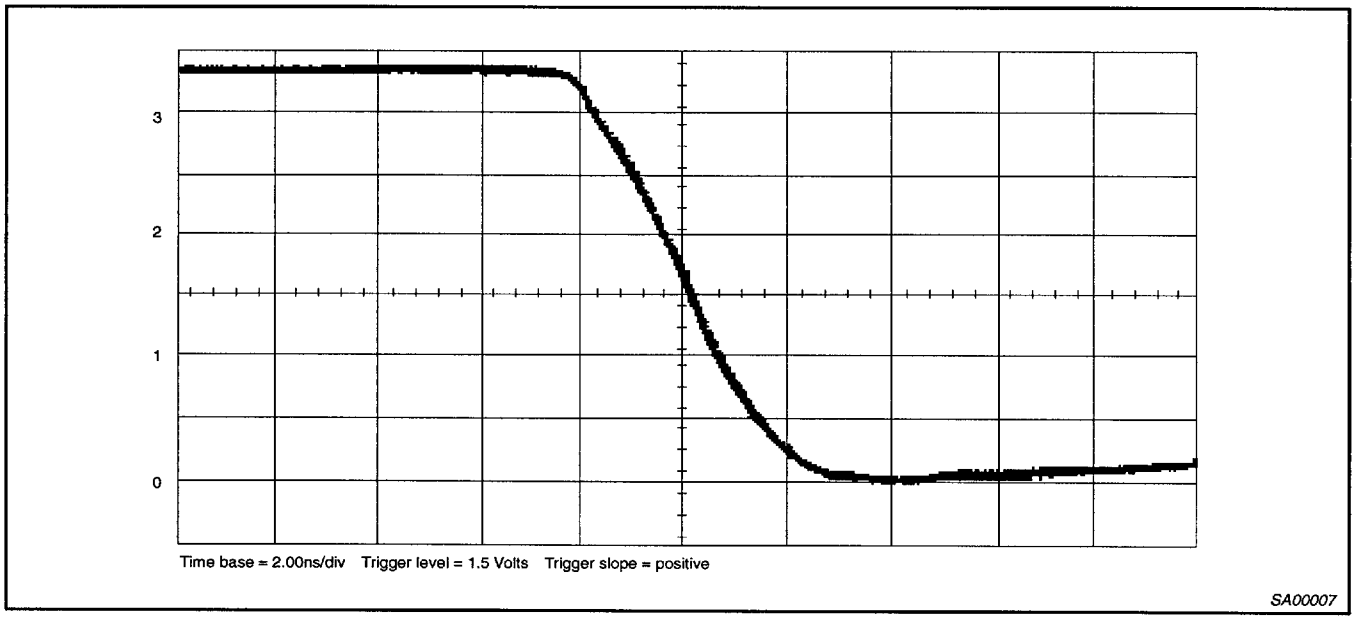


Figure 4. Metastable Immune $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

Design Example

Suppose a designer wants to use the ABT22V10-7 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), in a 5V system that has a clock frequency of 50MHz, at an ambient temperature of 25°C. She has decided that she would like to sample the output of the ABT22V10 8.5ns after the clock edge to ensure that any clock-to-Q delays that were the result of the ABT22V10 internal metastability resolution circuitry have completed and the outputs have transitioned. The MTBF for this situation can be calculated by using the equation below:

$$MTBF = \frac{e^{\left(\frac{t'}{\tau}\right)}}{T_0 F_C F_I}$$

In this formula, F_C is the frequency of the clock, F_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_0 and τ are derived from tests and can most nearly be defined as follows:

τ is a function of the rate at which a latch in a metastable state resolves that condition.

T_0 is a function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a normalization constant which is a very stron function of the normal propagation delay of the device.

In this situation, the F_I will be twice the data frequency, or 20MHz, because input events consist of both low and high transitions. Thus, in this case, F_C is 50MHz, F_I is 20MHz, τ is 83ps, t' is 8.5ns, and T_0 is 2.2×10^{17} seconds. Using the above formula, the actual MTBF for this situation is 1.36×10^{12} seconds, or 43,095 years for the ABT22V10-7.

ABT22V10–7 VALUES FOR τ AND T_0

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	83ps	8.1×10^{18} sec	82ps	7.5×10^{18} sec	101ps	3.0×10^{12} sec
5.0V	80ps	4.0×10^{18} sec	83ps	2.2×10^{17} sec	98ps	4.4×10^{11} sec
4.5V	85ps	3.4×10^{14} sec	91ps	2.5×10^{12} sec	106ps	1.1×10^{8} sec

Summary

The Philips ABT22V10-7 has on-chip circuitry that completely eliminates any output glitches, oscillations, or other output anomalies associated with metastable conditions. For outputs that are then used to generate clocks, control signals or other asynchonous data, this represents an unparalled level of reliability in a PLD. In addition, a complete set of metastability data is provided, which allows designers the ability to design extremely robust systems where data is synchronously pipelined.

LOW NOISE

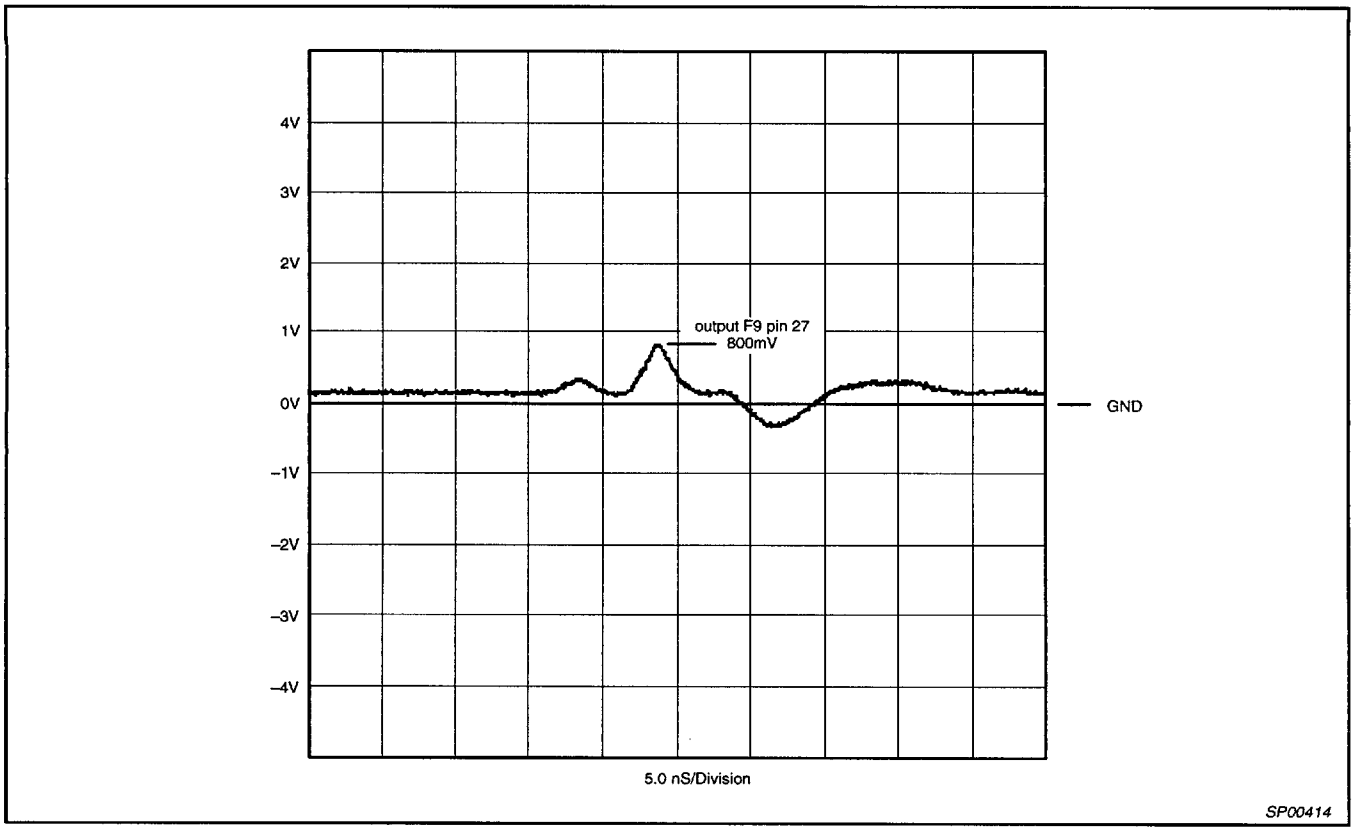


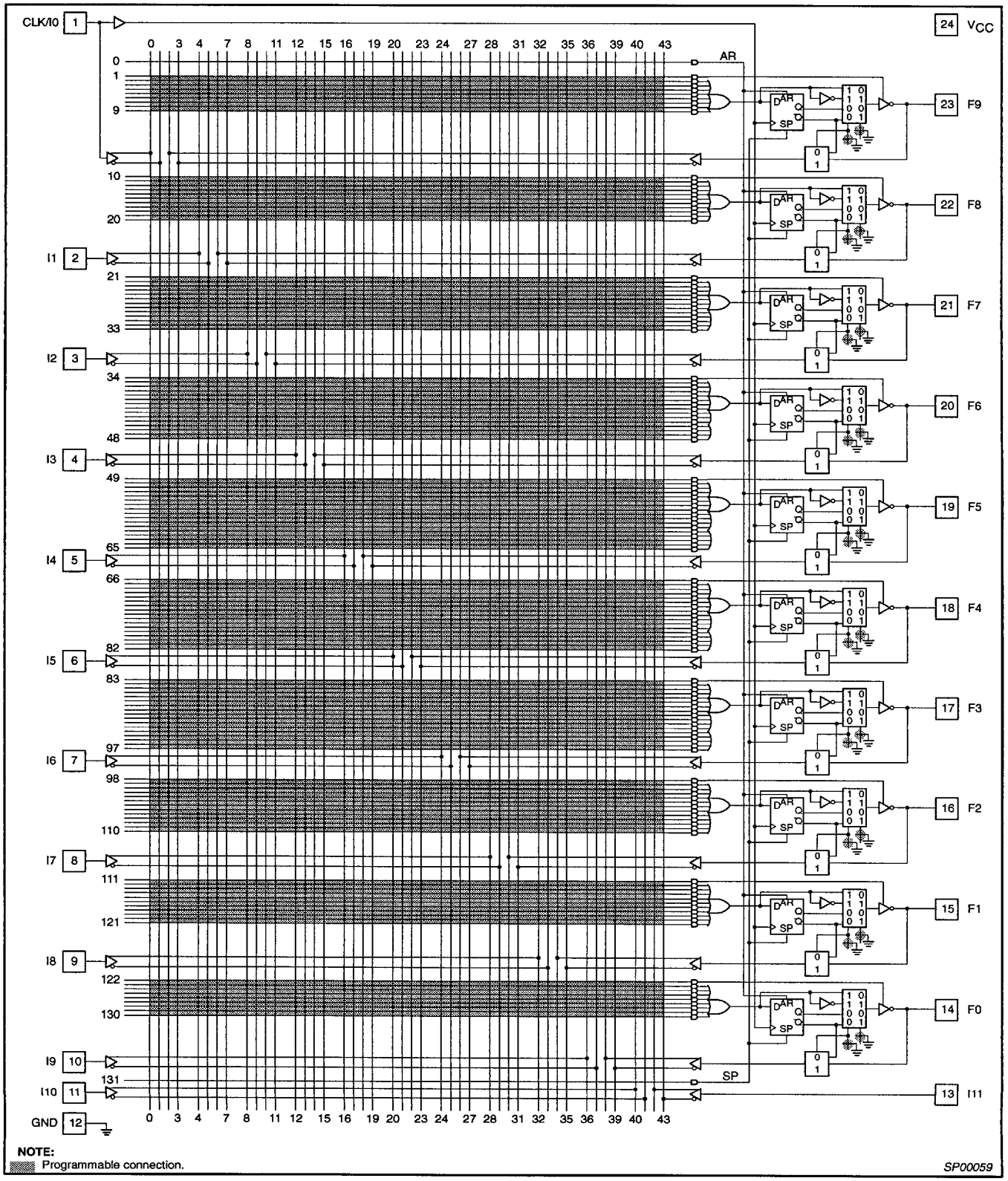
Figure 5. Device Characterization

Ground Bounce

Figure 5 shows the low ground (V_{OLP}) bounce (0.8V) observed on the 10th output of the ABT22V10 under the following conditions: 9 remaining outputs switching, each driving 50pF loads, in PLCC non-socketed device, at 5.25V, 25°C. Similar testing of comparable EECMOS 22V10 devices resulted in ground bounce in the 1.5 – 2.0V range.

At Philips the utilization of our advanced BiCMOS process, QUBiC, enables the production of high performance devices with the lowest output noise to ensure first pass system reliability. Quiet your concerns on ground bounce with Philips ABT22V10-7.

LOGIC DIAGRAM



NOTE:
Programmable connection.

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FUNCTIONAL DIAGRAM

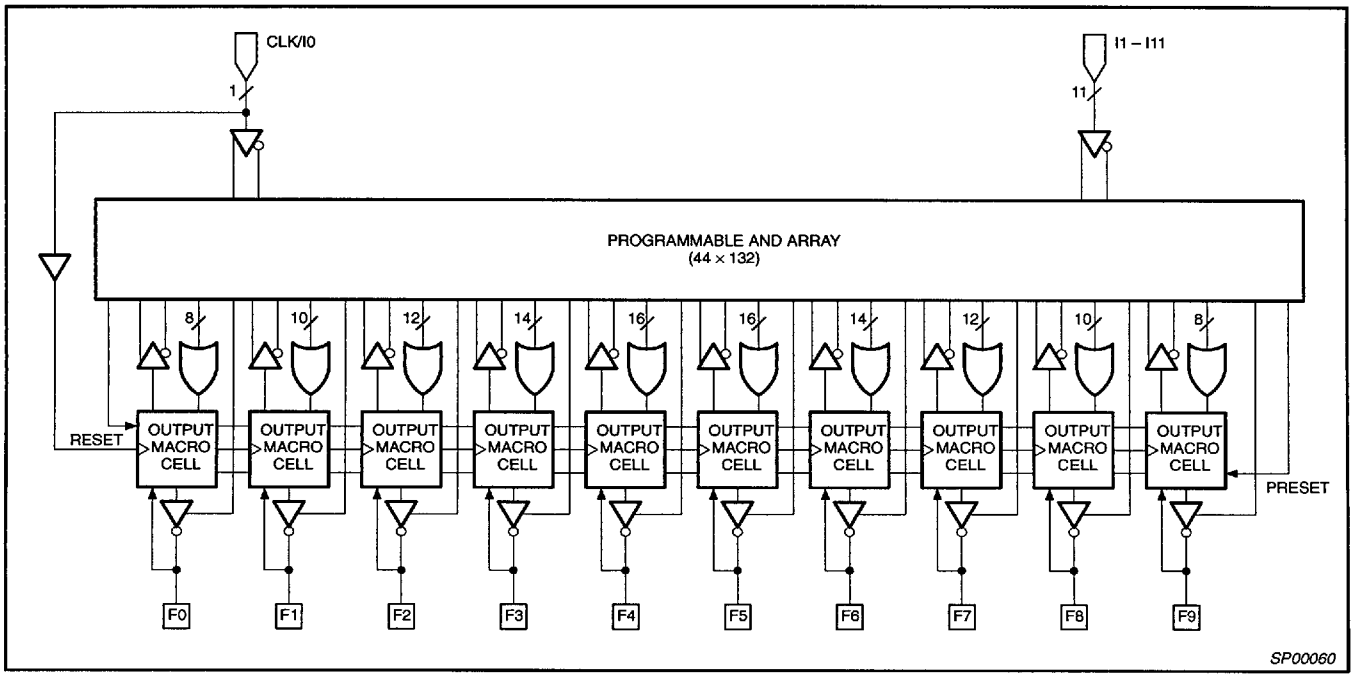


Figure 6. Functional Diagram

FUNCTIONAL DESCRIPTION

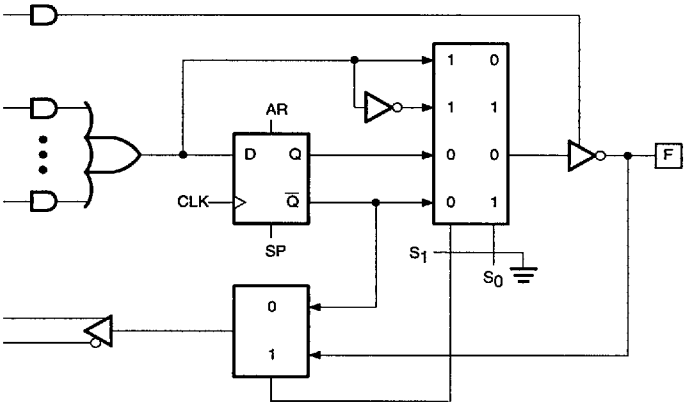
The ABT22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The ABT22V10 has 12 inputs and 10 I/O Macro Cells (Figure 6). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 7). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test fuses are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve parametric correlation.

OUTPUT MACRO CELL

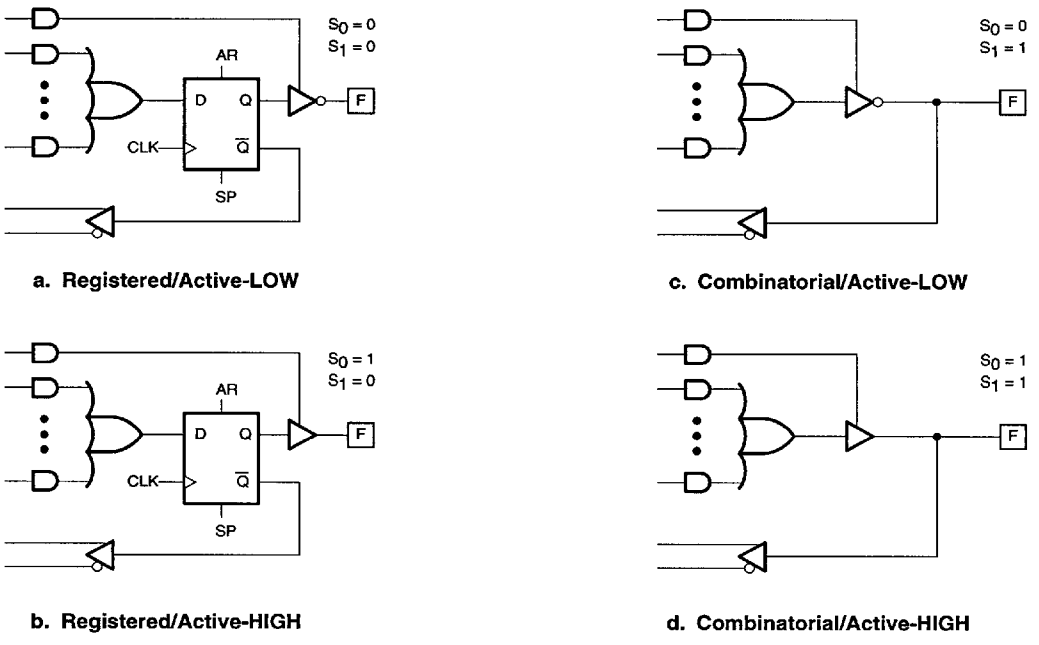


S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

SP00375

Figure 7. Output Macro Cell Logic Diagram



SP00376

Figure 8. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the ABT22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

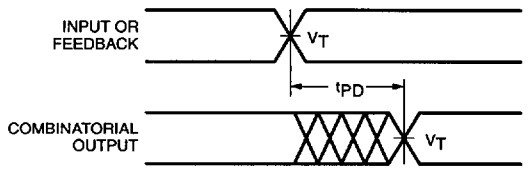
Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

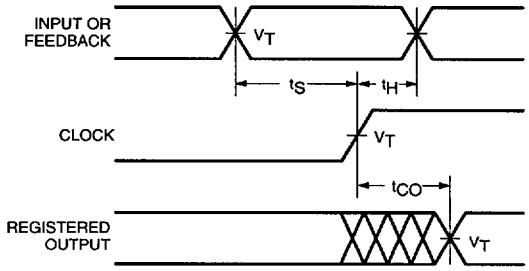
Variable Input/Output Pin Ratio

The ABT22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

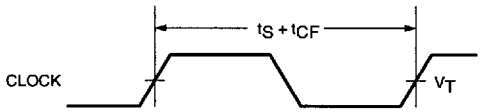
SWITCHING WAVEFORMS



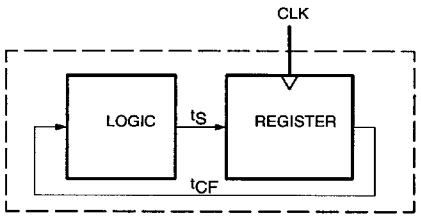
Combinatorial Output



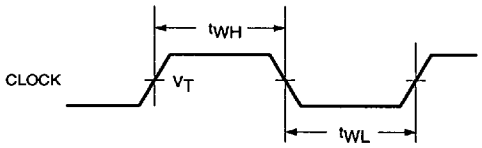
Registered Output



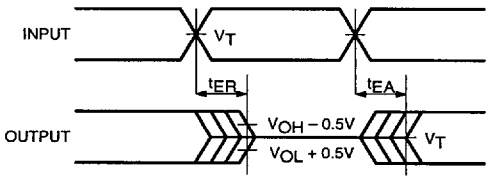
Clock to Feedback (f_{MAX} Internal)
(See Path at Right)



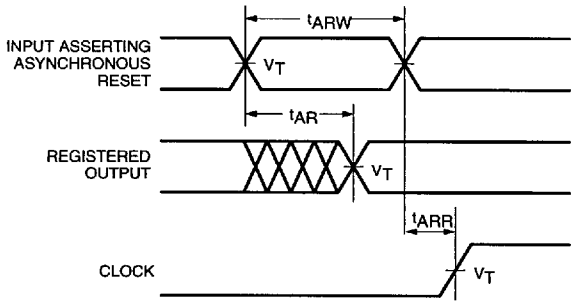
Clock to Feedback



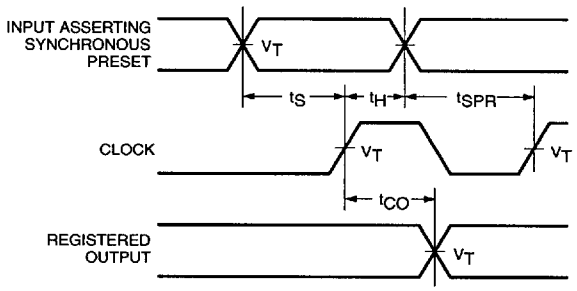
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

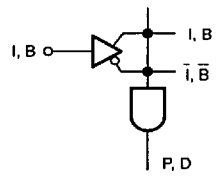


Synchronous Preset

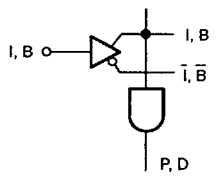
SP00377

NOTES:
1. $V_T = 1.5V$.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.5ns max.

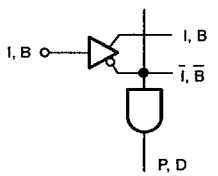
"AND" ARRAY – (I, B)



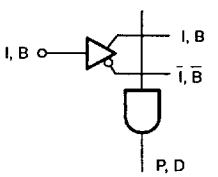
STATE	CODE
INACTIVE[1]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L



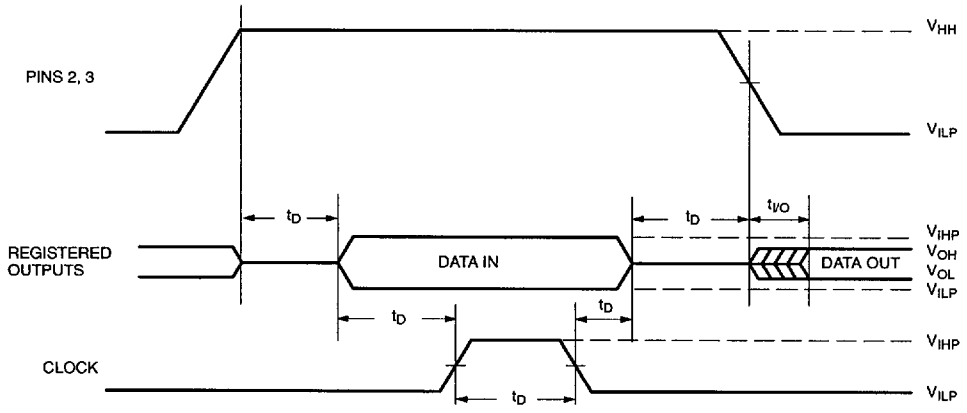
STATE	CODE
DON'T CARE	—

SP00008

NOTE:
1. This is the initial state.

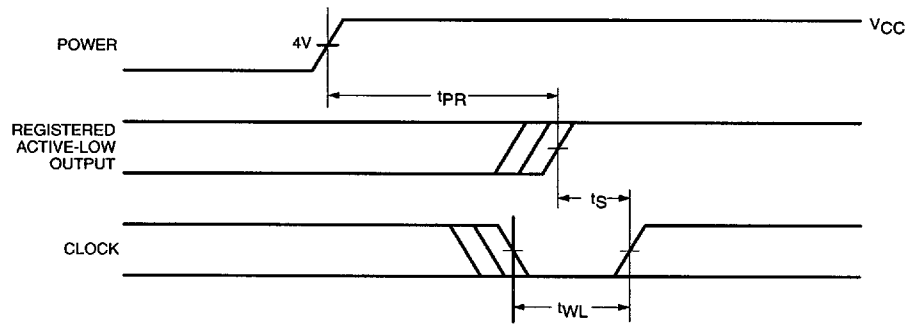
PRELOAD SET-UP

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILP}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



Output Register Preload Waveform

SP00373



Power-Up Reset Waveform

SP00066

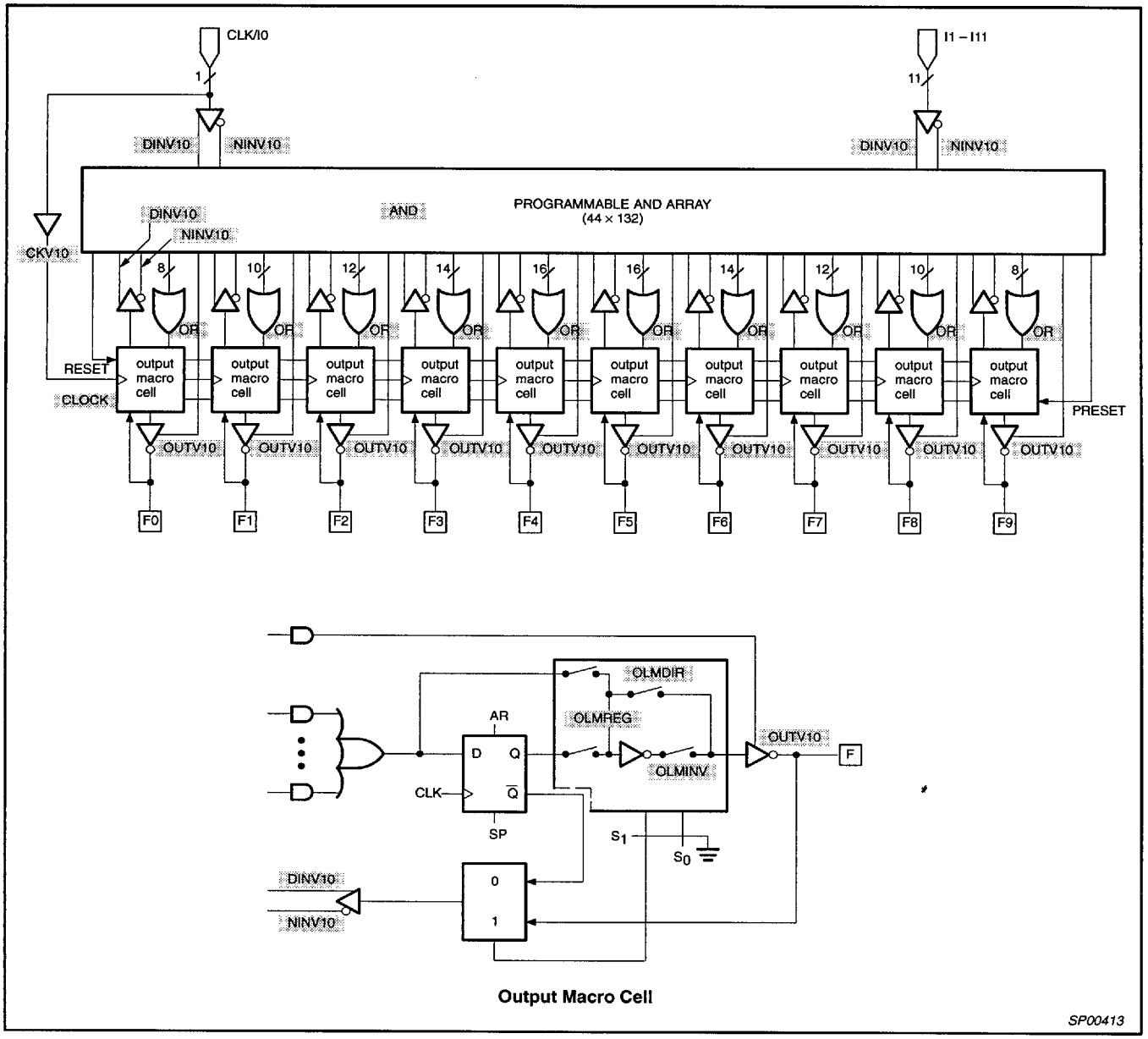
SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown above. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

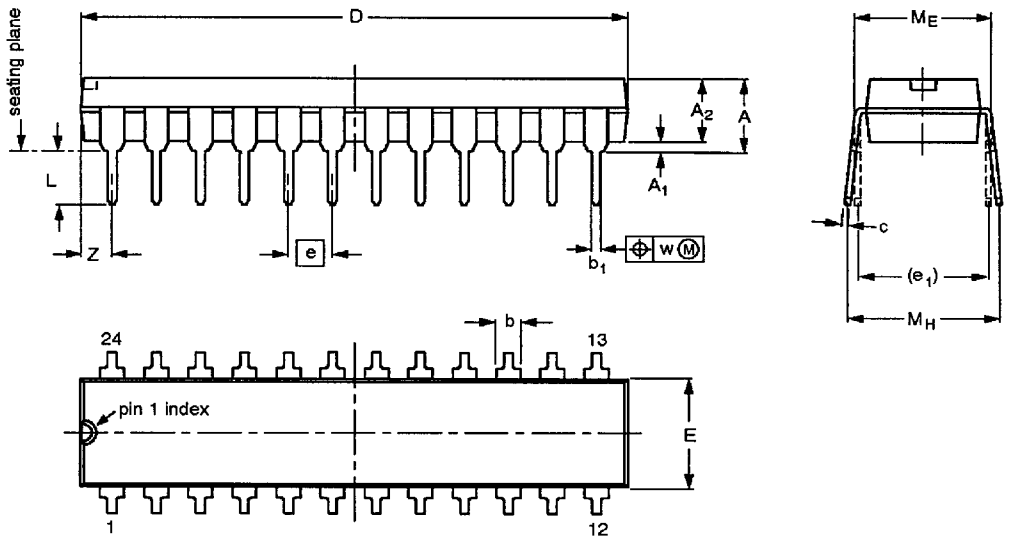
SNAP RESOURCE SUMMARY DESIGNATIONS

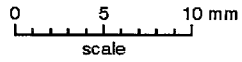


Output Macro Cell

SP00413

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

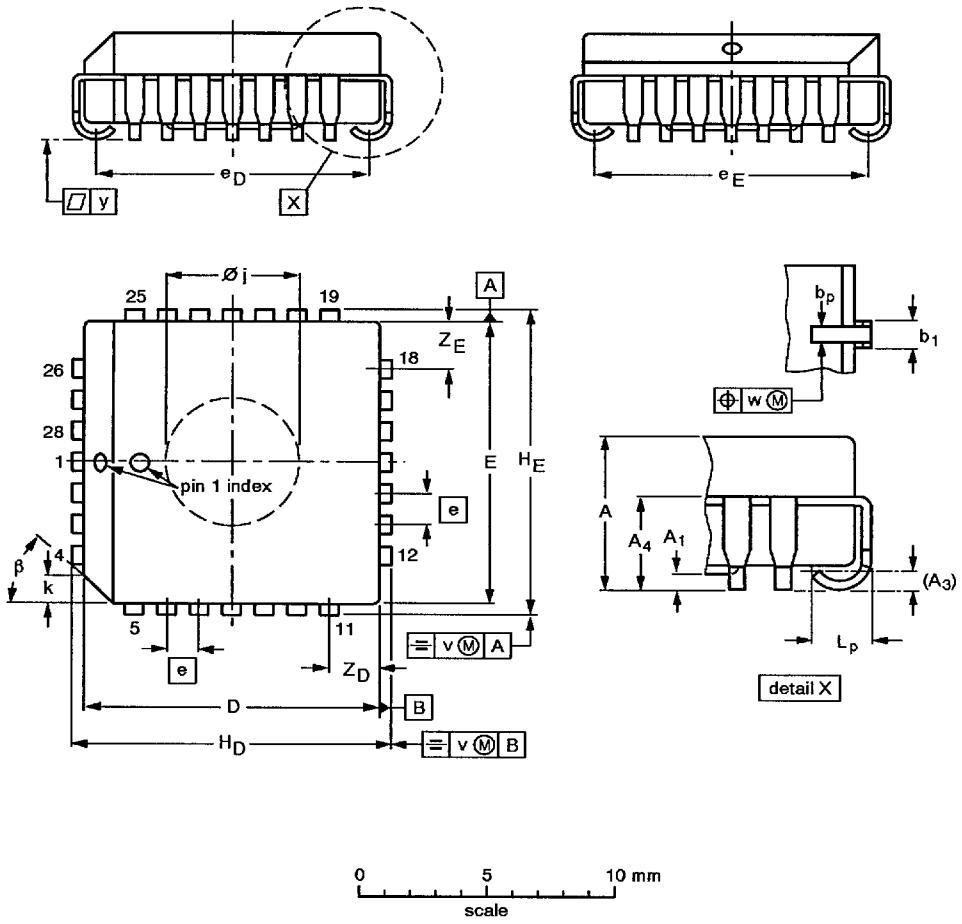
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

PLCC28: plastic leaded chip carrer; 28 leads; pedestal SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~92-11-17~~ 95-02-25