TRS208 5V Multichannel RS-232 Line Driver and Receiver with ±15kV ESD Protection

1 Features

- ESD Protection for RS-232 I/O pins
  - ±15kV Human-Body Model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates at 5V V_{CC} supply
- Four drivers and four receivers
- Operates up to 120kbit/s
- External capacitors: 4 × 0.1µF
- Latch-up performance exceeds 100mA per JESD 78, class II

2 Applications

- Battery-powered systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment

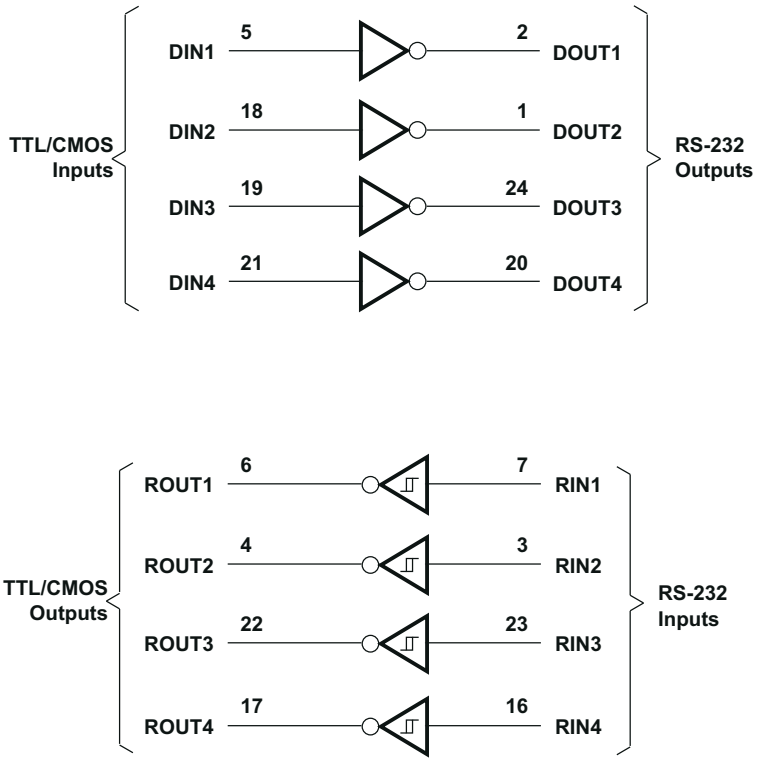
3 Description

The TRS208 device consists of four line drivers, four line receivers, and a dual charge-pump circuit with ±15kV HBM ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The devices operate at data signaling rates up to 120kbit/s and a maximum of 30V/µs driver output slew rate.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRS208	DB (SSOP)	8.2 mm x 7.8mm
	DW (SOIC)	15.5mm x 10.3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Electrical Characteristics, Driver....5
5.7 Electrical Characteristics, Receiver....6
5.8 Switching Characteristics, Driver....6
5.9 Switching Characteristics, Receiver....6
6 Parameter Measurement Information....7
7 Device Functional Modes....8
8 Application and Implementation....9
8.1 Application Information....9
9 Device and Documentation Support....12
9.1 Receiving Notification of Documentation Updates....12
9.2 Support Resources....12
9.3 Trademarks....12
9.4 Electrostatic Discharge Caution....12
9.5 Glossary....12
10 Revision History....12
11 Mechanical, Packaging, and Orderable Information....12

4 Pin Configuration and Functions

DB, DW, OR NT PACKAGE
(TOP VIEW)

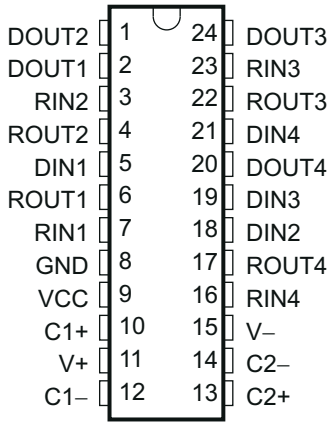


Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DB or DW		
DOUT2	1	O	RS232 line data output (to remote RS232 system)
DOUT1	2	O	RS232 line data output (to remote RS232 system)
RIN2	3	I	RS232 line data input (from remote RS232 system)
ROUT2	4	O	Logic data output (to UART)
DIN1	5	I	Logic data input (from UART)
ROUT1	6	O	Logic data output (to UART)
RIN1	7	I	RS232 line data input (from remote RS232 system)
GRD	8	-	Ground
V_{CC}	9	-	Supply Voltage, Connect to external 3V to 5.5V power supply
C1+	10	-	Positive lead of C1 capacitor
V+	11	O	Positive charge pump output for storage capacitor only
C1-	12	-	Negative lead of C1 capacitor
C2+	13	-	Positive lead of C2 capacitor
C2-	14	-	Negative lead of C2 capacitor
V-	15	O	Negative charge pump output for storage capacitor only
RIN4	16	I	RS232 line data input (from remote RS232 system)
ROUT4	17	O	Logic data output (to UART)
DIN2	18	I	Logic data input (from UART)
DIN3	19	I	Logic data input (from UART)
DOUT4	20	O	RS232 line data output (to remote RS232 system)
DIN4	21	I	Logic data input (from UART)
ROUT3	22	O	Logic data output (to UART)
RIN3	23	I	RS232 line data input (from remote RS232 system)
DOUT3	24	O	RS232 line data output (to remote RS232 system)
Thermal Pad	-	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted), see (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive charge pump voltage range(2)		V_{CC} – 0.3	14	V
V–	Negative charge pump voltage range(2)		–14	0.3	V
V_I	Input voltage range	Drivers	–0.3	V+ + 0.3	V
		Receivers (DB package)		±25	V
		Receivers (DW package)		±30	V
V_O	Output voltage range	Drivers	V– – 0.3	V+ + 0.3	V
		Receivers	–0.3	V_{CC} + 0.3	V
	Short-circuit duration	DOUT		Continuous	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) DOUT and RIN pins	±15	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See Figure 8-3 and (1)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	DIN	2			V
V_{IL}	Driver low-level input voltage	DIN			0.8	V
V_I	Driver input voltage	DIN	0		5.5	V
	Receiver input voltage (DB package)		–25		25	V
	Receiver input voltage (DW package)		-30		30	V
T_A	Operating free-air temperature	TRS208C	0		70	°C
		TRS208I	–40		85	°C

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

5.4 Thermal Information

THERMAL METRIC(1)		DB (SSOP)	DW (SOIC)	UNIT
		24-Pins	24-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.0	46	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.8	54.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.0	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-3)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
I_{CC}	Supply current	No load,	V_{CC} = 5V,	T_A = 25°C		11	20	mA

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8-3)

PARAMETER		TEST CONDITIONS(3)		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = GND	5	9		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND,	DIN = V_{CC}	–5	–9		V
I_{IH}	High-level input current	V_I = V_{CC}			15	200	µA
I_{IL}	Low-level input current	V_I at 0V			–15	–200	µA
I_{OS} (2)	Short-circuit output current	V_{CC} = 5.5V,	V_O = 0V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V– = 0V,	V_O = ±2V	300			Ω

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

5.7 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 8-3)

PARAMETER		TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA			3.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA					0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V,	T_A = 25°C			1.7	2.4	V
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 5V,	T_A = 25°C		0.8	1.2		V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT–}$)	V_{CC} = 5V			0.2	0.5	1	V
r_i	Input resistance	V_I = ±3V to ±25V,	V_{CC} = 5V,	T_A = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

5.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 8-3)

PARAMETER		TEST CONDITIONS[3]		MIN	TYP[1]	MAX	UNIT
	Maximum data rate	C_L = 50pF to 1000pF, One DOUT switching,	R_L = 3kΩ to 7kΩ, See Figure 6-1	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See Figure 6-1		2		µs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, All drivers loaded,	R_L = 3kΩ, See Figure 6-1		2		µs
$t_{sk(p)}$	Pulse skew[2]	C_L = 150pF to 2500pF, See Figure 6-2	R_L = 3kΩ to 7kΩ,		300		ns
SR(tr)	Slew rate, transition region (see Figure 6-1)	C_L = 50pF to 1000pF, V_{CC} = 5V	R_L = 3kΩ to 7kΩ,	3	6	30	V/µs

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

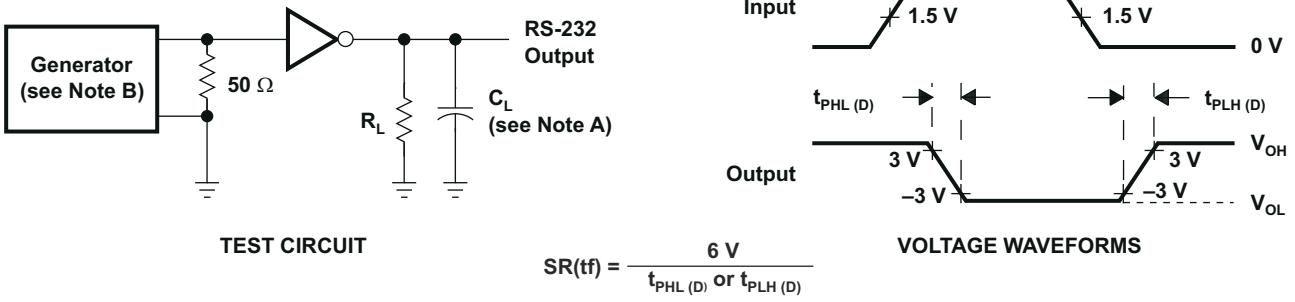
5.9 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 6-3)

PARAMETER		TEST CONDITIONS[3]	MIN	TYP[1]	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150pF		0.5	10	µs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150pF		0.5	10	µs
$t_{sk(p)}$	Pulse skew[2]			300		ns

(1) All typical values are at V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 5V ± 0.5V.

6 Parameter Measurement Information



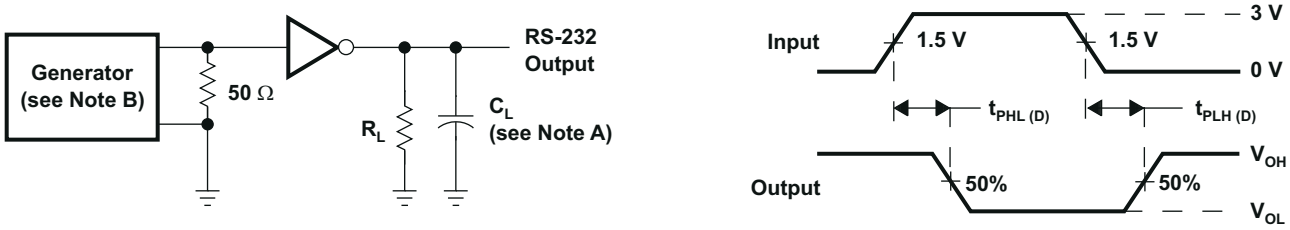
TEST CIRCUIT

$$SR(tf) = \frac{6\ V}{t_{PHL\ (D)} \text{ or } t_{PLH\ (D)}}$$

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-1. Driver Slew Rate

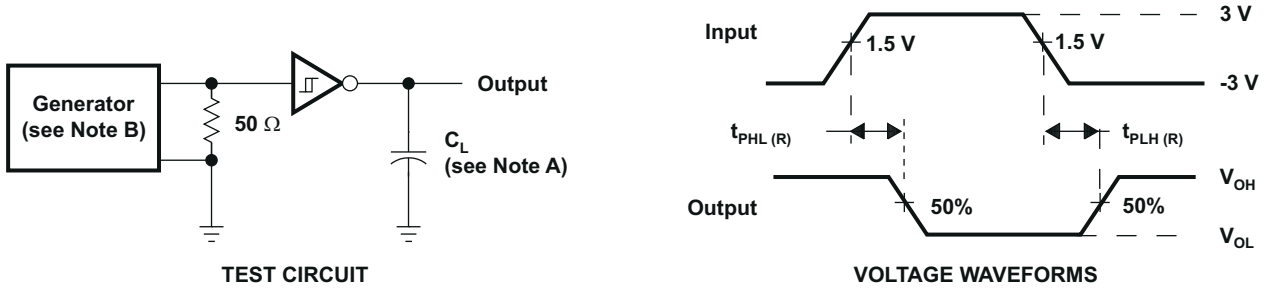


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-2. Driver Pulse Skew



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 6-3. Receiver Propagation Delay Times

7 Device Functional Modes

Function Table
Each Driver[1]

INPUT DIN	OUTPUT DOUT
L	H
H	L

(1) H = high level, L = low level

Function Table
Each Receiver[1]

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level, Open = input disconnected or connected driver off

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The TRS208 requires 0.1µF capacitors, although capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V–.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

8.1.2 Electrostatic Discharge (ESD) Protection

TI TRS208 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15kV when powered down.

8.1.3 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

8.1.4 Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 8-1, while Figure 8-2 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100pF capacitor, charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5kΩ resistor.

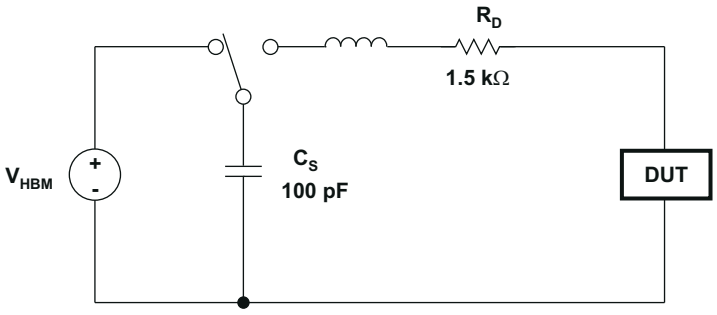


Figure 8-1. HBM ESD Test Circuit

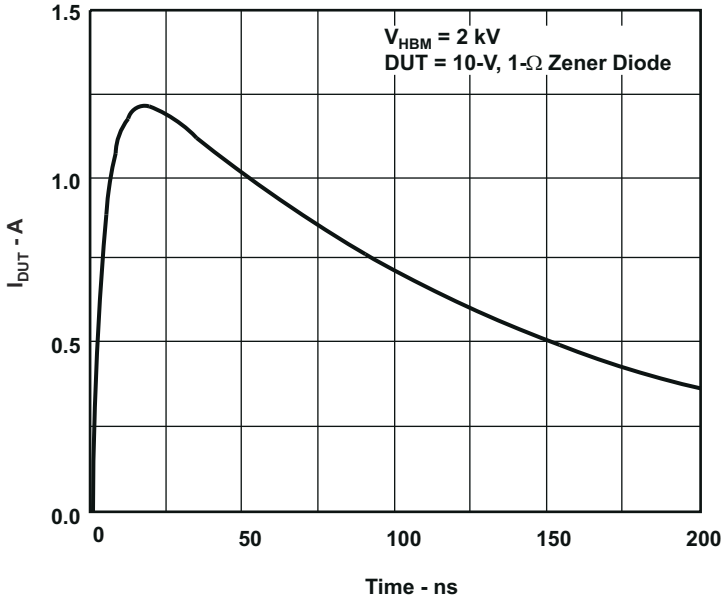
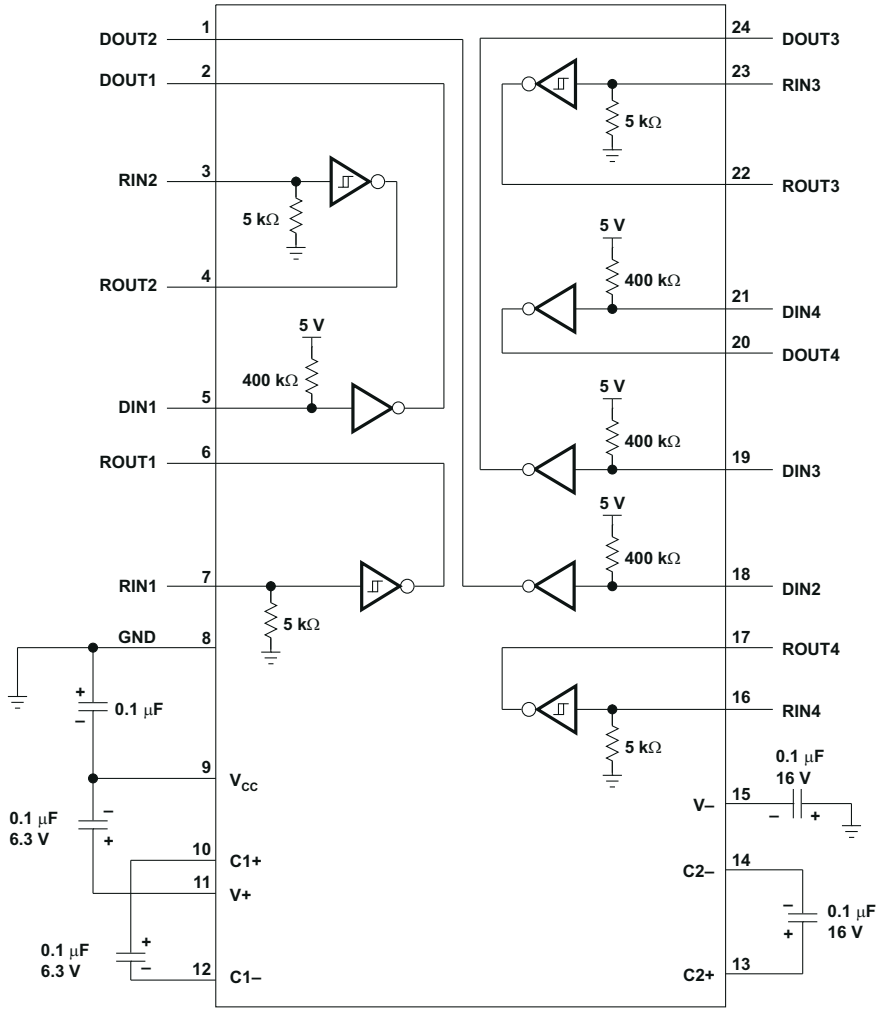


Figure 8-2. Typical HBM Current Waveform

8.1.5 Machine Model (MM)

The MM ESD test applies to all pins using a 200pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

8.1.6 Typical Application



NOTES: A. Resistor values shown are nominal.
B. Non-polarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 8-3. Typical Operating Circuit and Capacitor Values

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2007) to Revision A (July 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the DB package Input voltage range for Receivers from ±30V to ±25V in the *Absolute Maximum Ratings* and the *Recommended Operating Conditions*	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS208CDBR	Obsolete	Production	SSOP (DB) | 24	-	-	Call TI	Call TI	0 to 70	RU08C
TRS208CDWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS208C
TRS208CDWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS208C
TRS208IDB	Obsolete	Production	SSOP (DB) | 24	-	-	Call TI	Call TI	-40 to 85	RU08I
TRS208IDBR	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU08I
TRS208IDBR.A	Active	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU08I
TRS208IDWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS208I
TRS208IDWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS208I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

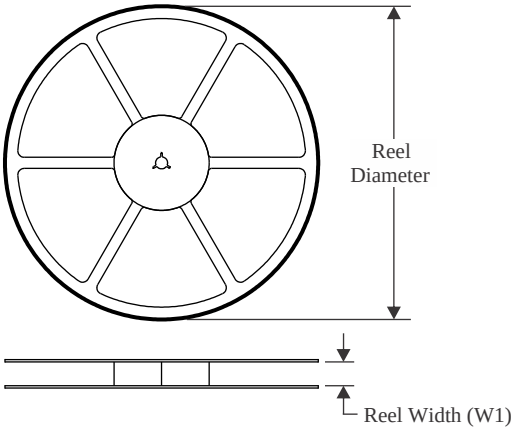
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

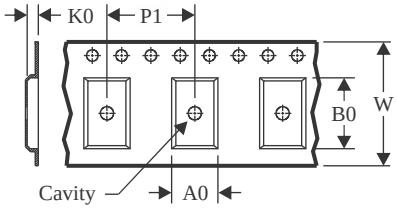
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

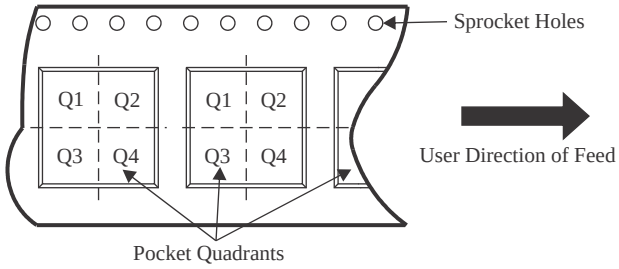


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

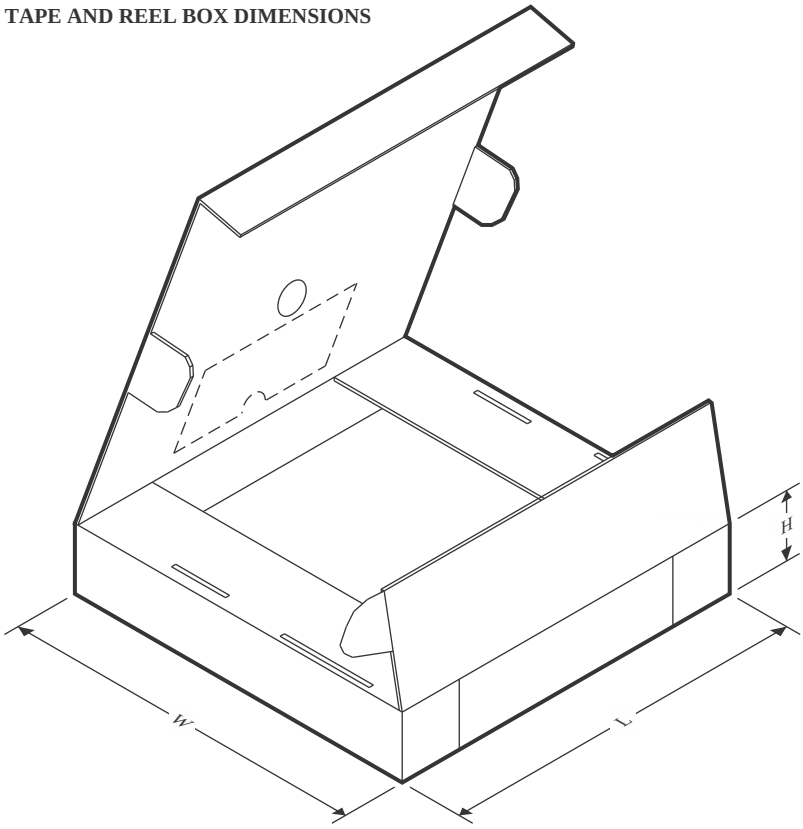
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS208CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TRS208IDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TRS208IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

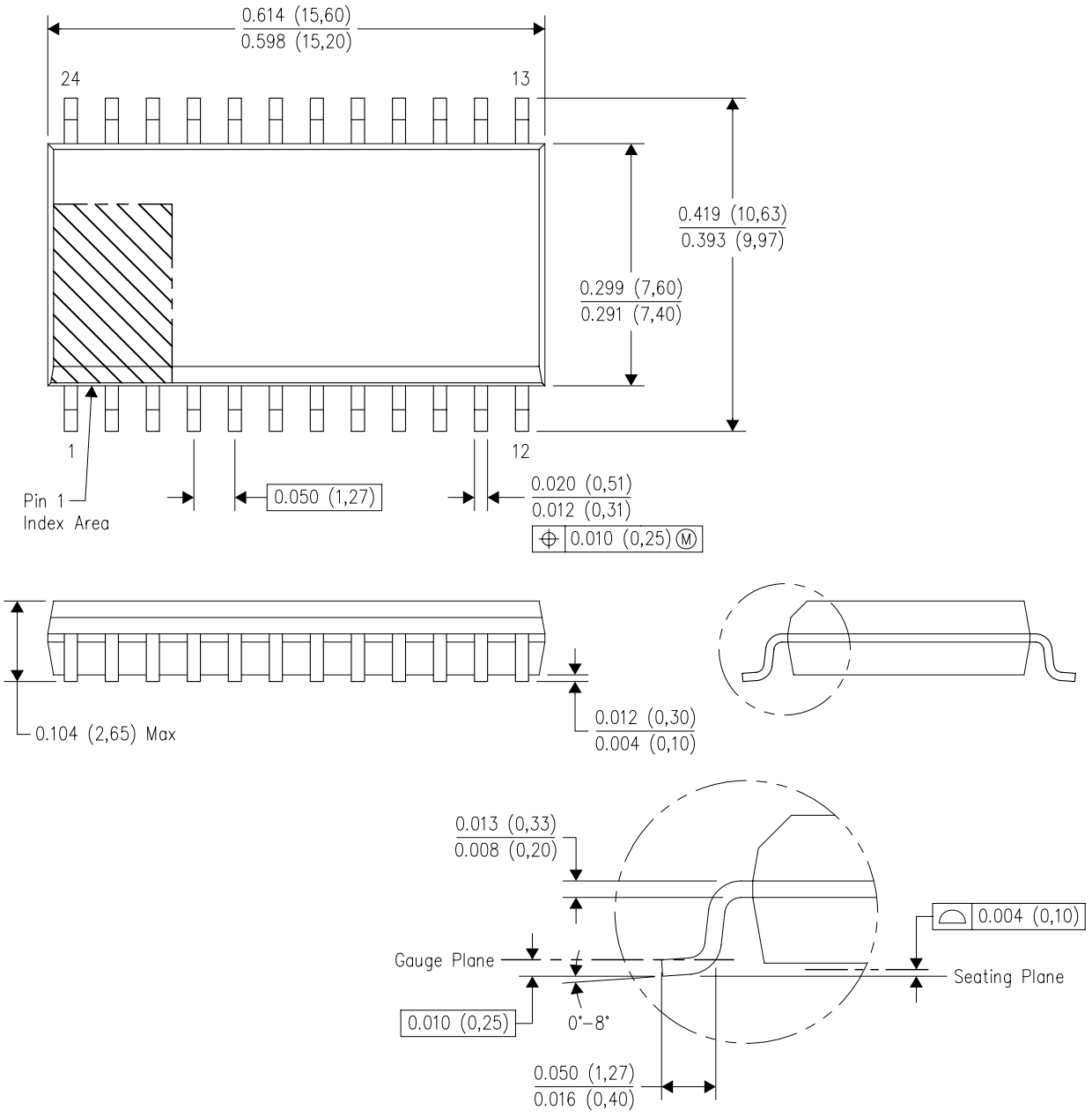
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS208CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TRS208IDBR	SSOP	DB	24	2000	353.0	353.0	32.0
TRS208IDWR	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

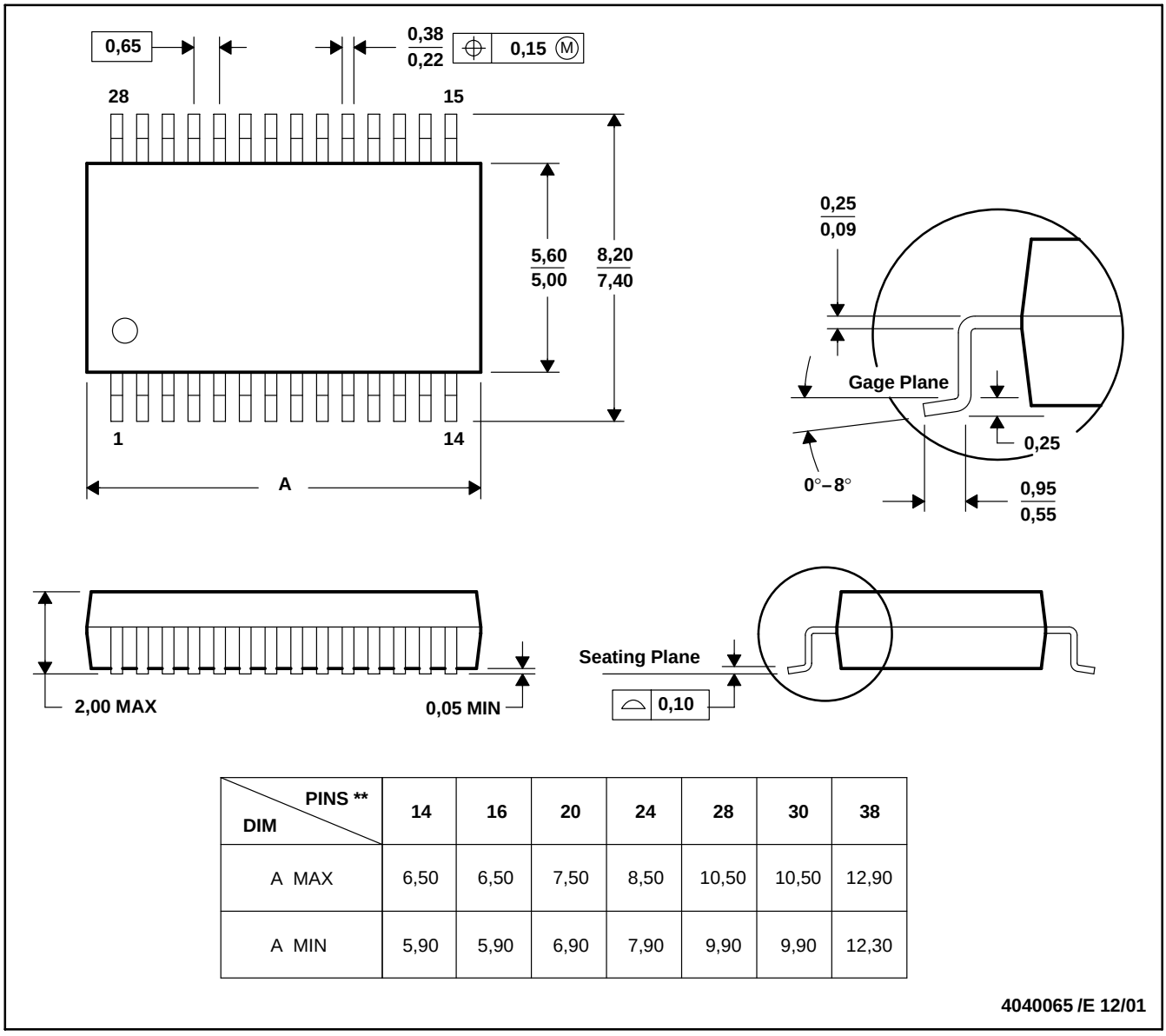


NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265