

SN54ABT823, SN74ABT823 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS158E – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (NT) and Ceramic (JT) DIPs

description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

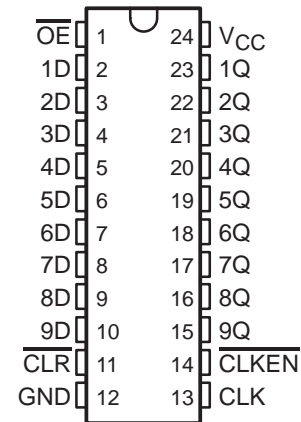
With the clock-enable ($\overline{\text{CLKEN}}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{\text{CLR}}$) input low causes the nine Q outputs to go low, independently of the clock.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

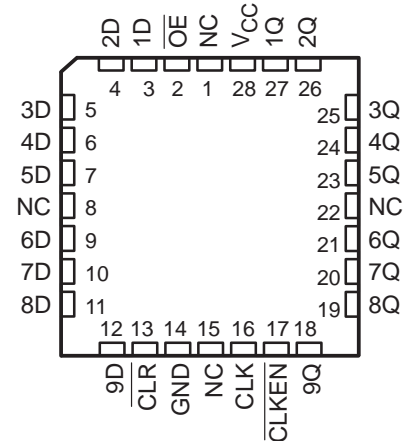
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT823 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT823 is characterized for operation from -40°C to 85°C .

SN54ABT823 . . . JT OR W PACKAGE
SN74ABT823 . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT823 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

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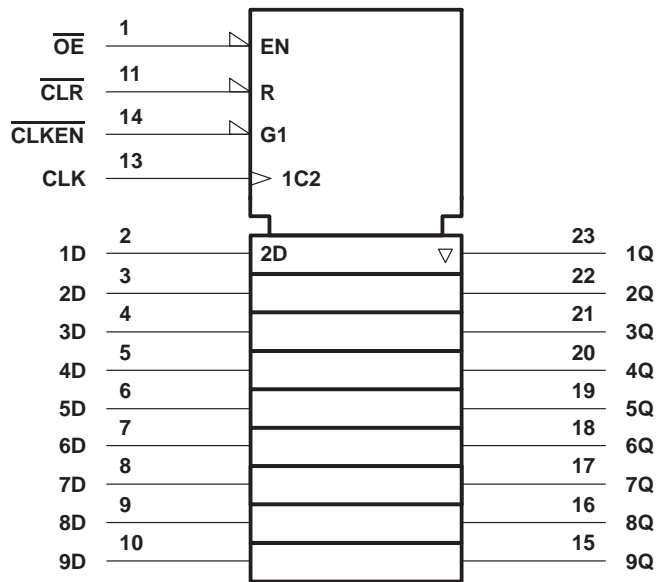
SN54ABT823, SN74ABT823 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each flip-flop)

| INPUTS | | | | | OUTPUT |
|-----------------|------------------|--------------------|-----|---|----------------|
| \overline{OE} | \overline{CLR} | \overline{CLKEN} | CLK | D | Q |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | Q ₀ |
| H | X | X | X | X | Z |

logic symbol†

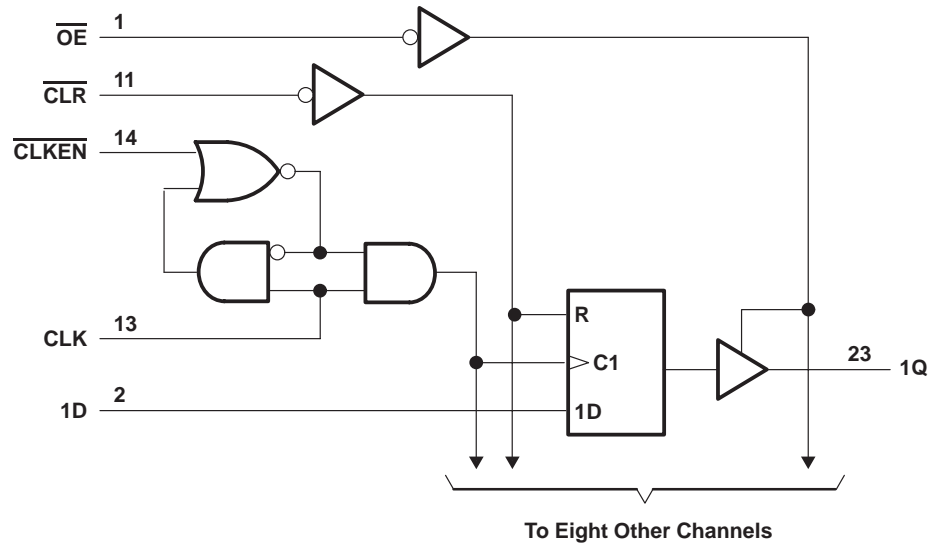


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT823 | 96 mA |
| SN74ABT823 | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DB package | 104°C/W |
| DW package | 81°C/W |
| NT package | 67°C/W |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions (see Note 3)

| | | SN54ABT823 | | SN74ABT823 | | UNIT |
|--------------------------|------------------------------------|------------|----------|------------|----------|--------------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -24 | | -32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 5 | | 5 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μ s/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | $^{\circ}$ C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = 25^{\circ}$ C | | | SN54ABT823 | | SN74ABT823 | | UNIT |
|-----------------------|---|----------------------|------|-----------|------------|----------|------------|-----------|---------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V_{IK} | $V_{CC} = 4.5$ V, $I_I = -18$ mA | | | -1.2 | | -1.2 | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5$ V, $I_{OH} = -3$ mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC} = 5$ V, $I_{OH} = -3$ mA | 3 | | | 3 | | 3 | | |
| | $V_{CC} = 4.5$ V, $I_{OH} = -24$ mA | 2 | | | 2 | | | 2 | |
| V_{OL} | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | 0.55 | | 0.55 | | | V |
| | | $I_{OL} = 64$ mA | | 0.55* | | | 0.55 | | |
| V_{hys} | | | 100 | | | | | | mV |
| I_I | $V_{CC} = 5.5$ V, $V_I = V_{CC}$ or GND | | | ± 1 | | ± 1 | | ± 1 | μ A |
| I_{OZPU}^{\ddagger} | $V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$ | | | ± 50 | | ± 50 | | ± 50 | μ A |
| I_{OZPD}^{\ddagger} | $V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$ | | | ± 50 | | ± 50 | | ± 50 | μ A |
| I_{OZH} | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V | | | 10§ | | 10§ | | 10§ | μ A |
| I_{OZL} | $V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V | | | -10§ | | -10§ | | -10§ | μ A |
| I_{off} | $V_{CC} = 0$, V_I or $V_O \leq 4.5$ V | | | ± 100 | | | | ± 100 | μ A |
| I_{CEX} | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | | | 50 | | 50 | | 50 | μ A |
| I_{O}^{\parallel} | $V_{CC} = 5.5$ V, $V_O = 2.5$ V | -50 | -140 | -180 | -50 | -180 | -50 | -180 | mA |
| I_{CC} | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | 1 | 250 | 250 | | 250 | | μ A |
| | | Outputs low | 24 | 38 | 38 | | 38 | | mA |
| | | Outputs disabled | 0.5 | 250 | 250 | | 250 | | μ A |
| $\Delta I_{CC}^{\#}$ | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND | | | 1.5 | | 1.5 | | 1.5 | mA |
| C_i | $V_I = 2.5$ V or 0.5 V | | | 4 | | | | | pF |
| C_o | $V_O = 2.5$ V or 0.5 V | | | 7 | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5$ V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | $V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$ | | SN54ABT823 | | SN74ABT823 | | UNIT |
|--------------------|--|--|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 0 | 125 | 0 | 125 | 0 | 125 | MHz |
| t_w | Pulse duration | CLR low | 5.5 | 5.5 | 5.5 | 5.5 | 5.5 | ns |
| | | CLK high | 2.9 | 2.9 | 2.9 | 2.9 | | |
| | | CLK low | 3.8 | 3.8 | 3.8 | 3.8 | | |
| t_{su} | Setup time before $\text{CLK}\uparrow$ | CLR inactive | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | ns |
| | | Data | 2.1 | 2.1 | 2.1 | 2.1 | | |
| | | CLKEN high | 2 | 2 | 2 | 2 | | |
| | | CLKEN low | 3.3 | 3.3 | 3.3 | 3.3 | | |
| t_h | Hold time after $\text{CLK}\uparrow$ | Data | 1.3 | 1.3 | 1.3 | 1.3 | ns | |
| | | CLKEN high | 1 | 1 | 1 | 1 | | |
| | | CLKEN low | 2 | 2 | 2 | 2 | | |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

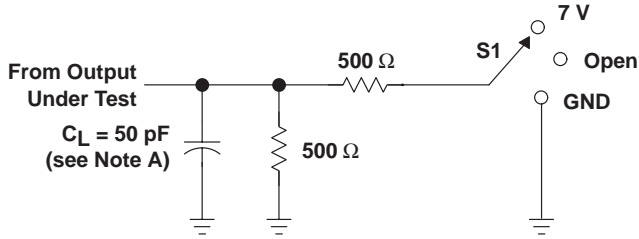
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$ | | | SN54ABT823 | | SN74ABT823 | | UNIT |
|------------------|-------------------------|-------------|--|-----|------------------|------------|-----|------------|------------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 125 | 200 | | 125 | | 125 | | MHz |
| t_{PLH} | CLK | Q | 2.1 | 4.3 | 5.9 | 2.1 | 8.1 | 2.1 | 6.8 | ns |
| t_{PHL} | | | 2.2 | 4.4 | 6.1 | 2.2 | 7 | 2.2 | 6.7 | |
| t_{PHL} | $\overline{\text{CLR}}$ | Q | 2 | 4.1 | 6.3 | 2 | 7.3 | 2 | 7.1 | ns |
| t_{PZH} | $\overline{\text{OE}}$ | Q | 1 | 3 | 4.7 [†] | 1 | 6.3 | 1 | 6 [†] | ns |
| t_{PZL} | | | 2.2 | 4.1 | 5.6 | 2.2 | 6.6 | 2.2 | 6.5 [†] | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | 2.7 | 4.8 | 6.5 [†] | 2.7 | 7.7 | 2.7 | 7.5 [†] | ns |
| t_{PLZ} | | | 1.9 | 5 | 6.4 | 1.9 | 7.4 | 1.9 | 6.9 | |

[†] This data sheet limit may vary among suppliers.

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9-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

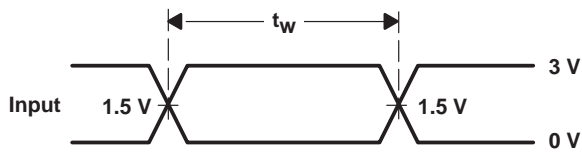
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PARAMETER MEASUREMENT INFORMATION

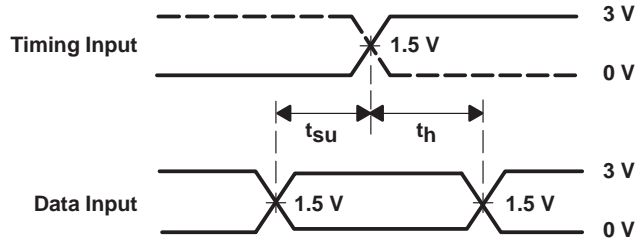


LOAD CIRCUIT

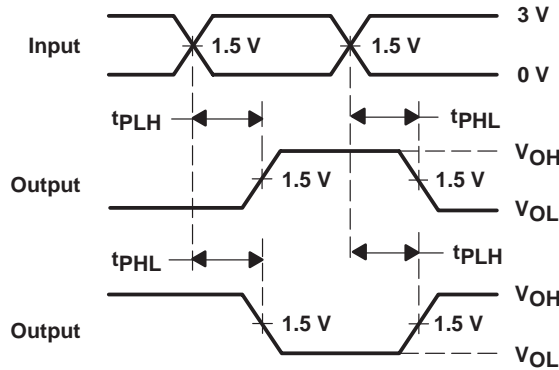
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



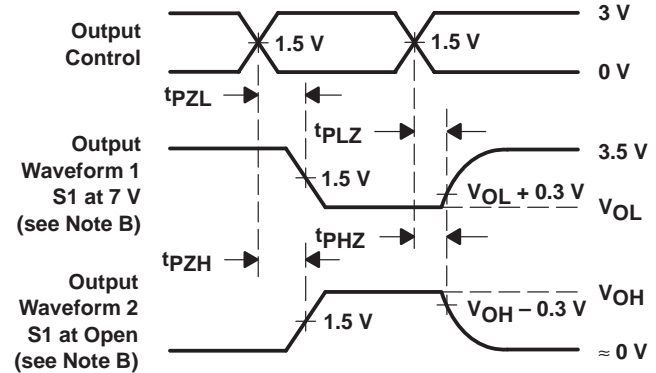
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-9450801Q3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9450801Q3A SNJ54 ABT823FK | Samples |
| 5962-9450801QKA | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9450801QK A SNJ54ABT823W | Samples |
| 5962-9450801QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9450801QL A SNJ54ABT823JT | Samples |
| SN74ABT823DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74ABT823DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AB823 | Samples |
| SN74ABT823DBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AB823 | Samples |
| SN74ABT823DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT823 | Samples |
| SN74ABT823DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT823 | Samples |
| SN74ABT823NT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ABT823NT | Samples |
| SNJ54ABT823FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9450801Q3A SNJ54 ABT823FK | Samples |
| SNJ54ABT823JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9450801QL A SNJ54ABT823JT | Samples |
| SNJ54ABT823W | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9450801QK A SNJ54ABT823W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ABT823, SN74ABT823 :

● Catalog: [SN74ABT823](#)

● Military: [SN54ABT823](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT823DBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT823DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT823DBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74ABT823DWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

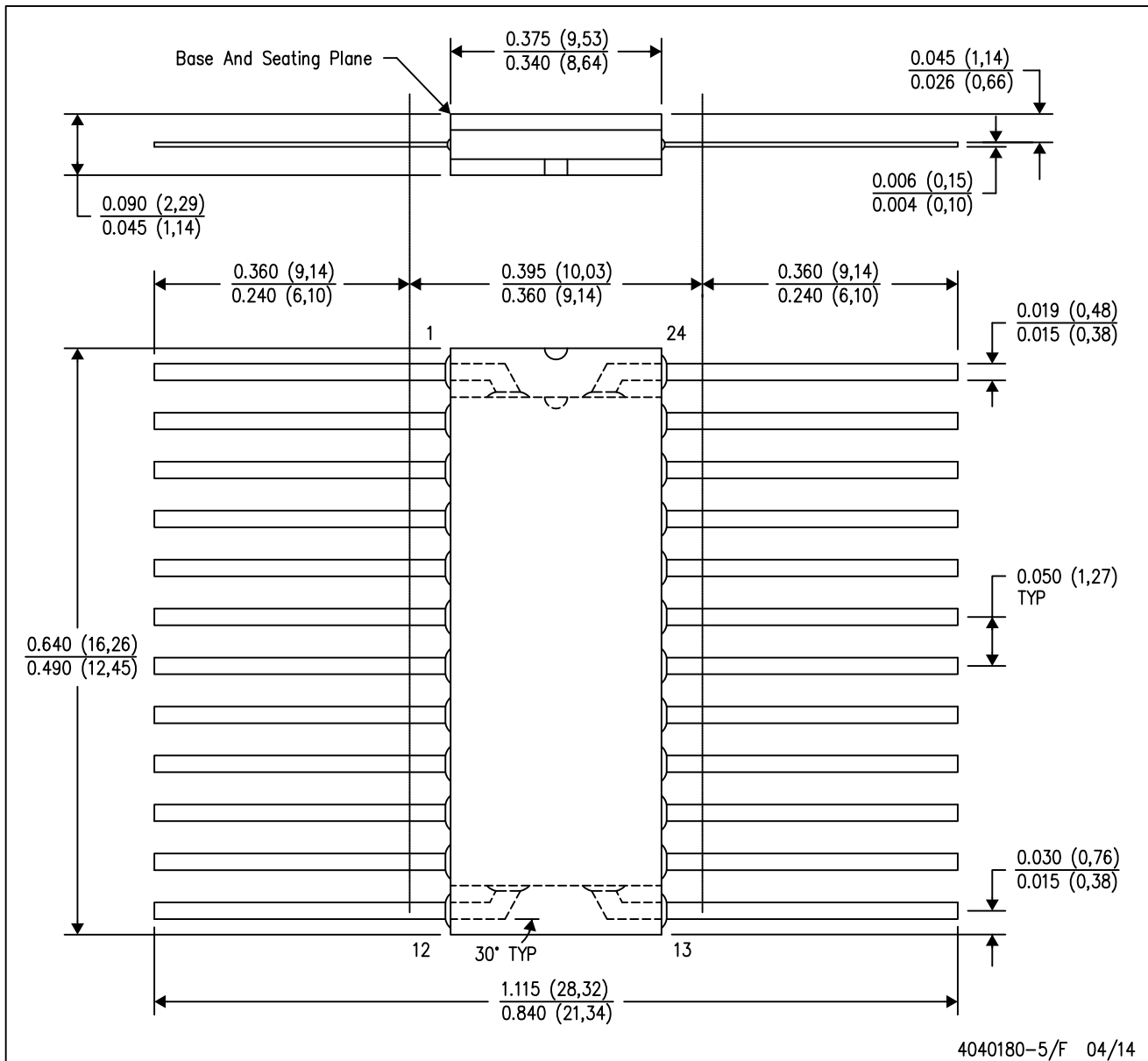
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



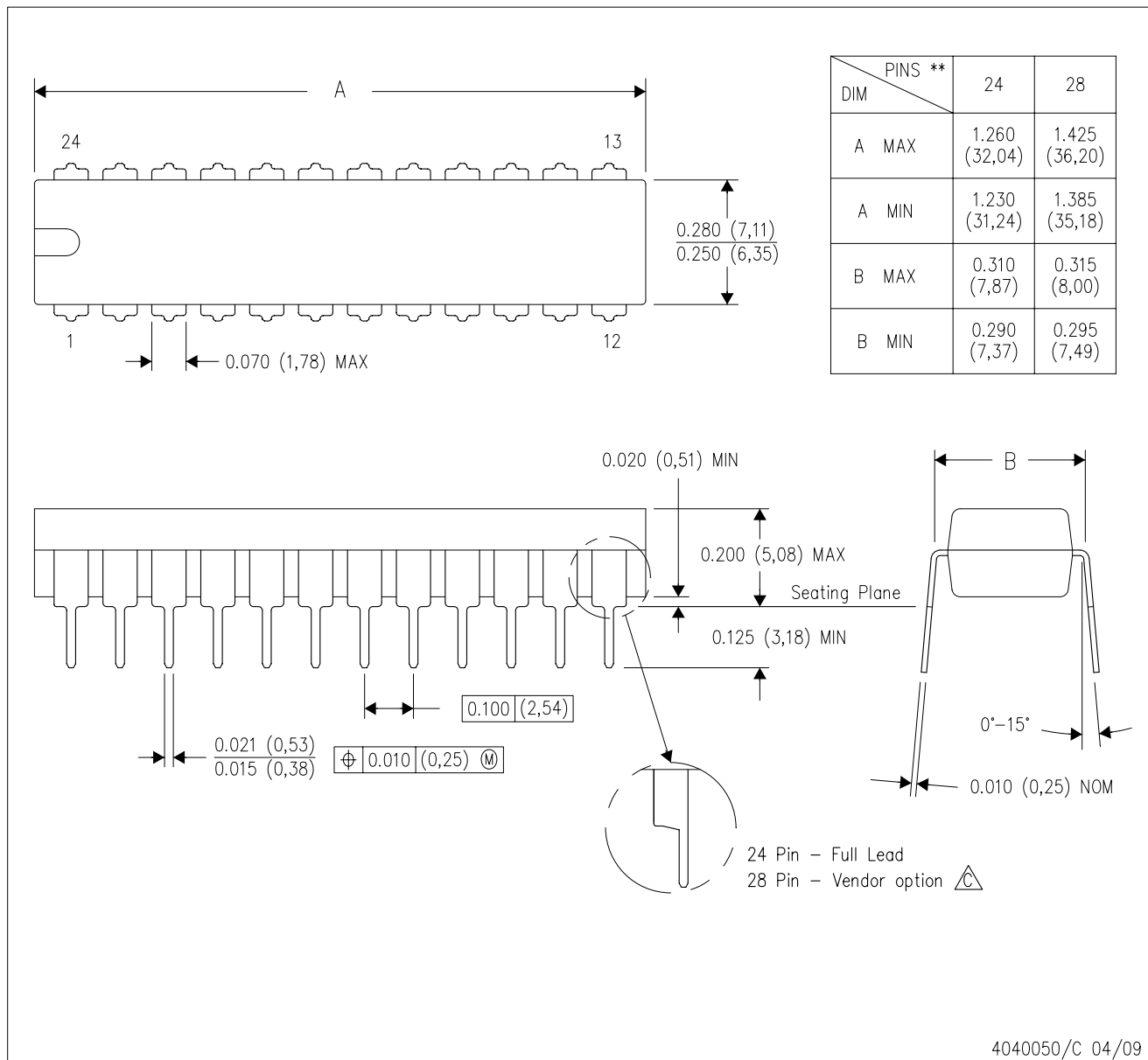
4040140/D 01/11


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

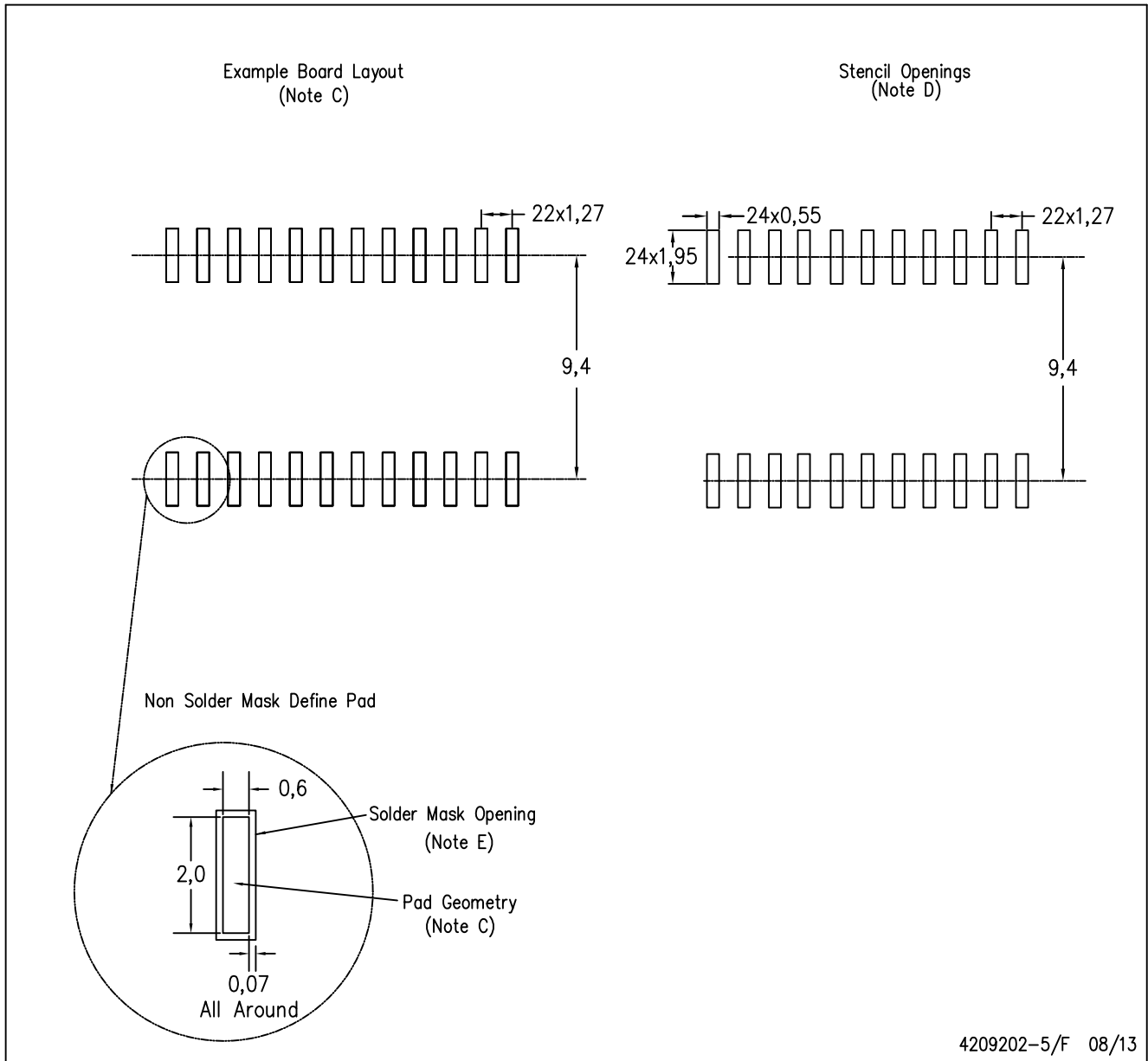
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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