1M × 16-MBit Synchronous DRAM for High-Speed Graphics Applications

- High Performance:

	-5.5	-6	-7	Unit
f_{CKMAX} @ CL = 3	183	166	143	MHz
t_{CK3}	5.5	6	7	ns
t_{AC3}	4.5	5	5	ns
f_{CKMAX} @ CL = 2	133	125	115	MHz
t_{CK2}	7.5	8	9	ns
t_{AC2}	5.4	6	6	ns

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Dual Banks controlled by A11 (Bank Select)
- Programmable $\overline{\text{CAS}}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8
- Full page (optional) for sequential wrap around
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write Control
- Dual Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- 4096 Refresh Cycles/64 ms
- Latency 2 at 133 MHz
- Latency 3 at 183 MHz
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface
- Plastic Packages: P-TSOPII-50 400 mil width (x16)

The HYB 39S16160CT-5.5/-6/-7 are high-speed dual-bank Synchronous DRAM's organized as 2 banks × 512 kbit × 16. These synchronous devices achieve high-speed data transfer rates up to 183 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated using the Infineon advanced 16 MBit DRAM process technology.

The device is designed to comply with all JEDEC standards set for Synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the two memory banks in an interleaved fashion allows random access operation to occur at higher rates than is possible with standard DRAMs. A sequential and gapless data rate of up to 183 MHz is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

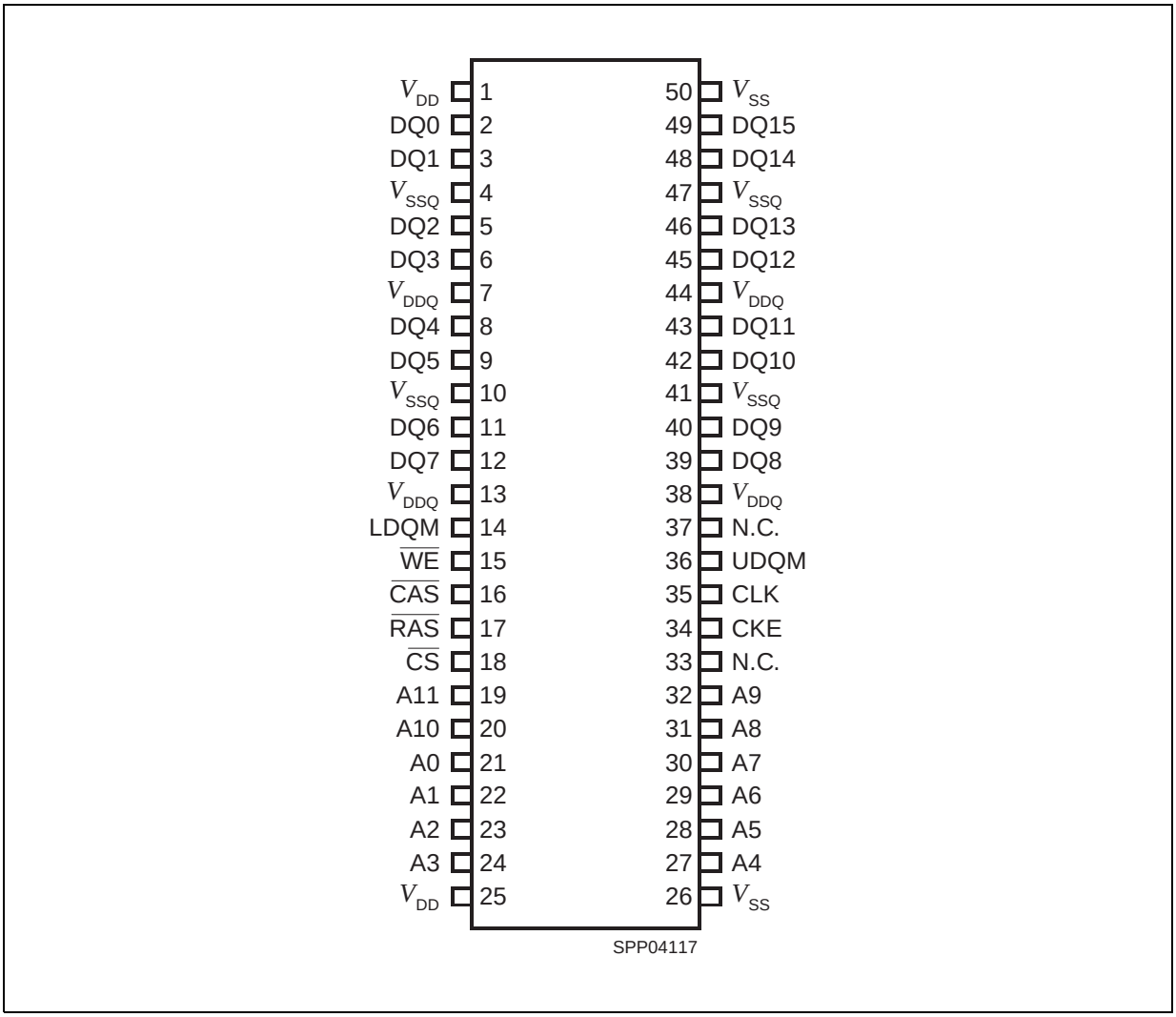
Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply and are available in TSOPII packages.

Ordering Information

Type	Ordering Code	Package	Description
LVTTL-Version			
HYB 39S16160CT-5.5	on request	P-TSOPII-50 (400mil)	183 MHz 2B × 512k x16 SDRAM
HYB 39S16160CT-6	on request	P-TSOPII-50 (400mil)	166 MHz 2B × 512k x16 SDRAM
HYB 39S16160CT-7	on request	P-TSOPII-50 (400mil)	143 MHz 2B × 512k x16 SDRAM

Pin Definitions and Functions

CLK	Clock Input	DQ	Data Input/Output
CKE	Clock Enable	LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Power for DQ's (+ 3.3 V)
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQ's
A0 - A10	Address Inputs	N.C.	Not connected
A11(BS)	Bank Select		



Pin Configuration

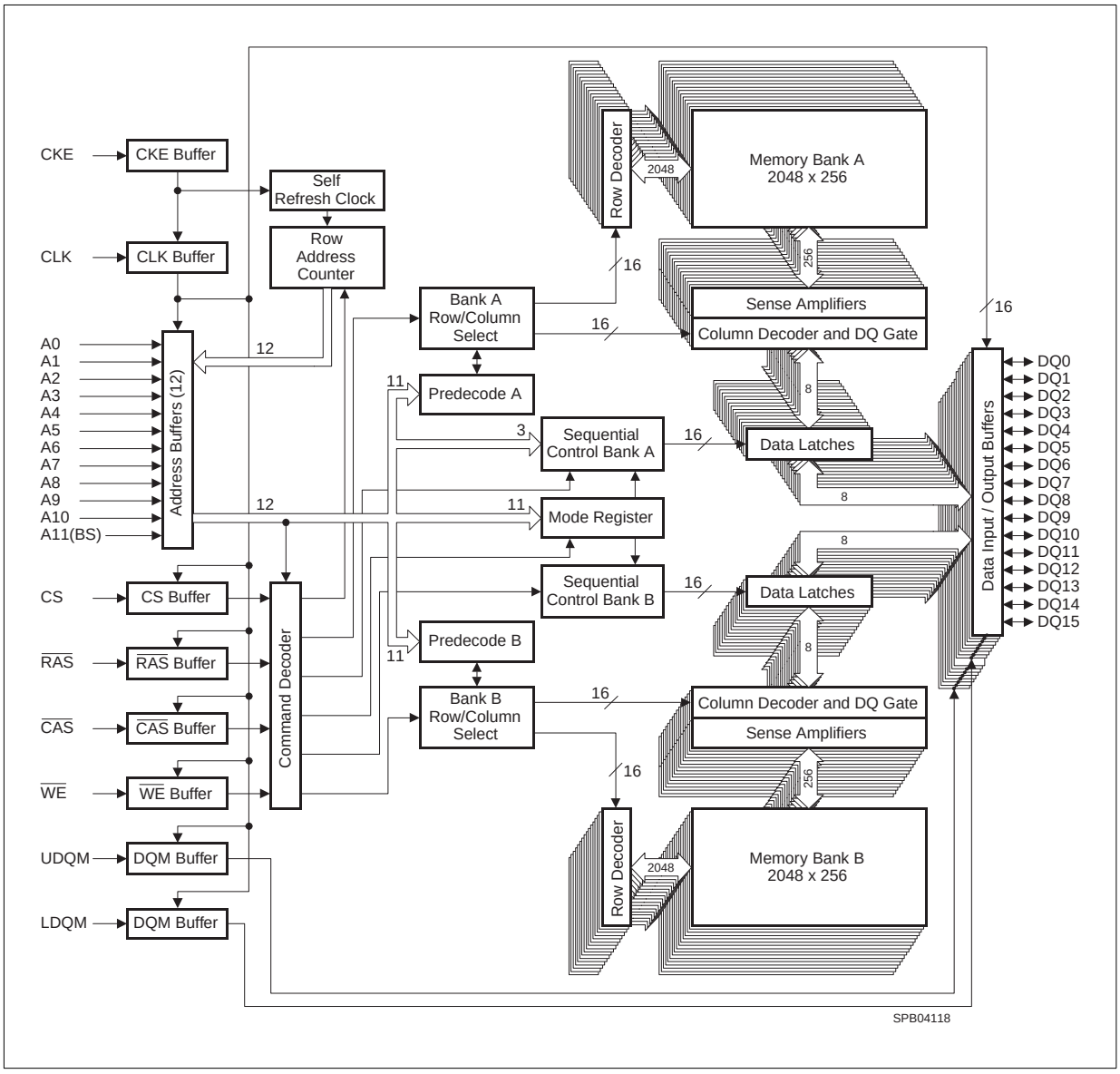
Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The System Clock Input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby inititiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A10	Input	Level	–	During a Bank Activate command cycle, A0-A10 define the row address (RA0 - RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 define the column address (CA0 - CAn) when sampled at the rising clock edge. CAn depends on the SDRAM organization. 1M $\times$ 16 SDRAM CAn = CA7 In addition to the column address, A10 is used to invoke autoprecharge operation at the end of the burst Read or Write cycle. If A10 is high, autoprecharge is selected and A11 defines the bank to be precharged (low = bank A, high = bank B). If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with A11 to control which bank(s) to precharge. If A10 is high, both bank A and bank B will be precharged regardless of the state of A11. If A10 is low, then A11 is used to define which bank to precharge.
A11 (BS)	Input	Level	–	Selects which bank is to be active. A11 low selects bank A and A11 high selects bank B.
DQx	Input Output	Level	–	Data Input/Output pins operate in the same manner as on conventional DRAMs.

Signal Pin Description (cont'd)

Pin	Type	Signal	Polarity	Function
LDQM, UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low, but blocks the write operation if DQM is high.
V_{DD} V_{SS}	Supply	–	–	Power and Ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	–	–	Power Supply and Ground for the output buffers to provide improved noise immunity.

Functional Block Diagrams



Block Diagram: HYB 39S16160CT (2 bank × 512k × 16 SDRAM)

Operation Definition

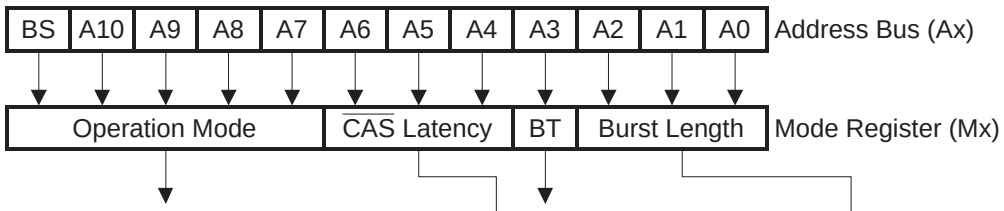
All SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and DQM at the positive edge of the clock. The following list shows the most important operation commands.

Operation	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	(L/U)DQM
Standby, Ignore $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address	H	X	X	X	X
Row Address Strobe and Activating a Bank	L	L	H	H	X
Column Address Strobe and Read Command	L	H	L	H	X
Column Address Strobe and Write Command	L	H	L	L	X
Precharge Command	L	L	H	L	X
Burst Stop Command	L	H	H	L	X
Self Refresh Entry	L	L	L	H	X
Mode Register Set Command	L	L	L	L	X
Write Enable/Output Enable	X	X	X	X	L
Write Inhibit/Output Disable	X	X	X	X	H
No Operation (NOP)	L	H	H	H	X

Mode Register

For application flexibility, $\overline{CAS}$ latency, burst length, and burst sequence can be programmed in the SDRAM Mode Register. The mode set operation must be done after the initial power up and before any activate command . Any content of the Mode Register can be altered by re-executing the mode set command. Both banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set, as shown in the following table.

Address Input for Mode Set (Mode Register Operation)



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Normal
X	X	1	0	0	Multiple Burst with Single Write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{\text{CAS}}$ Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page*)	Reserved

*) Optional

Sequential Burst Addressing	Interleave Burst Addressing
0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

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Read and Write Access Mode

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a $\overline{RAS}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the word line are fired. A $\overline{CAS}$ cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the $\overline{RAS}$ timing. $\overline{WE}$ is used to define either a Read ($\overline{WE}$ = H) or a Write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{CAS}$ cycle, serial data Read or Write operations are allowed at up to a 183 MHz data rate. The number of serial data bits is determined by the burst length programmed at the mode set operation; that is, either 1, 2, 4, 8, or full page (Note that full page is an optional feature in this device). Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{CAS}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organization and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3, or 8, full page burst continues until it is terminated using another command.

Similar to the page mode of conventional DRAM’s, burst Read or Write accesses on any column address are possible once the $\overline{RAS}$ cycle latches sense amplifiers. The maximum refresh interval time (t_{RAS}) limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overwritten by the new address with the full burst length. An interrupt which accompanies with an operation change from a Read to a Write is possible by exploiting DQM to avoid bus contention.

When two banks are activated sequentially, interleaved bank Read or Write operations are possible. Using the programmed burst length, alternate access and precharge operations on two banks can implement fast serial data access modes among many different pages. After two banks are activated, column to column interleave operation can be done between two different pages.

Refresh Mode

SDRAM has two refresh modes: $\overline{CAS}$ before $\overline{RAS}$ (CBR) Automatic Refresh and a Self Refresh. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes. The chip enters the Automatic Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a Burst Refresh mode. The same rule applies to any access command after the Automatic Refresh operation.

The chip has an on-chip timer and the self Refresh Mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read write operations. During reads, when it turns to high at a clock timing, data outputs are disabled and become high impedance after a two-clock delay (DQM Data Disable Latency t_{DQZ}). DQM also provides a data mask function for writes. When it is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high and CLK is enabled. When CKE is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

To reduce standby power consumption, a Power Down mode is available. Bringing CKE low enters the Power Down mode and all of receiver circuits are gated. All banks must be precharged before entering this mode. One clock delay is required for mode entry and exit. The Power Down mode does not perform any refresh operations.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the Read with Auto-Precharge function is initiated. If CA10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation a time equal to t_{WR} (write recovery time) after the last data in.

Precharge Command

If CA10 is low, the chip needs another way to precharge. In this mode, a separate precharge command is necessary. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Two address bits, A10 and A11, are used to define banks as shown in the following list. The precharge command may be applied coincident with the last of burst reads for $\overline{CAS}$ Latency = 1 and with the second to the last read data for $\overline{CAS}$ Latencies = 2 & 3. Writes require a time t_{WR} from the last burst data to apply the precharge command.

Bank Selection by Address Bits

	A10	A11
Bank A only	Low	Low
Bank B only	Low	High
Both A and B	High	Don’t Care

Burst Termination

After a burst Read or Write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, using a Precharge Command to interrupt a burst

cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command, care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst Write operation, then any residual data from the burst Write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Power Up Procedure

All V_{DD} and V_{DDQ} must reach the specified voltage no later than any of input signal voltages. An initial pause of 200 µs is required after power on. During this time, CKE must be stable high and no Self Refresh command may be issued. All banks must be precharged and a minimum of eight Auto Refresh cycles are required prior to the mode register set operation.

Electrical Characteristics

Absolute Maximum Ratings

Operating Temperature Range ..... 0 to + 70 °C
Storage Temperature Range ..... – 55 to + 150 °C
Input/Output Voltage ..... – 0.5 to min (V_{DD} + 0.5, 4.6) V
Power Supply Voltage V_{DD}/V_{DDQ} ..... – 1.0 to + 4.6 V
Power Dissipation ..... 1 W
Data Out Current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operation and DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD},V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V	1, 2, 3
Input Low Voltage	V_{IL}	– 0.3	0.8	V	1, 2, 3
Output High Voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V	3
Output Low Voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	3
Input Leakage Current, any input (0 V < V_{IN} < V_{DDQ}, all other inputs = 0 V)	$I_{I(L)}$	– 5	5	µA	–
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 5	5	µA	–

Notes

1. All voltages are referenced to V_{SS}
2. V_{IH} may overshoot to V_{DD} + 2.0 V for pulse width of < 4 ns with 3.3 V. V_{IL} may undershoot to – 2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% with amplitude measured peak to DC reference.

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Values		Unit
		min.	max.	
Input Capacitance (CLK)	C_{I1}	2.5	4.0	pF
Input Capacitance (A0 - A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM, UDQM, LDQM)	C_{I2}	2.5	5.0	pF
Input/Output Capacitance (DQ)	C_{IO}	4.0	6.5	pF

Operating Currents

T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-5.5	-6	-7	Unit	Note
			max.				
Operating current	Burst Length = 4 $t_{RC} \geq t_{RC(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA 2 bank interleave operation	I_{CC1}	110	100	90	mA	1, 2
Precharge standby Current in Power Down Mode	CKE ≤ $V_{IL(MAX.)}$ $t_{CK} \geq t_{CK(MIN.)}$	I_{CC2P}	2	2	2	mA	2
	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite	I_{CC2PS}	1	1	1	mA	–
Precharge standby Current in Non-Power Down Mode	CKE ≥ $V_{IH(MIN.)}$ $t_{CK} \geq t_{CK(MIN.)}$, input signals changed once in 3 cycles	I_{CC2N}	15	15	15	mA	$\overline{CS}$ = High
	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, input signals are stable	I_{CC2NS}	5	5	5	mA	–
Active standby Current in Power Down Mode	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = $t_{CK(MIN.)}$	I_{CC3P}	4	4	4	mA	–
	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = infinite, input signals are stable	I_{CC3PS}	4	4	4	mA	–
Active standby Current in Non Power Down Mode	CKE ≥ $V_{IH(MIN.)}$, $t_{CK} \geq t_{CK(MIN.)}$ changed once in 3 cycles	I_{CC3N}	25	25	25	mA	$\overline{CS}$= High, 1
	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = infinite, input signals are stable	I_{CC3NS}	15	15	15	mA	–
Burst Operating Current	Burst Length = full page t_{RC} = infinite $t_{CK} \geq t_{CK(MIN.)}$, I_O = 0 mA, 2 banks interleave	I_{CC4}	100	90	80	mA	1, 2

Operating Currents (cont'd)
T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V
(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-5.5	-6	-7	Unit	Note
			max.				
Auto (CBR) Refresh Current	$t_{RC} = t_{RC(MIN.)}$	I_{CC5}	70	60	50	mA	1, 2
Self Refresh	CKE ≤ 0.2 V	I_{CC6}	1	1	1	mA	1, 2

Notes

1. The specified values are valid when addresses are changed no more than three times during $t_{RC(MIN.)}$ and when No Operation commands are registered on every rising clock edge during $t_{RC(MIN.)}$.
2. The specified values are valid when data inputs (DQ's) are stable during $t_{RC(MIN.)}$.

AC Characteristics [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-5.5		-6		-7			
		min.	max.	min.	max.	min.	max.		
Clock and Clock Enable									
Clock Cycle Time									–
$\overline{CAS}$ Latency = 3	t_{CK}	5.5	–	6	–	7	–	ns	
$\overline{CAS}$ Latency = 2	t_{CK}	7.5	–	8	–	9	–	ns	
Clock frequency									–
$\overline{CAS}$ Latency = 3	t_{CK}	–	183	–	166	–	143	MHz	
$\overline{CAS}$ Latency = 2	t_{CK}	–	133	–	125	–	115	MHz	
Access time from clock									
$\overline{CAS}$ Latency = 3	t_{AC}	–	4.5	–	5	–	5	ns	2
$\overline{CAS}$ Latency = 2	t_{AC}	–	5.4	–	6	–	6	ns	3
Clock High Pulse Width	t_{CH}	2	–	2	–	2.5	–	ns	–
Clock Low Pulse Width	t_{CL}	2	–	2	–	2.5	–	ns	–
Transition Time	t_T	0.5	10	0.5	10	0.5	10	ns	–
Setup and Hold Times									
Input Setup Time	t_{IS}	1.5	–	2	–	2	–	ns	4
Input Hold Time	t_{IH}	1	–	1	–	1	–	ns	4
CKE Setup Time	t_{CKS}	1.5	–	2	–	2	–	ns	4
CKE Hold Time	t_{CKH}	1	–	1	–	1	–	ns	4
Mode Register Set-up Time	t_{RSC}	11	–	12	–	24	–	ns	–
Power Down Mode Entry Time	t_{SB}	0	5.5	0	6	0	7	ns	–
Common Parameters									
Row to Column Delay Time	t_{RCD}	15	–	16	–	18	–	ns	5
Row Precharge Time	t_{RP}	15	–	16	–	18	–	ns	5
Row Active Time	t_{RAS}	33	–	36	100k	42	100k	ns	5
Row Cycle Time	t_{RC}	49.5	–	54	–	63	–	ns	5
Activate(a) to Activate(b) Command Period	t_{RRD}	11	–	12	–	14	–	ns	–
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	1	–	1	–	CLK	–

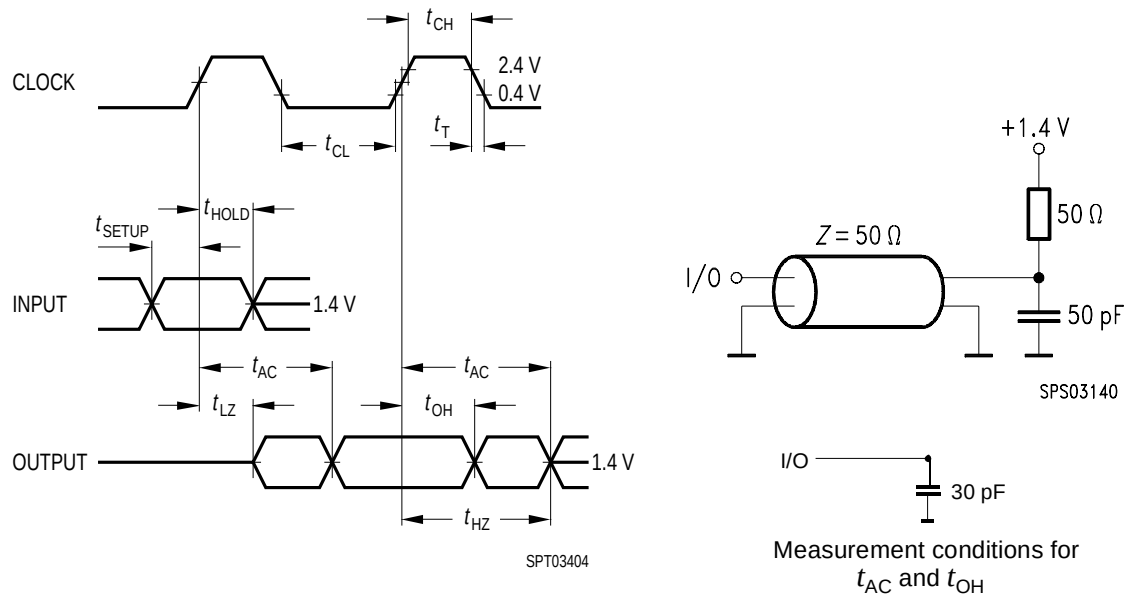
AC Characteristics (cont'd)[1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symb.	Limit Values						Unit	Note
		-5.5		-6		-7			
		min.	max.	min.	max.	min.	max.		
Refresh Cycle									
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	–	64	ms	–
Self Refresh Exit Time	t_{SREX}	10	–	10		10		ns	[6]
Read Cycle									
Data Out Hold time	t_{OH}	2	–	2	–	2.5	–	ns	[2]
Data Out to Low Impedance time	t_{LZ}	0	–	0	–	0	–	ns	–
Data Out to High Impedance time	t_{HZ}	2	5.5	2	6	2	7	ns	–
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	–
Write Cycle									
Write Recovery Time	t_{WR}	2	–	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	–
Write Latency	t_{WL}	0	–	0	–	0	–	CLK	–

Notes for AC Parameters:

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests for LV-TTL versions have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in Figure below. Specified t_{AC} and t_{OH} parameters are measured with a 30 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.



Measurement conditions for t_{AC} and t_{OH}

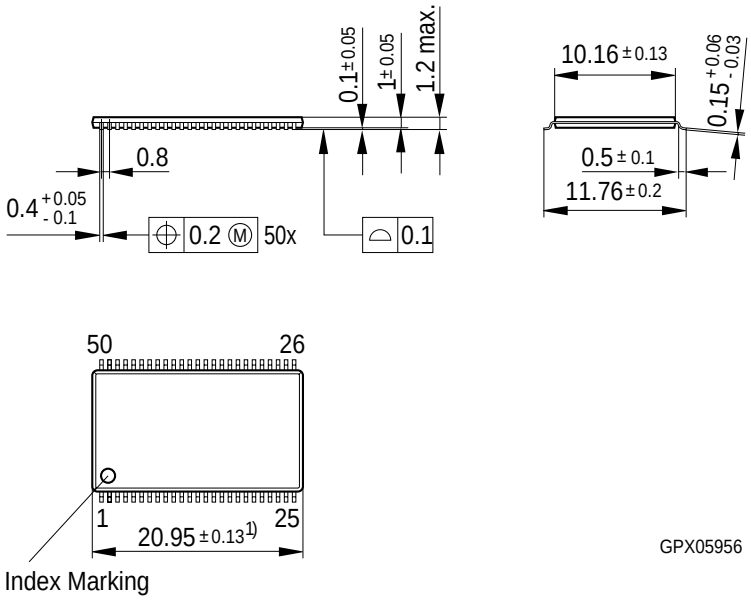
3. If clock rising time is longer than 1ns, a time (t_T/2 – 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
   the number of clock cycle = specified value of timing period (counted in fractions as a whole number)
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.

Frequency vs. AC Parameter Relationship Table

	CL	t_{RCD}	t_{RP}	t_{RC}	t_{RAS}	t_{RRD}	t_{CCD}	WL	t_{WR}
-5.5 -parts									
183 MHz	3	3	3	9	6	2	1	0	2
133 MHz	2	2	2	7	5	2	1	0	2
-6 -parts									
166 MHz	3	3	3	9	6	2	1	0	2
125 MHz	2	2	2	7	5	2	1	0	2
-7 -parts									
143 MHz	3	3	3	9	6	2	1	0	2
115 MHz	2	2	2	7	5	2	1	0	2

Package Outlines

Plastic Package, P-TSOPII-50
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm