SNx4AHCT245 Octal Bus Transceivers With 3-State Outputs

1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250 mA per JESD 17
- On products compliant to MIL-PRF-38535, All parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Enable or disable a digital signal
- Hold a signal during a controller reset
- Debounce a switch

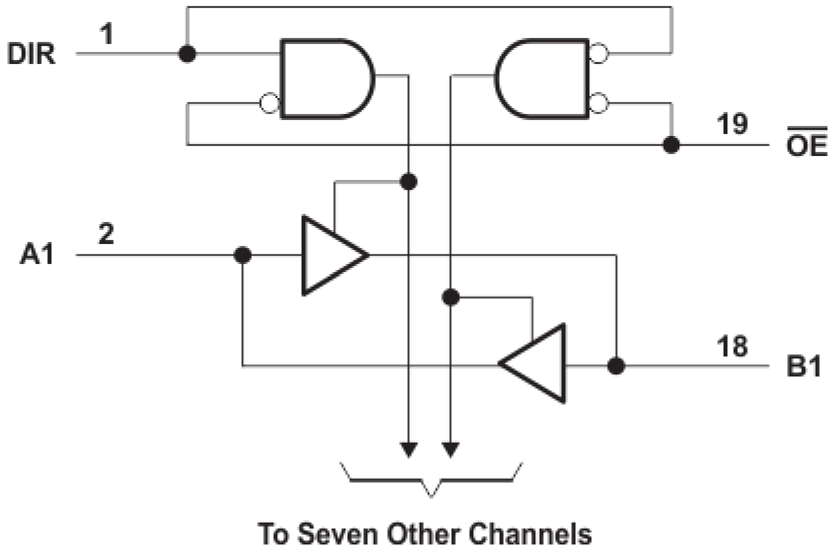
3 Description

The SNx4AHCT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. These parts operate from 4.5 V to 5.5 V.

Package Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54AHCT245	J (CDIP, 20)	24.2 mm × 6.92 mm
	W (CFP, 20)	13.09 mm × 6.92 mm
	FK (LCCC, 20)	8.89 mm × 8.89 mm
SN74AHCT245	RGY (VQFN, 20)	4.50 mm × 3.50 mm
	N (PDIP, 20)	25.40 mm × 6.35 mm
	NS (SOP, 20)	12.60 mm × 5.30 mm
	DB (SSOP (20)	7.50 mm × 5.30 mm
	DGV (TVSOP, 20)	5.00 mm × 4.40 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm
	RKS (VQFN, 20)	4.50 mm × 2.50 mm
	DGS (VSSOP, 20)	5.10 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (April 2023) to Revision S (July 2023)	Page
• Updated RθJA values: DB = 96.0 to 113.1, DW = 79.8 to 96.2, PW = 102.8 to 122.3; Updated DB, DW, and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	5

Changes from Revision Q (December 2022) to Revision R (April 2023)	Page
• Updated the Applications section	1
• Added DGS package information to the Package Information table, Pin Configuration and Functions, and Thermal Information	1
• Updated the Package Information table	1

Changes from Revision P (July 2014) to Revision Q (December 2022)	Page
• Added RKS package information to the Package Information table, Pin Configuration and Functions, and Thermal Information	1

5 Pin Configuration and Functions

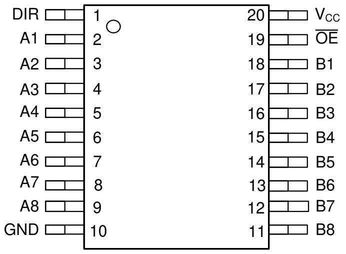


Figure 5-1. SN54AHCT245: J or W SN74AHCT245: DB, DGV, DW, N, NS, PW or DGS Package, 20-Pin CDIP, CFP, SSOP, TVSOP, SOIC, PDIP, SOP, TSSOP, or VSSOP (Top View)

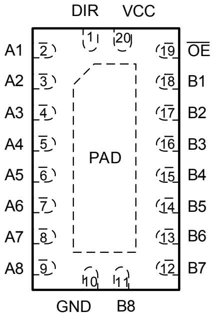


Figure 5-2. SN74AHCT245: RGY or RKS Package, 20-Pin VQFN (Top View)

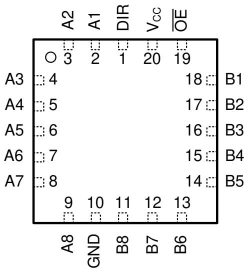


Figure 5-3. SN54AHCT245: FK Package, 20-Pin LCCC (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DIR	1	I	Direction Pin
A1	2	I/O	A1 Input/Output
A2	3	I/O	A2 Input/Output
A3	4	I/O	A3 Input/Output
A4	5	I/O	A4 Input/Output
A5	6	I/O	A5 Input/Output
A6	7	I/O	A6 Input/Output
A7	8	I/O	A7 Input/Output
A8	9	I/O	A8 Input/Output
GND	10	G	Ground Pin
B8	11	I/O	B8 Input/Output
B7	12	I/O	B7 Input/Output
B6	13	I/O	B6 Input/Output
B5	14	I/O	B5 Input/Output
B4	15	I/O	B4 Input/Output
B3	16	I/O	B3 Input/Output
B2	17	I/O	B2 Input/Output
B1	18	I/O	B1 Input/Output
$\overline{OE}$	19	I	Output Enable
VCC	20	P	Power Pin

(1) I = Input, O = Output, P= Positive Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range			–0.5	7	V
V_I	Input voltage range(2)		Control inputs	–0.5	7	V
V_O	Output voltage range(2)			–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$	Control inputs		–20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$			±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}			±25	mA
	Continuous current through V_{CC} or GND				±75	mA
T_{stg}	Storage temperature			-65	150	ºC

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		SN54AHCT245		SN74AHCT245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level Input voltage		0.8		0.8	V
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
$\Delta t/\Delta v$	Input Transition rise and fall rate		20		20	ns/V
T_A	Operating free-air temperature	–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AHCT245									UNIT
		DB	DGV	DW	N	NS	PW	RGY	RKS	DGS	
		20 PINS									
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.1	116.1	96.2	51.5	77.1	122.3	35.1	67.7	118.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.9	31.3	63.6	38.2	43.6	64.8	43.3	72.4	57.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	67.9	57.6	64.7	32.4	44.6	73.3	12.9	40.4	73.1	
Ψ_{JT}	Junction-to-top characterization parameter	39.3	1.0	40.5	24.6	17.2	19	0.9	10.3	5.7	
Ψ_{JB}	Junction-to-board characterization parameter	67.5	56.9	64.3	32.3	44.2	73	12.9	40.4	72.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	7.9	24.1	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHCT245 –55°C TO 125°C		SN74AHCT245 –40°C TO 85°C		Recommended SN74AHCT245 –40°C TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
		I_{OH} = –8 mA		3.94			3.8		3.8		3.7		
V_{OL}		I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1		0.1	V
		I_{OH} = 8 mA				0.36		0.44		0.44		0.44	
I_I	$\overline{OE}$ or DIR	V_I = 5.5 V or GND	0 to 5.5 V			±0.1		±1(1)		±1		±1	µA
I_{OZ}	A or B inputs(2)	V_O = V_{CC} or GND	5.5 V			±.25		±2.5		±2.5		±2.5	µA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40		40	µA
ΔI_{CC} (3)		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C_i	$\overline{OE}$ or DIR	V_I = V_{CC} or GND	5 V		2.5	10				10			pF
C_{io}	A or B inputs	V_I = V_{CC} or GND	5 V		4								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(3) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see (1))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		SN54AHCT245 –55°C TO 125°C		SN74AHCT245 –40°C TO 85°C		Recommended SN74AHCT245 –40°C TO 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	C_L = 15 pF	4.5(1)	7.7(1)	1(1)	10(1)	1	8.5	1	10	ns
t_{PHL}				4.5(1)	7.7(1)	1(1)	10(1)	1	8.5	1	10	
t_{PZH}	$\overline{OE}$	A or B	C_L = 15 pF	8.9(1)	13.8(1)	1(1)	16(1)	1	15	1	16	ns
t_{PZL}				8.9(1)	13.8(1)	1(1)	16(1)	1	15	1	16	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 15 pF	9.2(1)	14.4(1)	1(1)	16.5(1)	1	15.5	1	16.5	ns
t_{PLZ}				9.2(1)	14.4(1)	1(1)	16.5(1)	1	15.5	1	16.5	
t_{PLH}	A or B	B or A	C_L = 50 pF	5.3	8.7	1	11	1	9.5	1	11	ns
t_{PHL}				5.3	8.7	1	11	1	9.5	1	11	
t_{PZH}	$\overline{OE}$	A or B	C_L = 50 pF	9.7	14.8	1	17	1	16	1	17	ns
t_{PZL}				9.7	14.8	1	17	1	16	1	17	
t_{PHZ}	$\overline{OE}$	A or B	C_L = 50 pF	10	15.4	1	17.5	1	16.5	1	17.5	ns
t_{PLZ}				10	15.4	1	17.5	1	16.5	1	17.5	
$t_{sk(o)}$			C_L = 50 pF		1(2)				1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

6.7 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C(1)

PARAMETER		SNx4AHCT245			UNIT
		MIN	TYP	MAX	
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	13	pF

6.9 Typical Characteristics

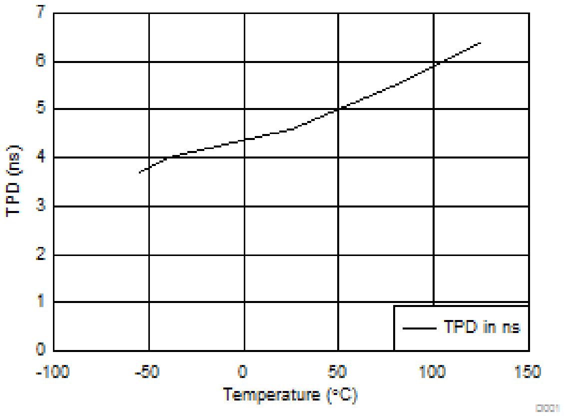
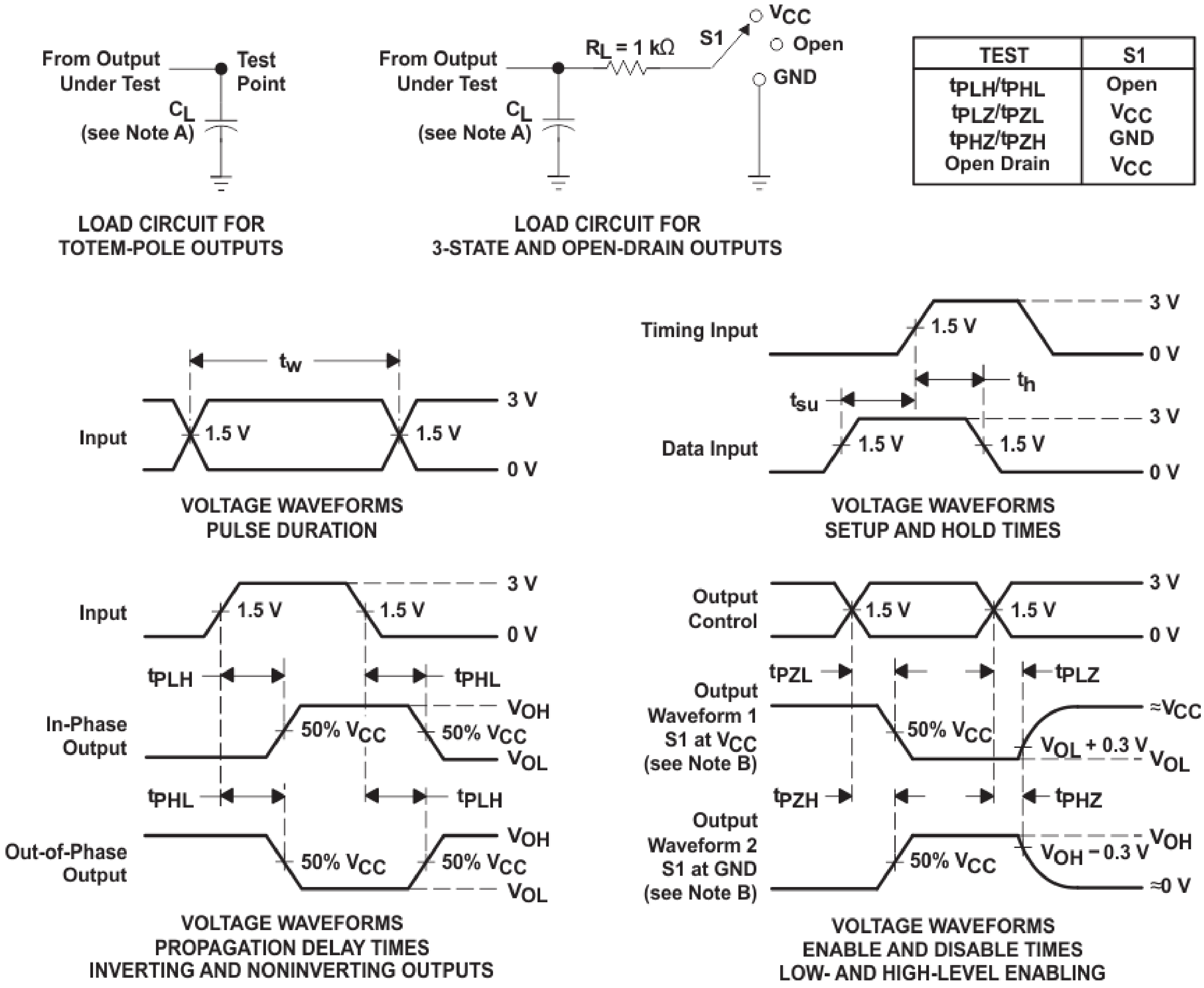


Figure 6-1. SNx4AHCT245 TPD vs Temperature, 15 pF Load

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx7ACHT245 octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4AHCT245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction–control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses effectively are isolated. For the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

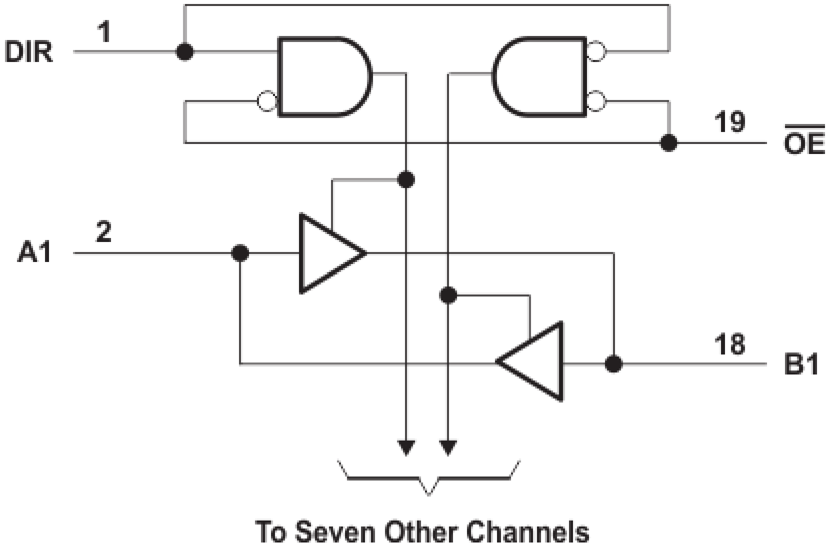


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs accept V_{IH} levels of 2 V
- Slow edge rates minimize output ringing

8.4 Device Functional Modes

Table 8-1. Function Table (Each Transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT245 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8 V V_{IL} and 2 V V_{IH}. This feature makes it ideal for translating up from 3.3 V to 5 V. The following figure shows this type of translation.

9.2 Typical Application

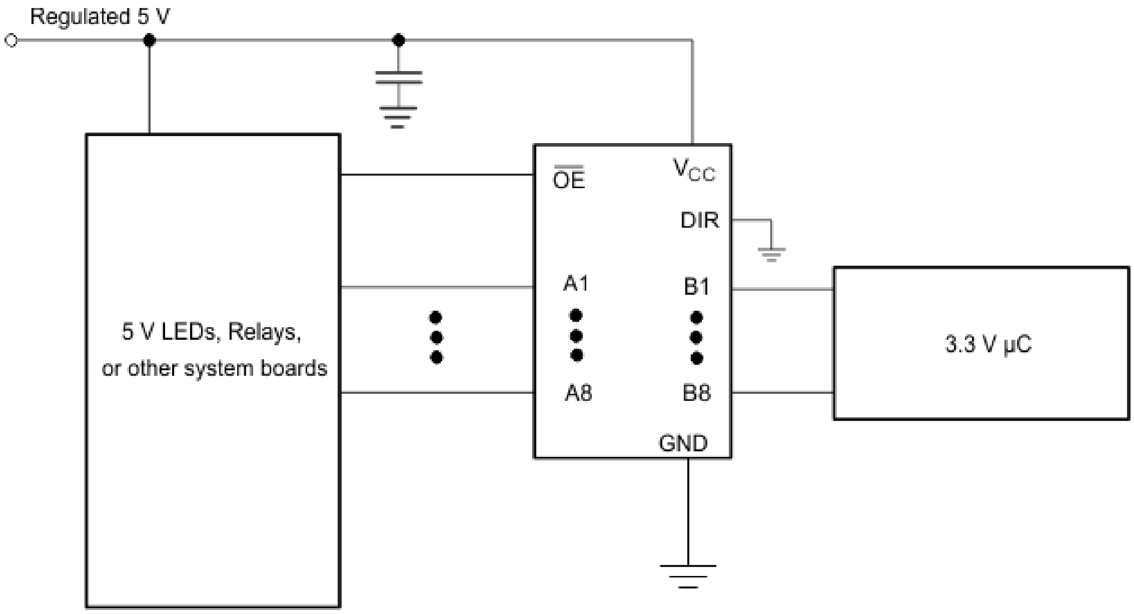


Figure 9-1. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has a balanced output drive. Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommend output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

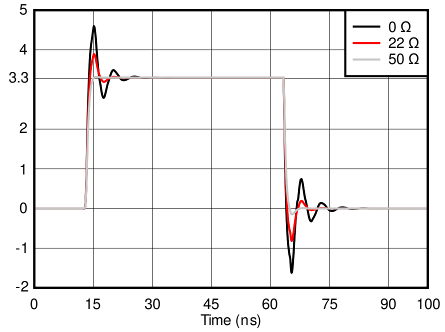


Figure 9-2. Typical Application Curve

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple VCC pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 9-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

9.4.2 Layout Example

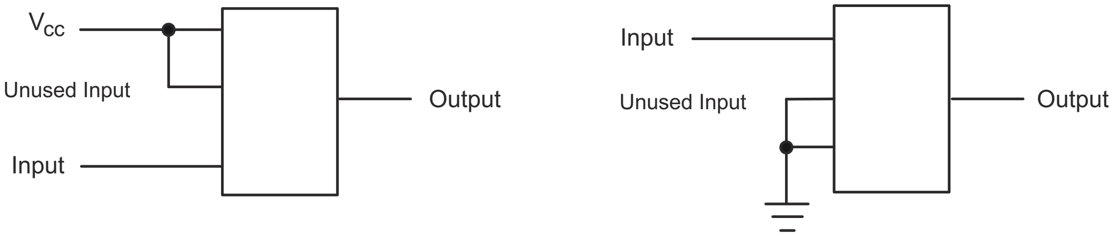


Figure 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9681901Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901Q2A SNJ54AHCT245FK
5962-9681901QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QRA SNJ54AHCT245J
5962-9681901QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QSA SNJ54AHCT245W
SN74AHCT245DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DBRG4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DGSR.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	AHCT245
SN74AHCT245DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT245N
SN74AHCT245N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHCT245N
SN74AHCT245NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245NSR.B	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	HB245
SN74AHCT245PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245PWRE4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245PWRG3	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245PWRG3.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	HB245

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHCT245PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245PWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB245
SN74AHCT245RGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB245
SN74AHCT245RGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HB245
SN74AHCT245RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT245
SN74AHCT245RKSR.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AHCT245
SNJ54AHCT245FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901Q2A SNJ54AHCT 245FK
SNJ54AHCT245FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901Q2A SNJ54AHCT 245FK
SNJ54AHCT245J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QRA SNJ54AHCT245J
SNJ54AHCT245J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QRA SNJ54AHCT245J
SNJ54AHCT245W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QSA SNJ54AHCT245W
SNJ54AHCT245W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9681901QSA SNJ54AHCT245W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHCT245, SN74AHCT245 :

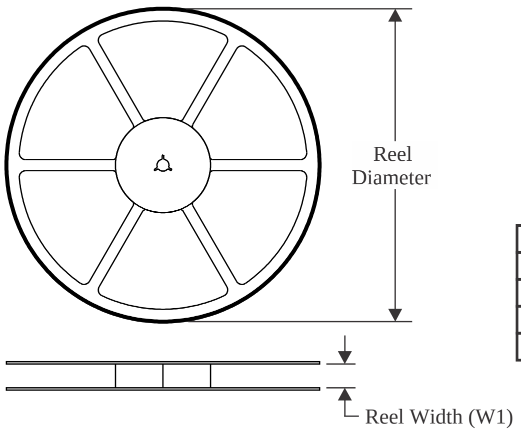
- Catalog : SN74AHCT245
- Automotive : SN74AHCT245-Q1, SN74AHCT245-Q1
- Enhanced Product : SN74AHCT245-EP, SN74AHCT245-EP
- Military : SN54AHCT245

NOTE: Qualified Version Definitions:

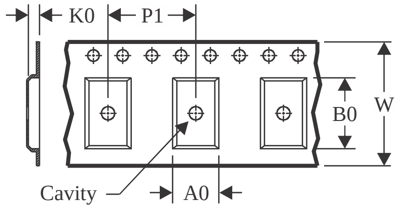
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

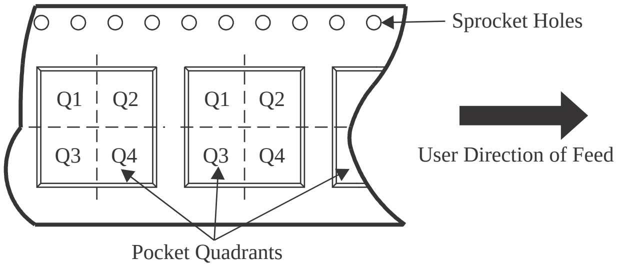


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

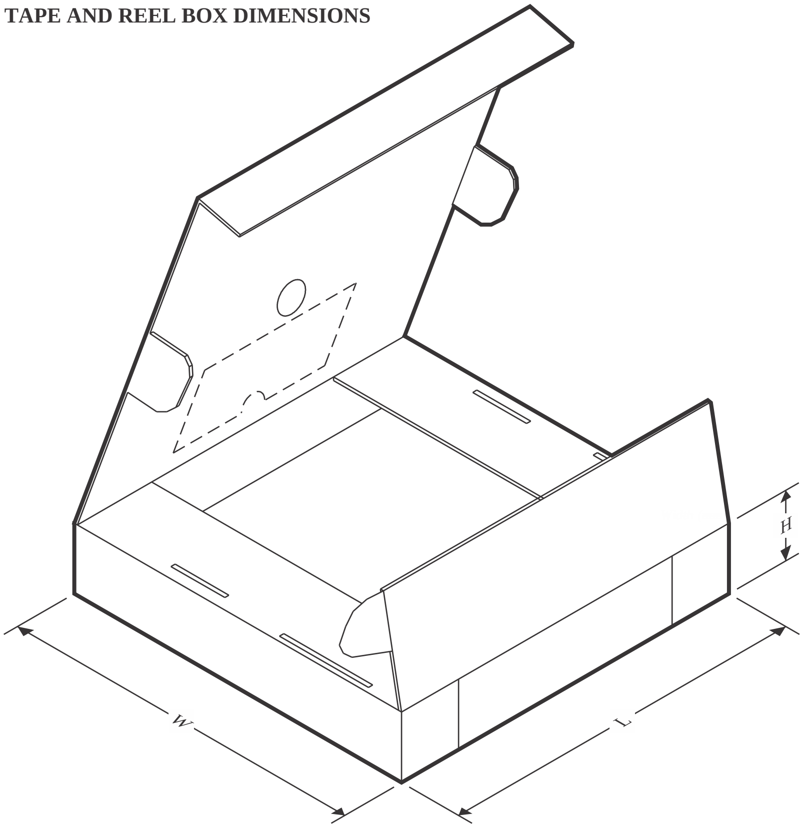
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT245DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHCT245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT245NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT245PWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT245RGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74AHCT245RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

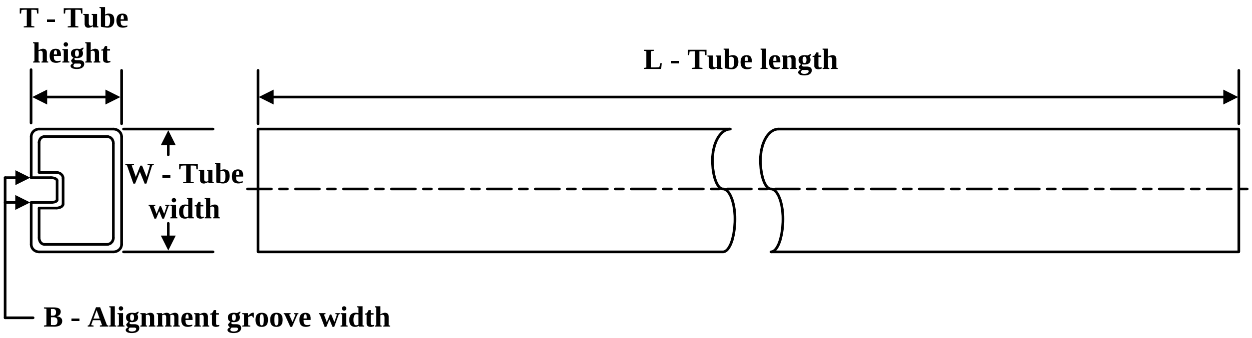
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT245DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT245DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHCT245DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHCT245DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT245NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHCT245PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT245PWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT245PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT245RGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74AHCT245RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE

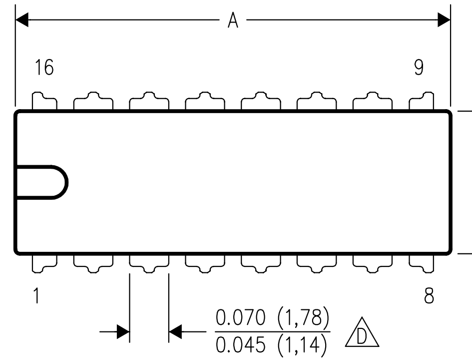


*All dimensions are nominal

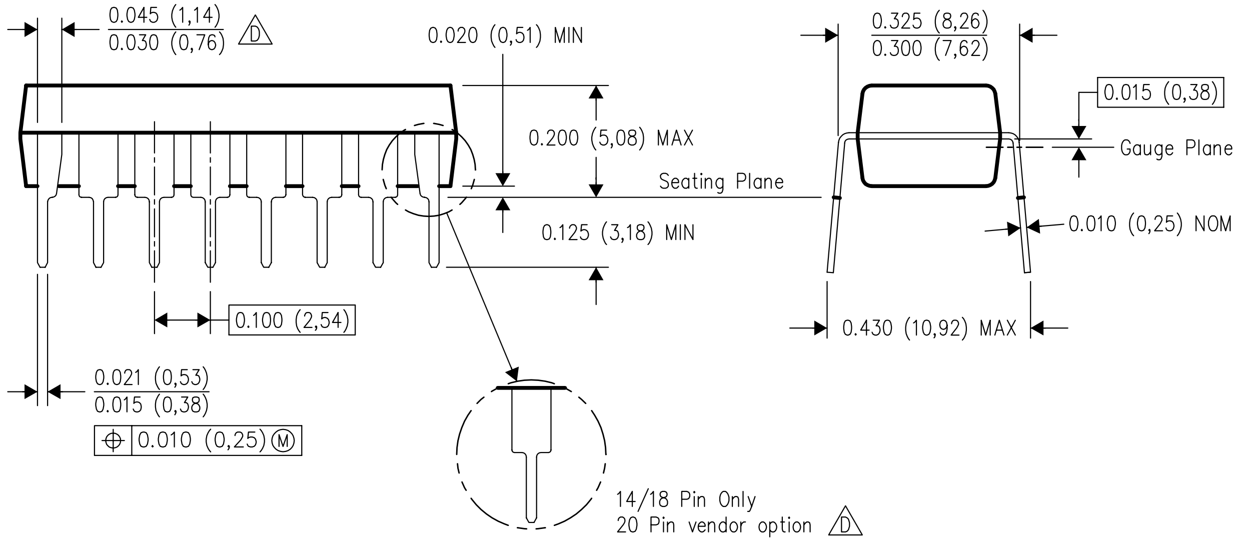
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9681901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9681901QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHCT245N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT245FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT245FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT245W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHCT245W.A	W	CFP	20	25	506.98	26.16	6220	NA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

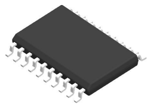


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

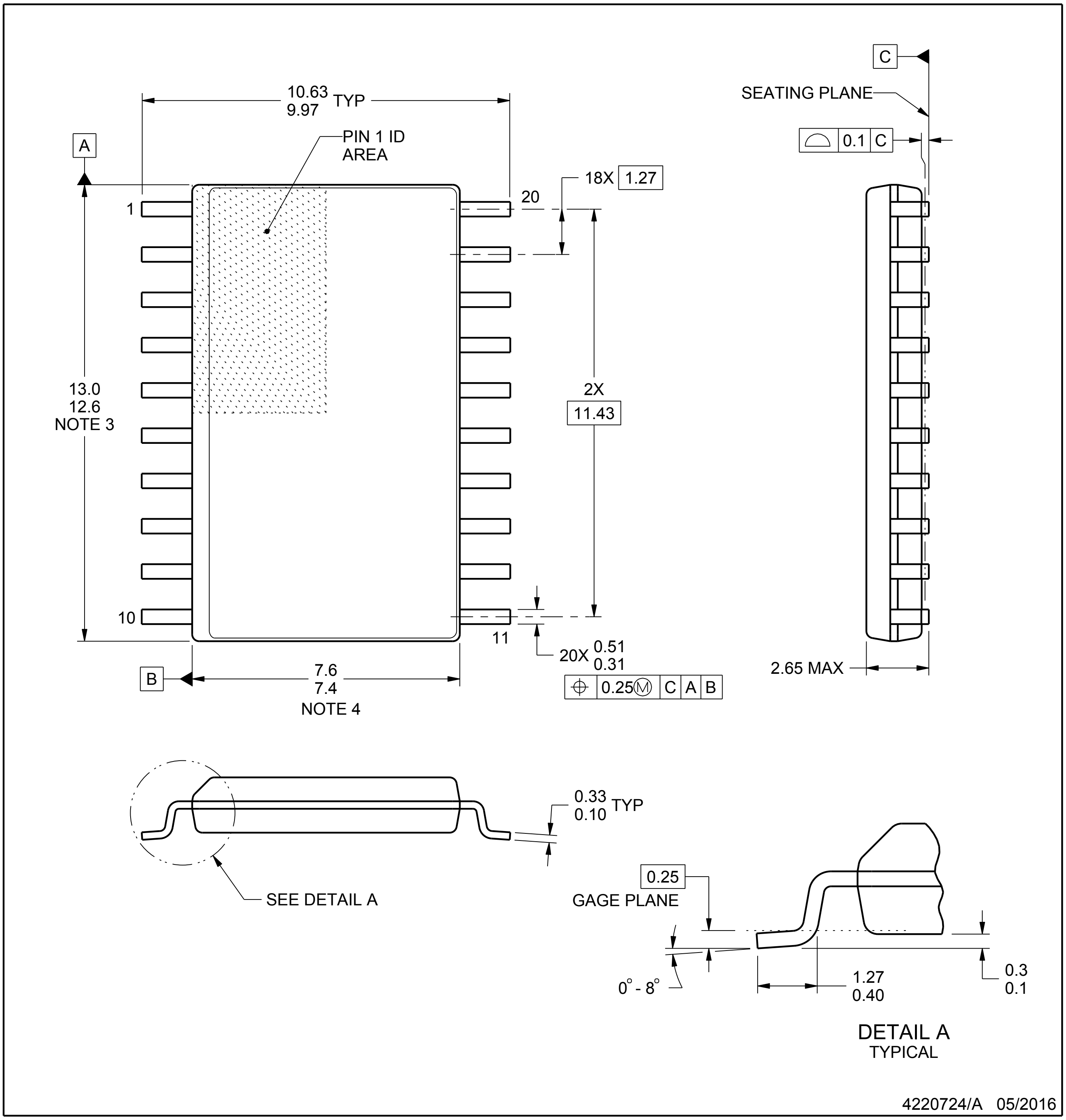


PACKAGE OUTLINE

DW0020A

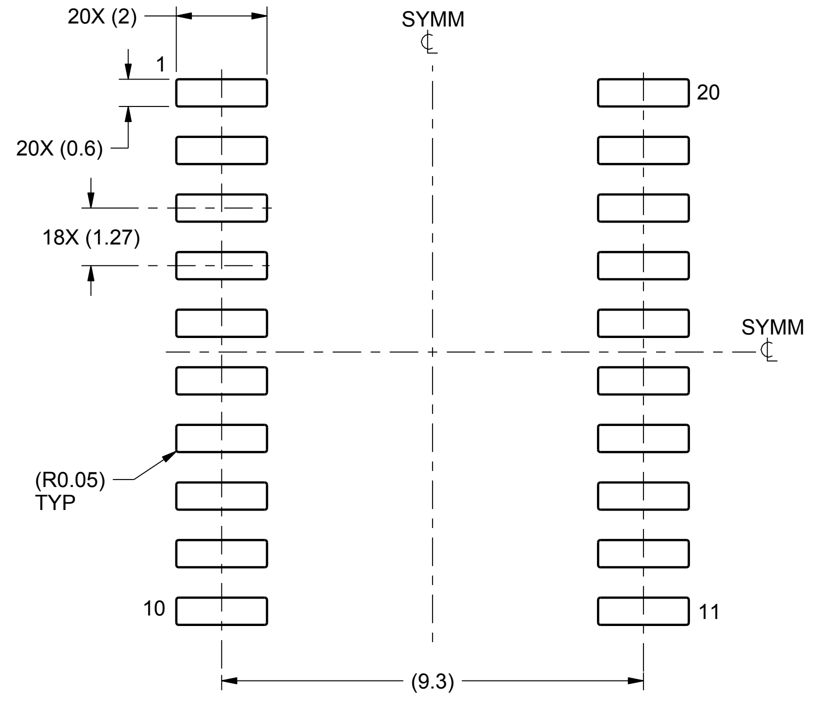
SOIC - 2.65 mm max height

SOIC

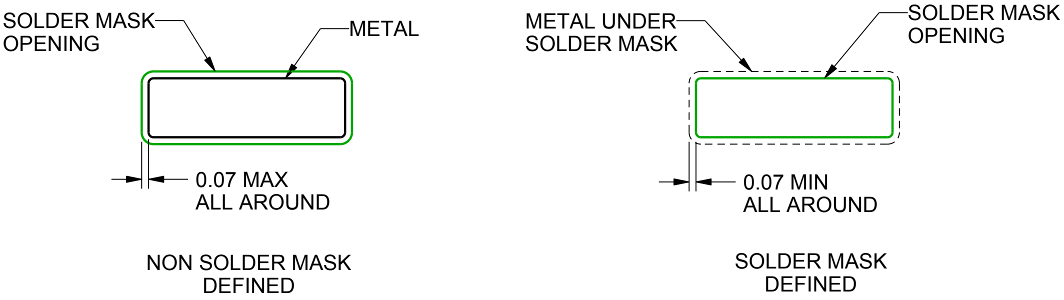


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

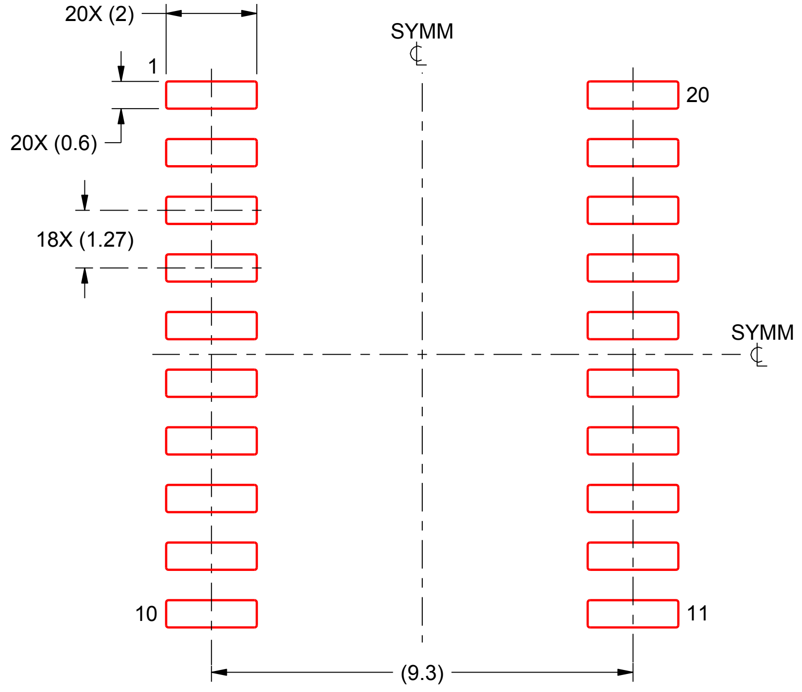


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



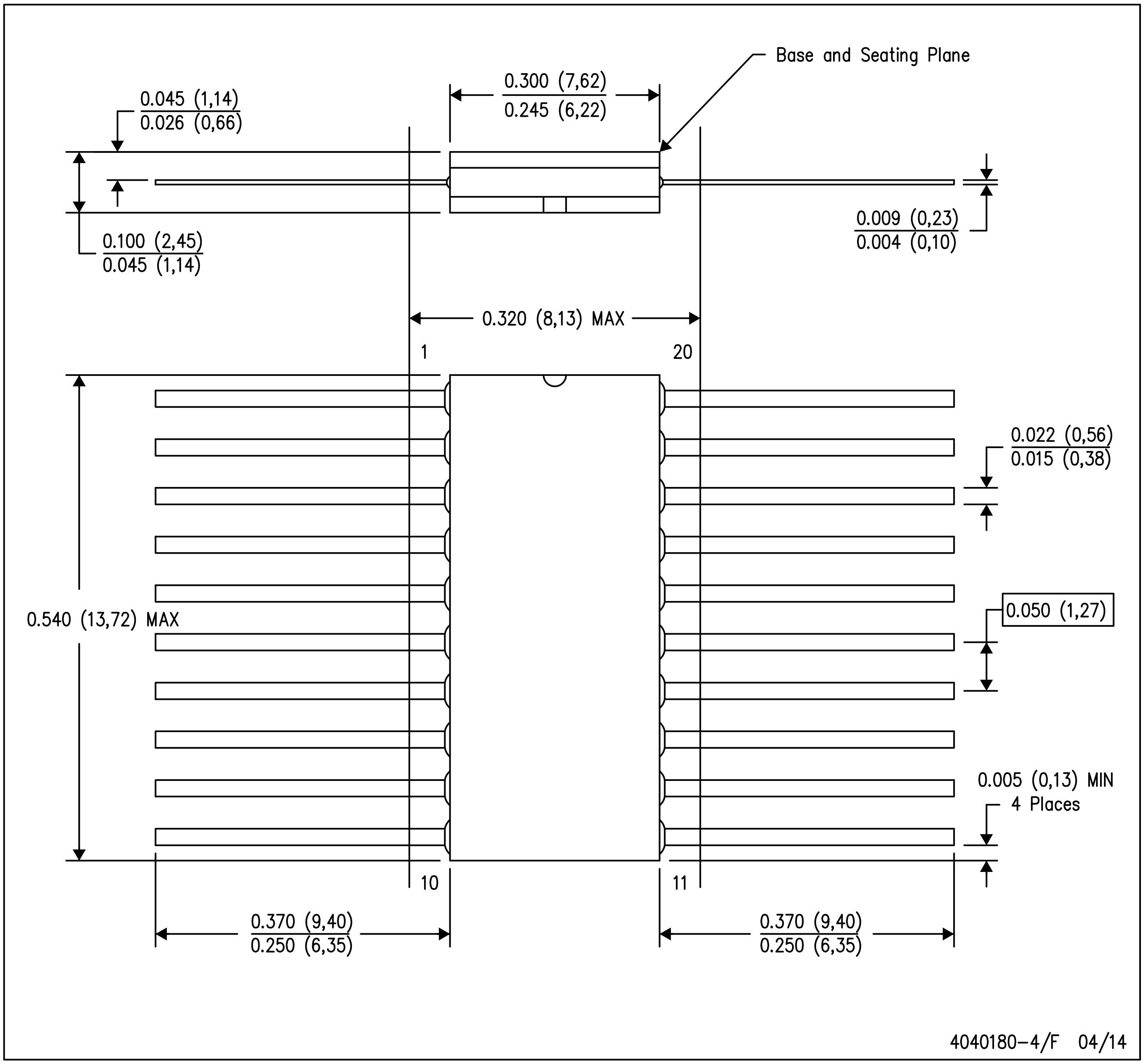
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

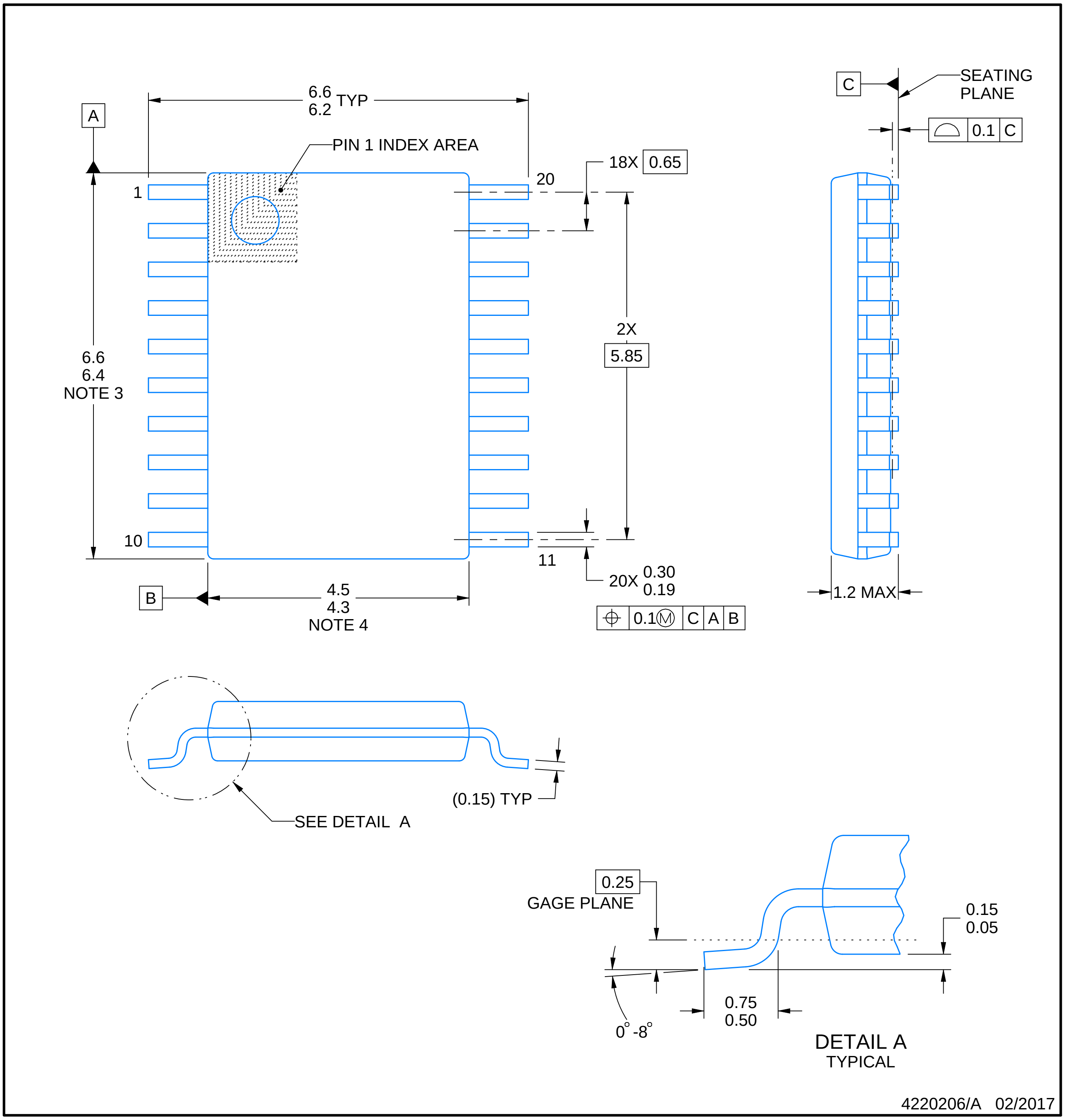


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

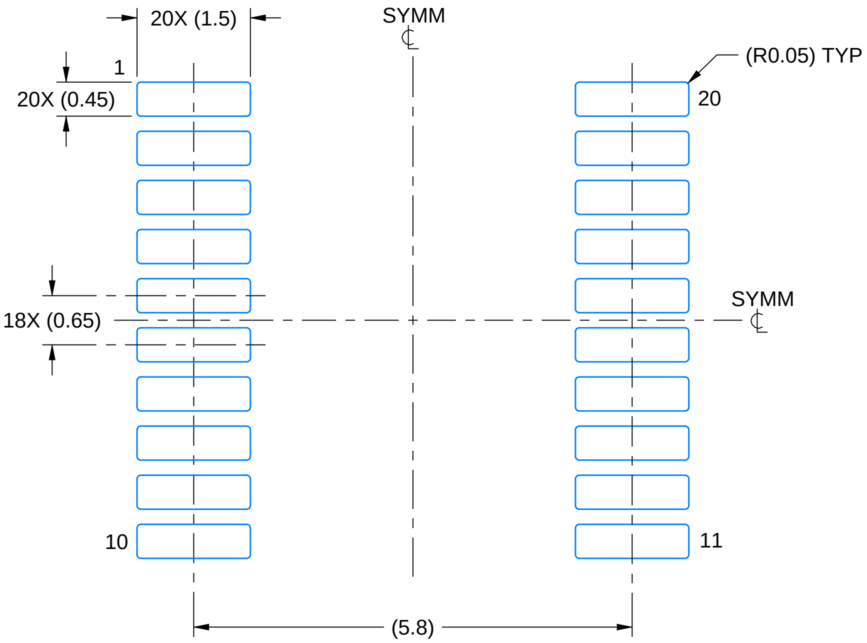
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

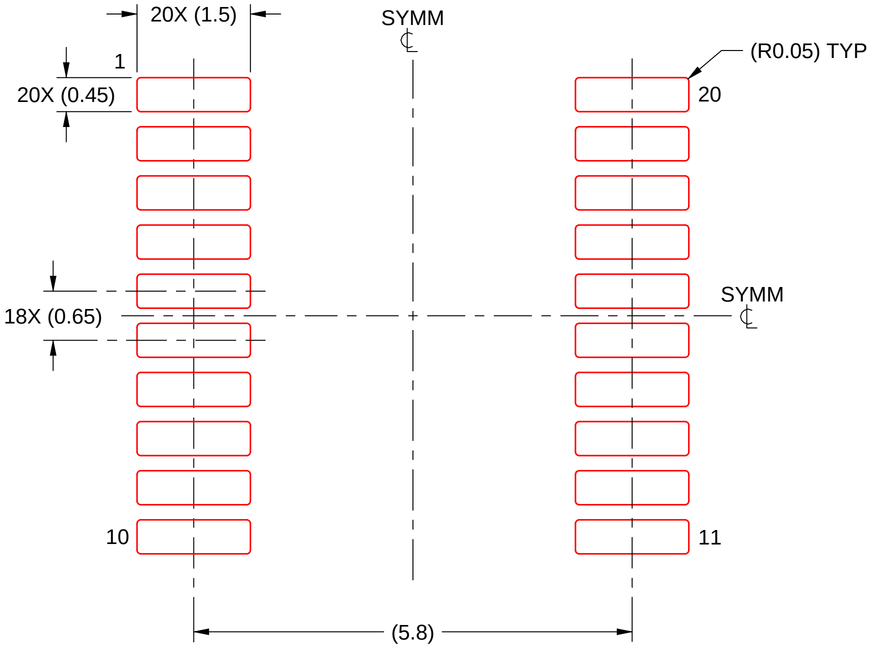
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

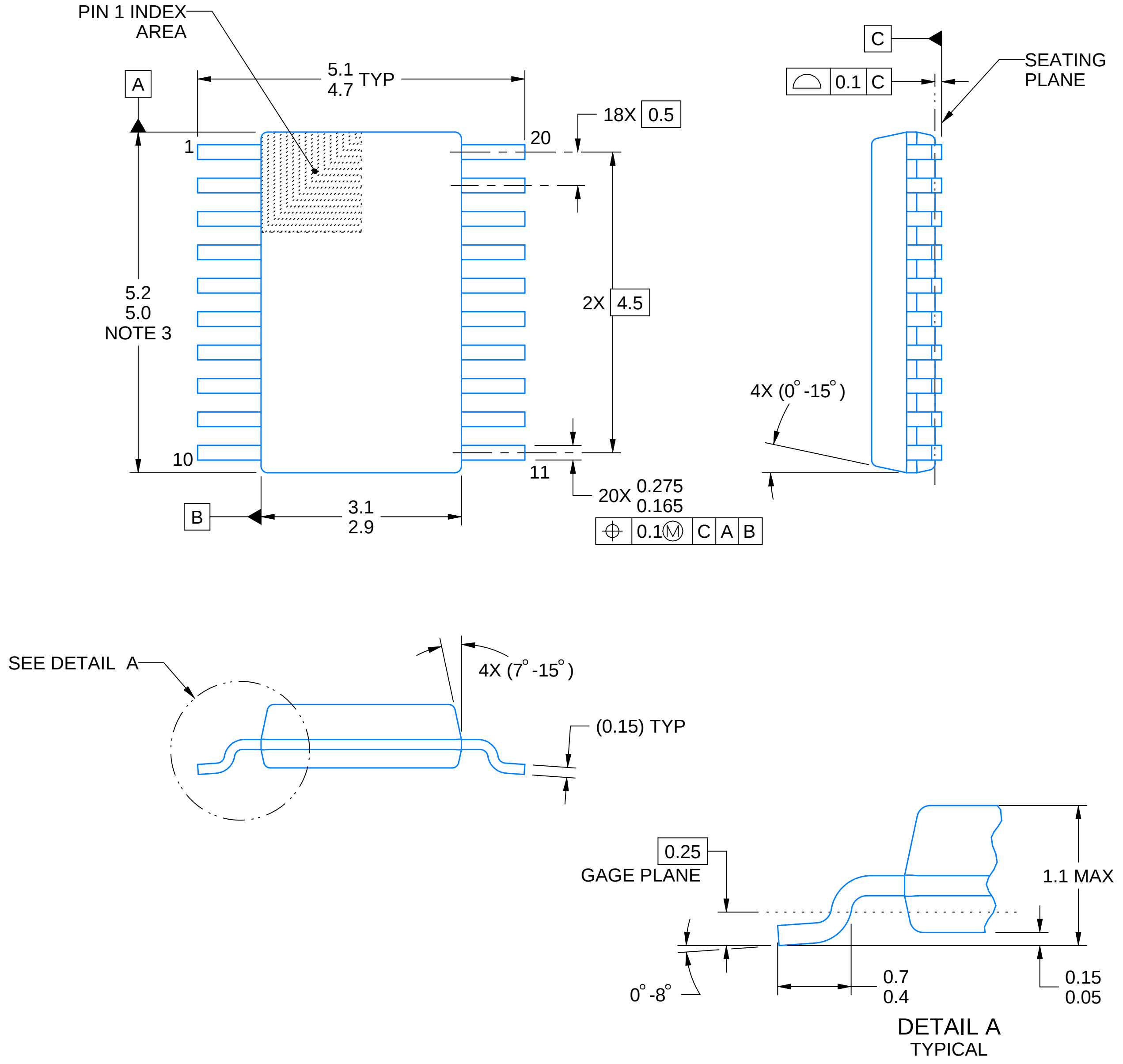
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

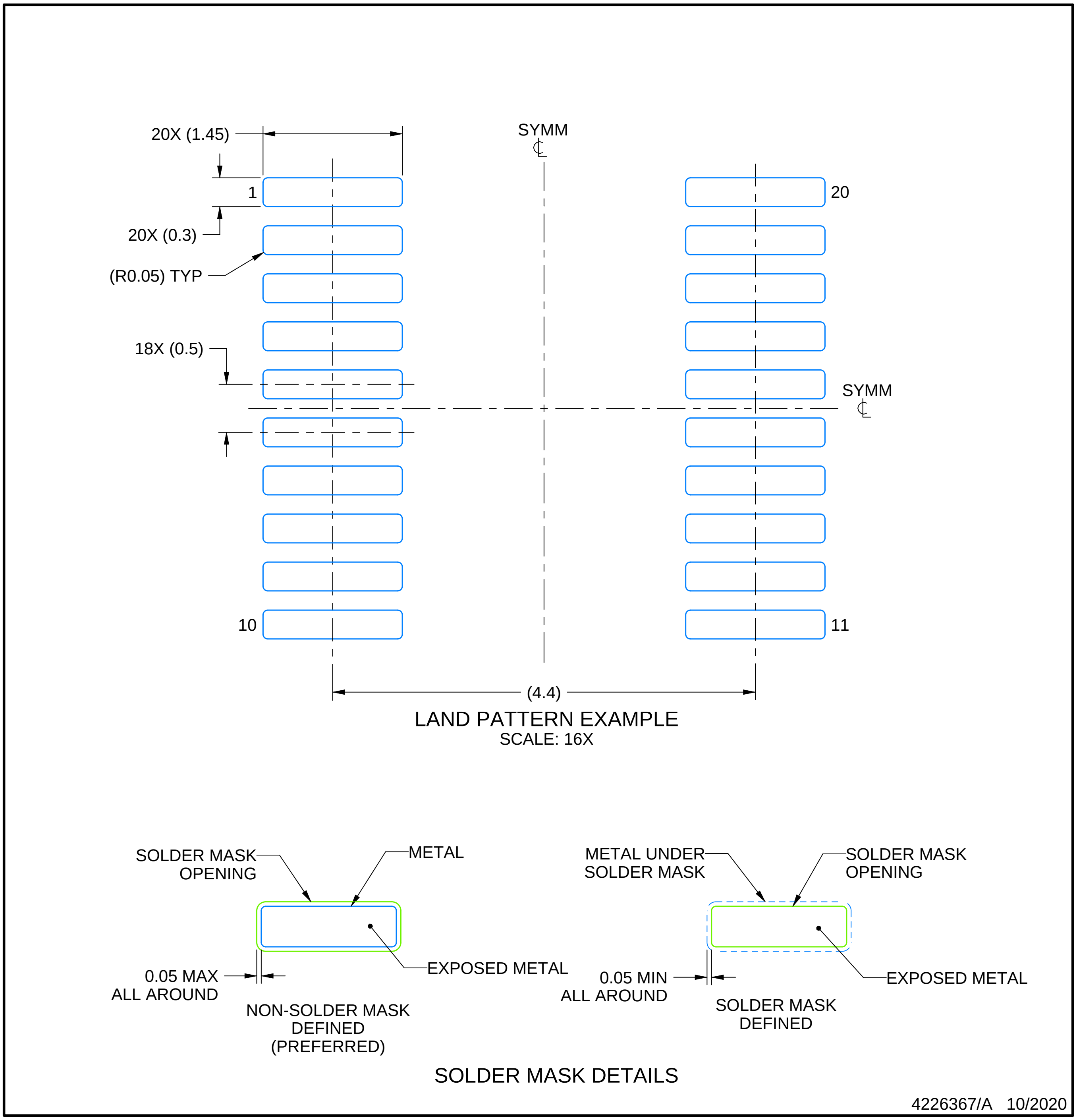


4226367/A 10/2020

PowerPAD is a trademark of Texas Instruments.

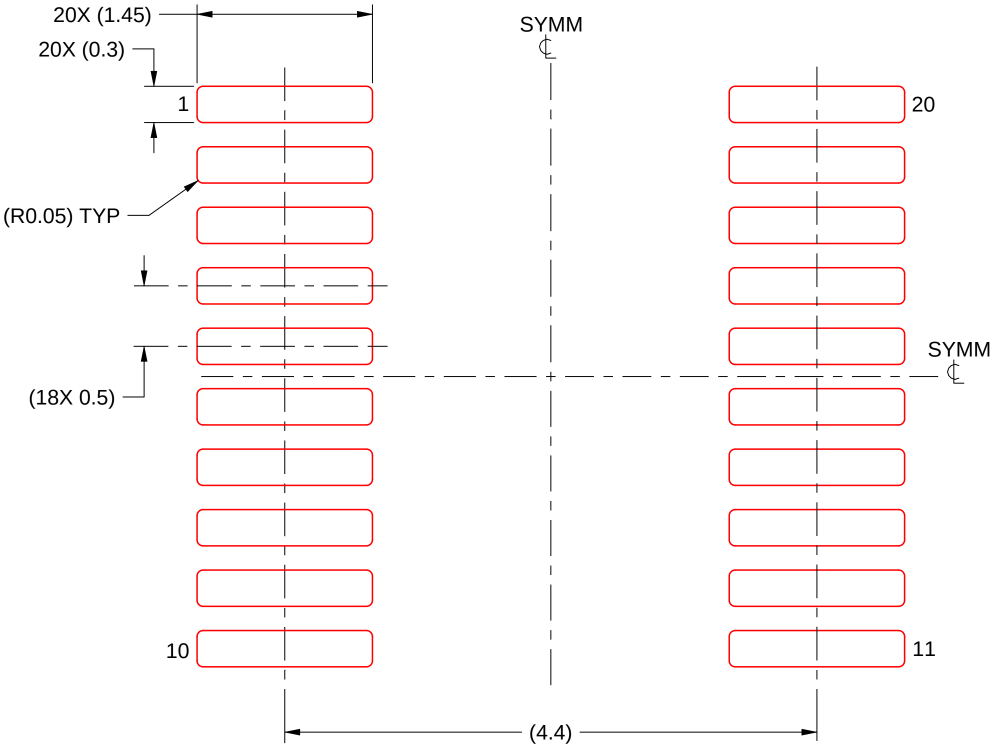
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



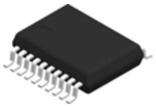
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

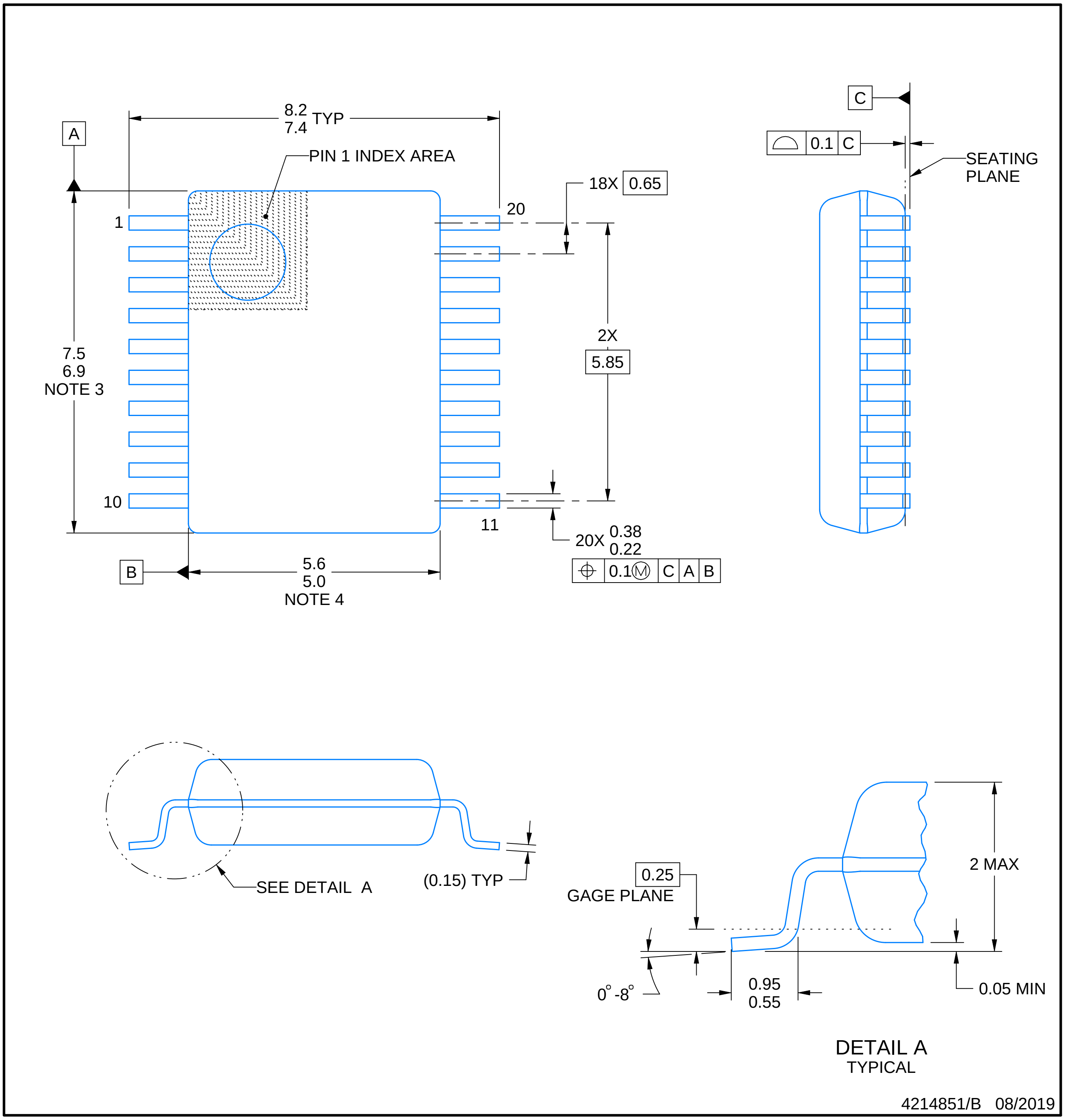
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

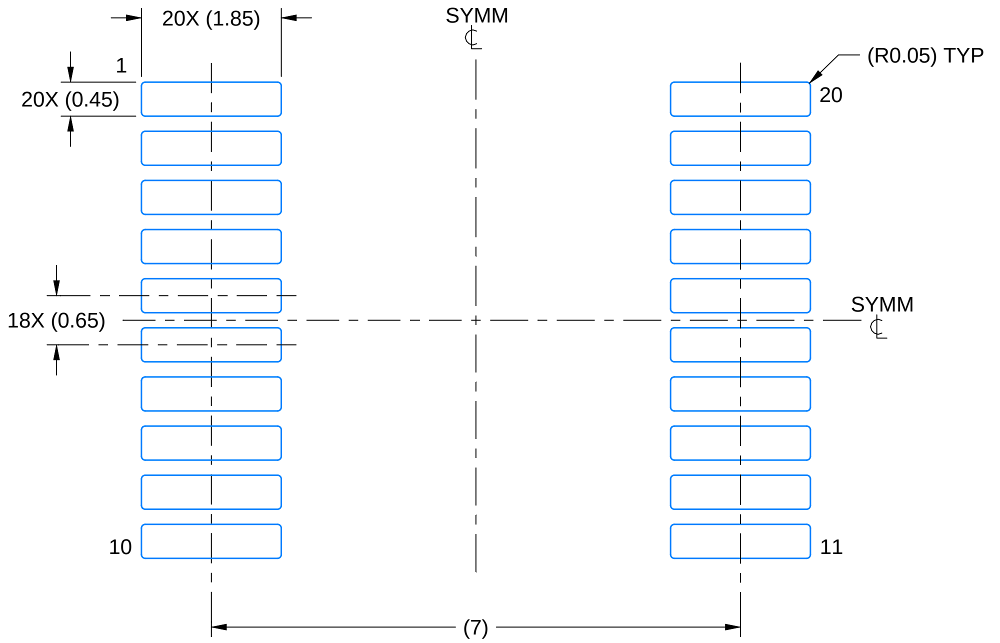


4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

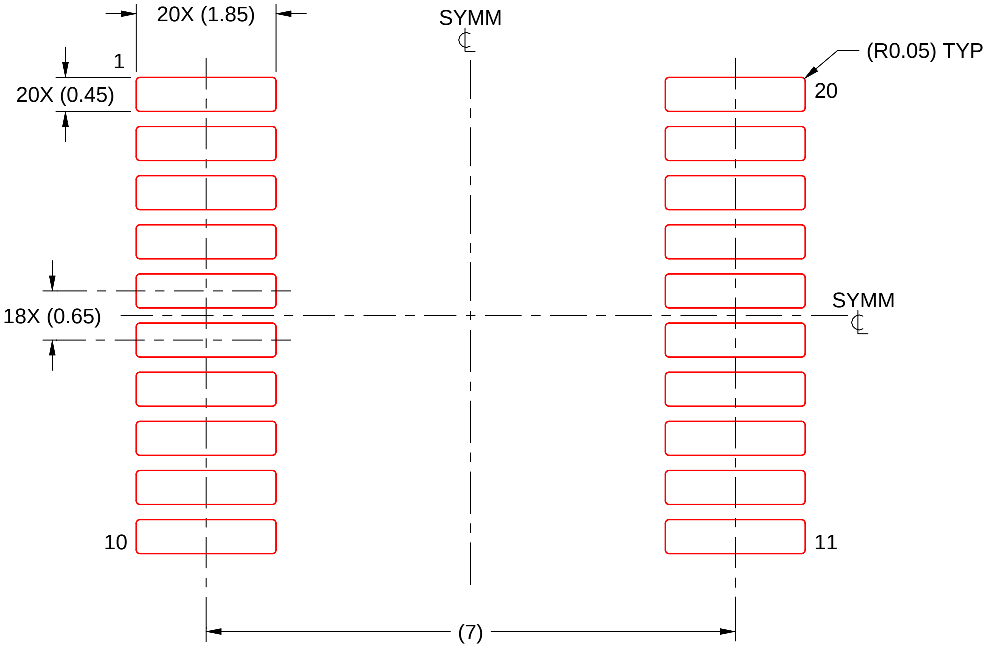
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

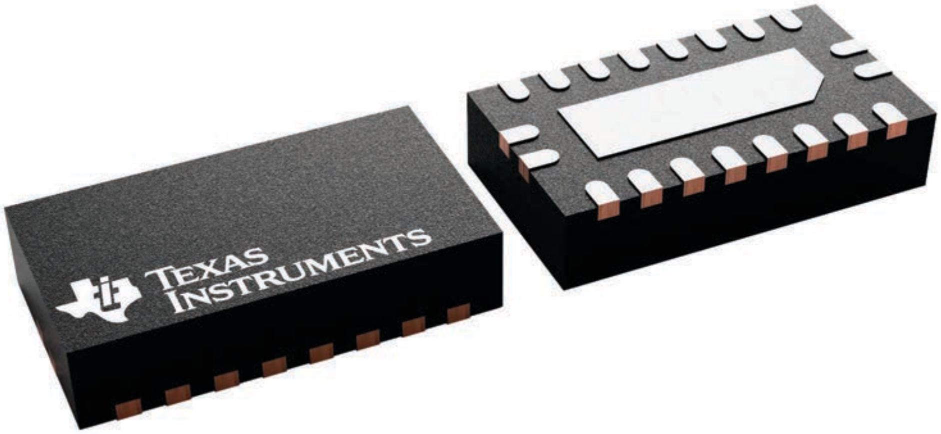
RKS 20

VQFN - 1 mm max height

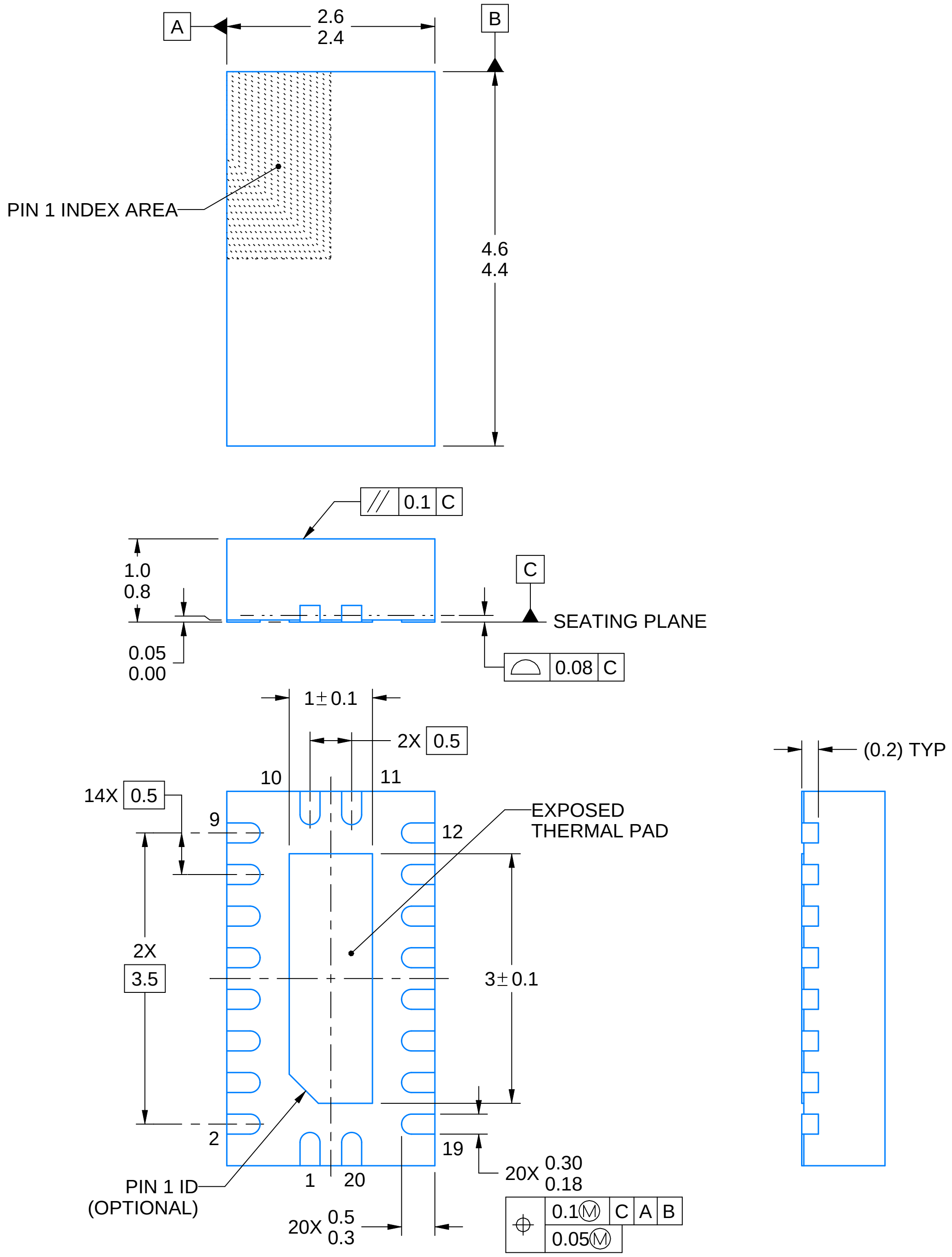
2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



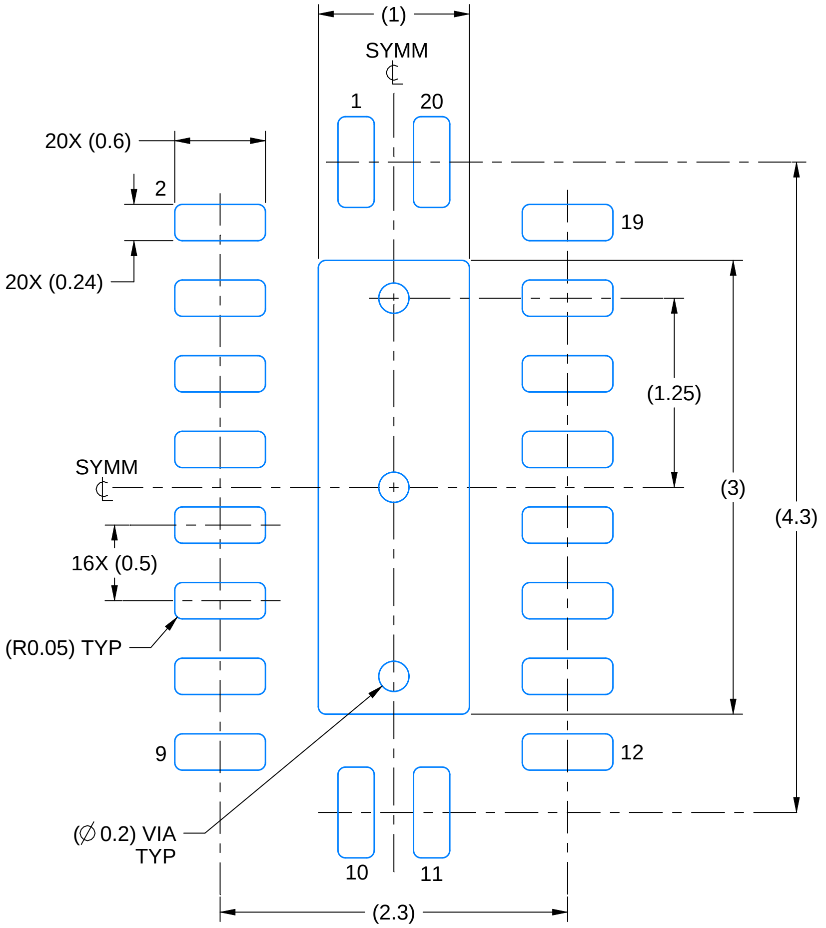
PACKAGE OUTLINE



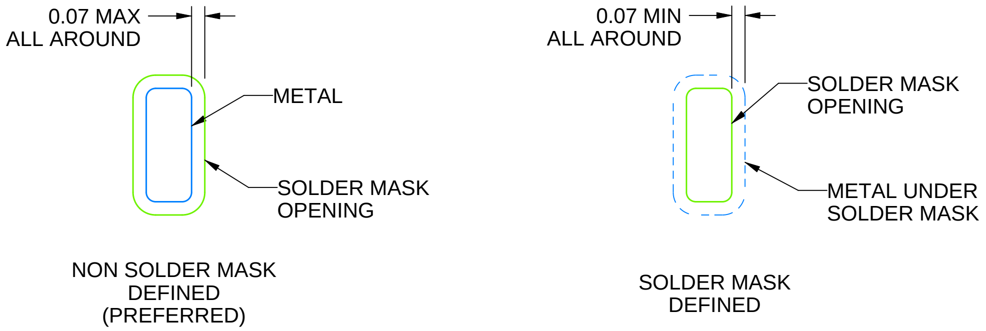
4222490/B 02/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

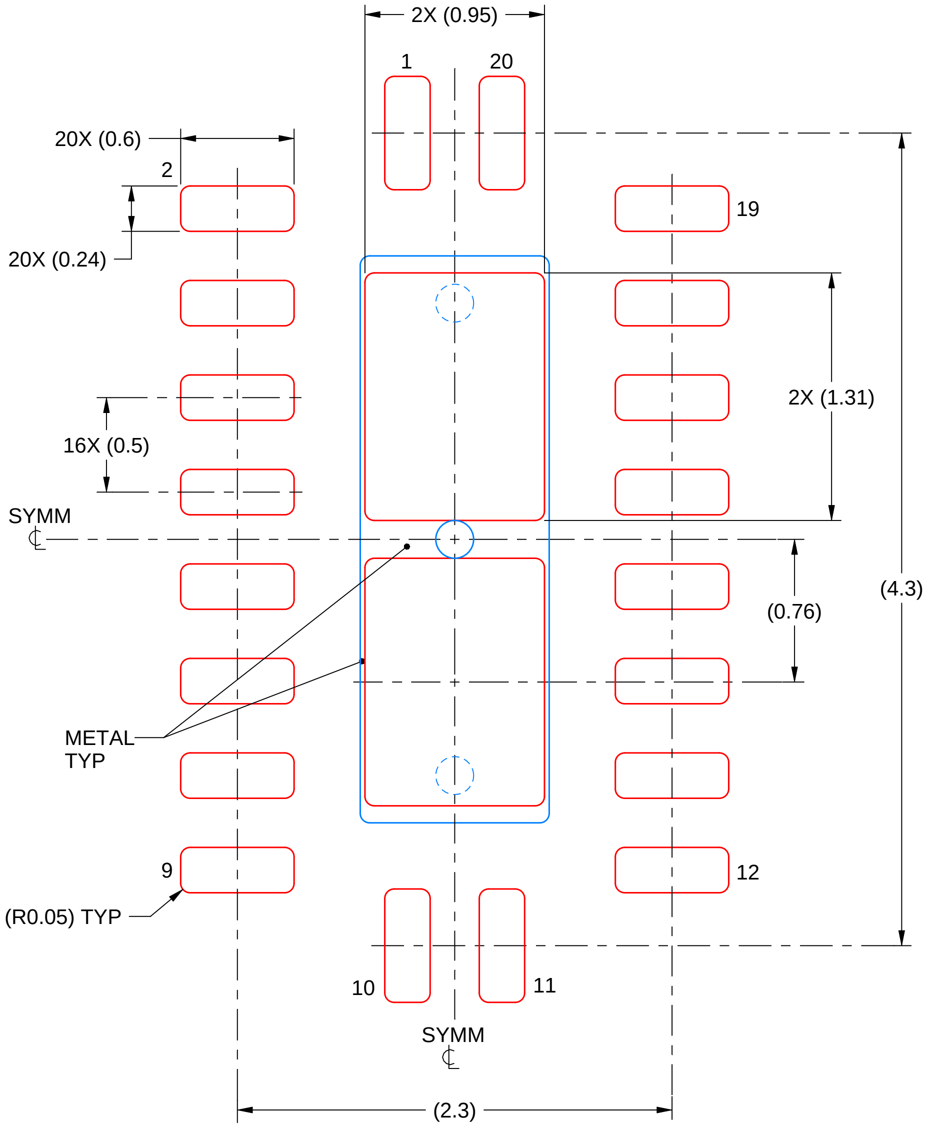


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

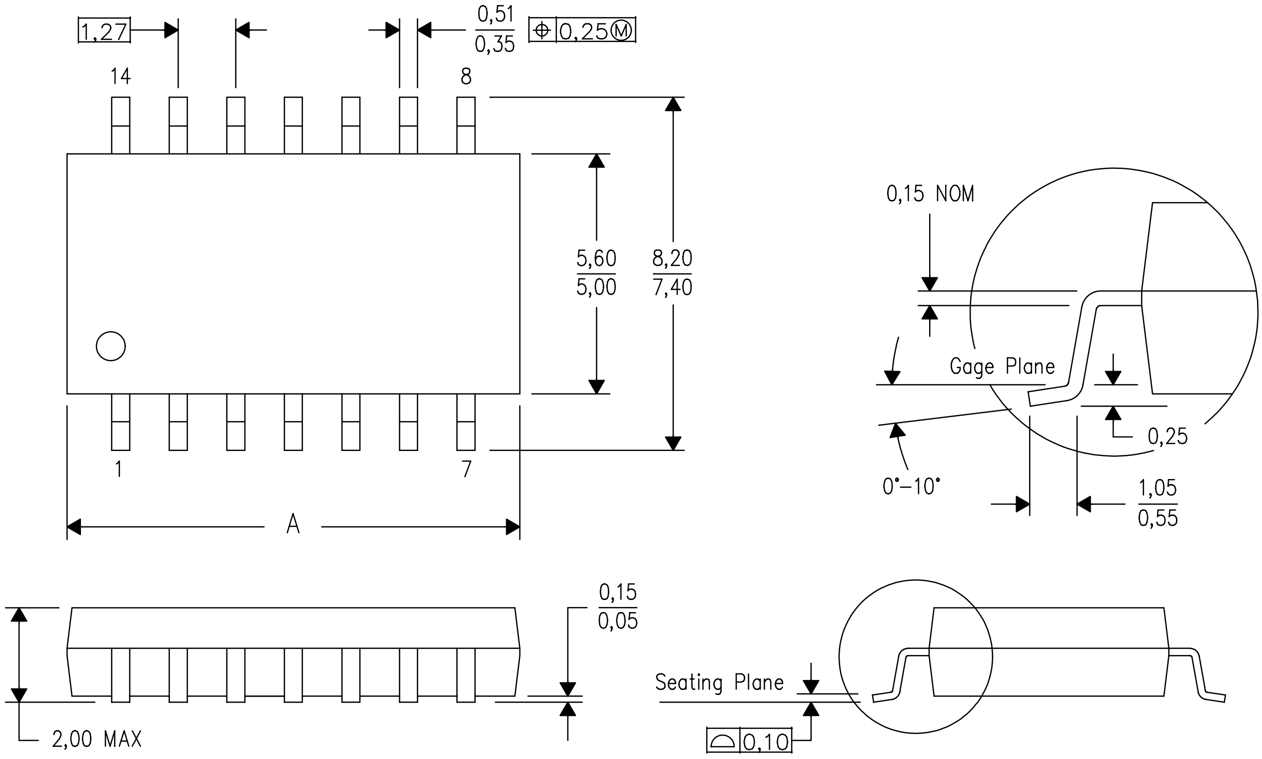
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

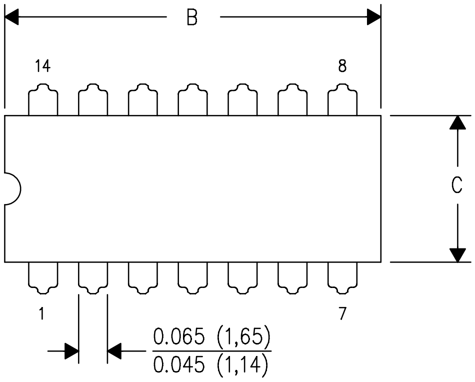
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

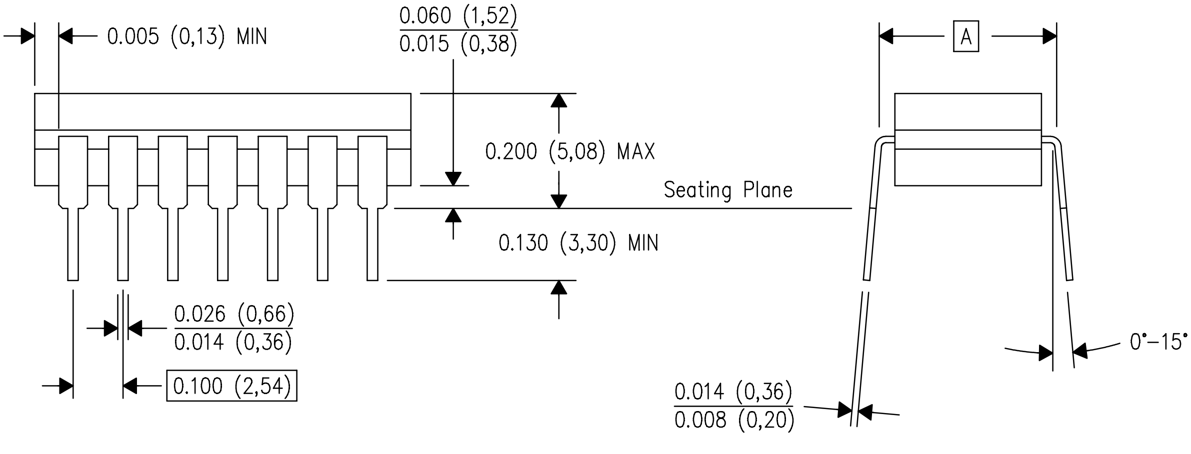
J (R−GDIP−T**)

CERAMIC DUAL IN−LINE PACKAGE

14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)





4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

GENERIC PACKAGE VIEW

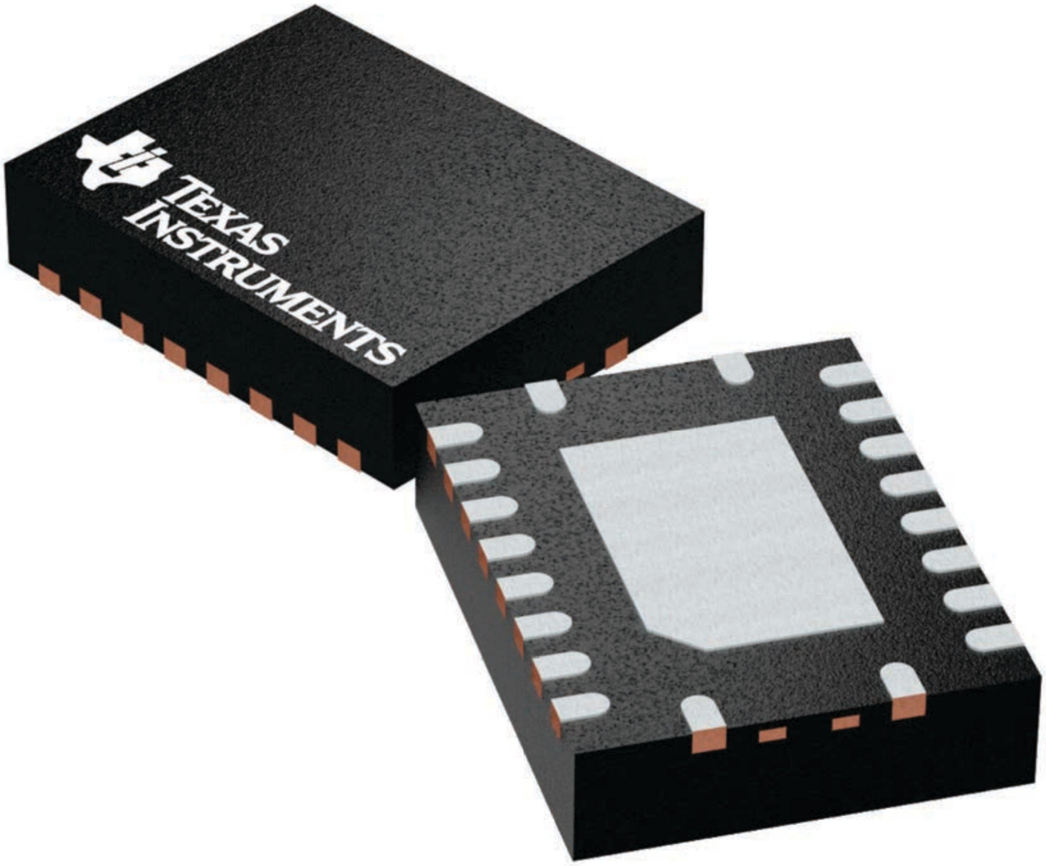
RGY 20

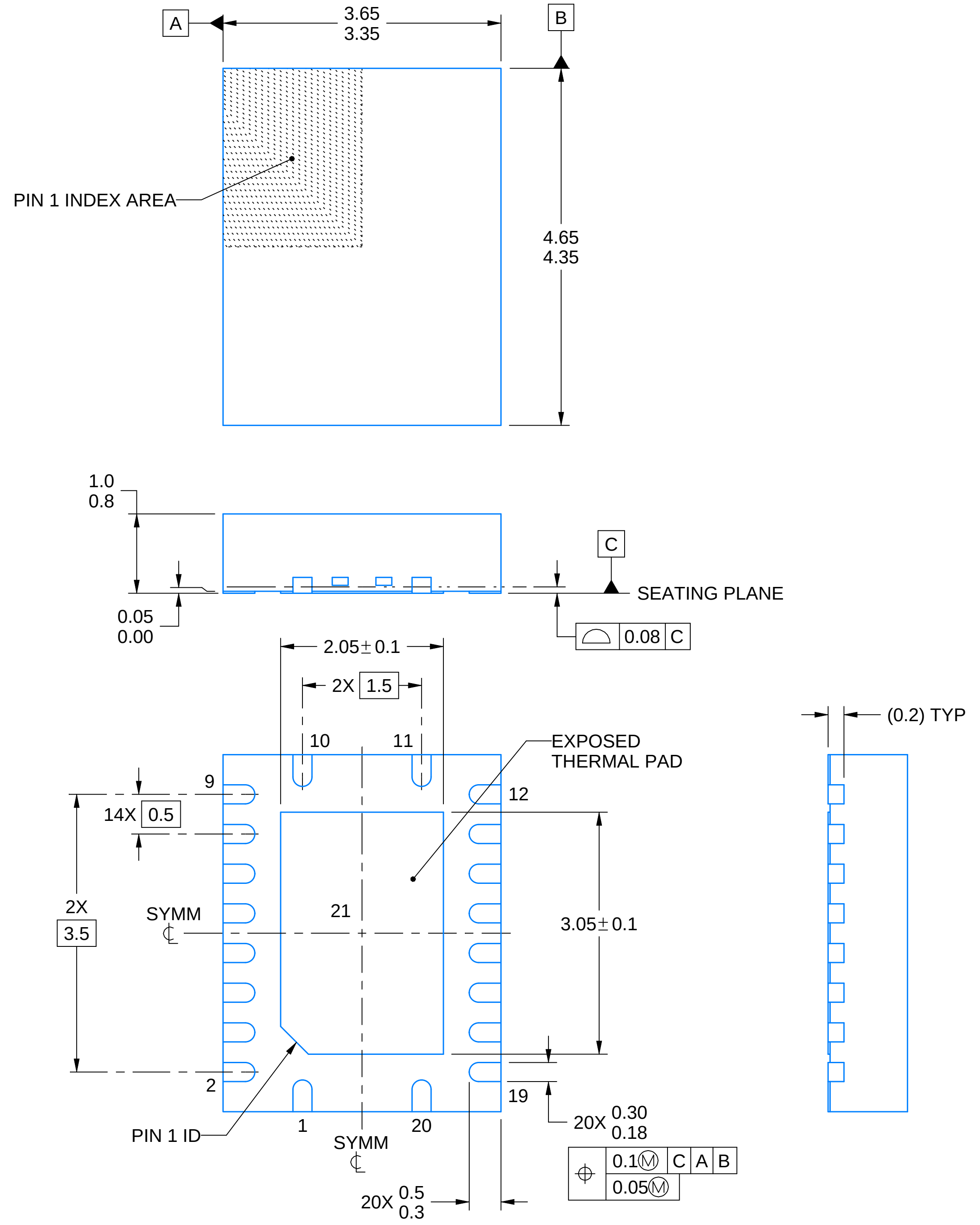
VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

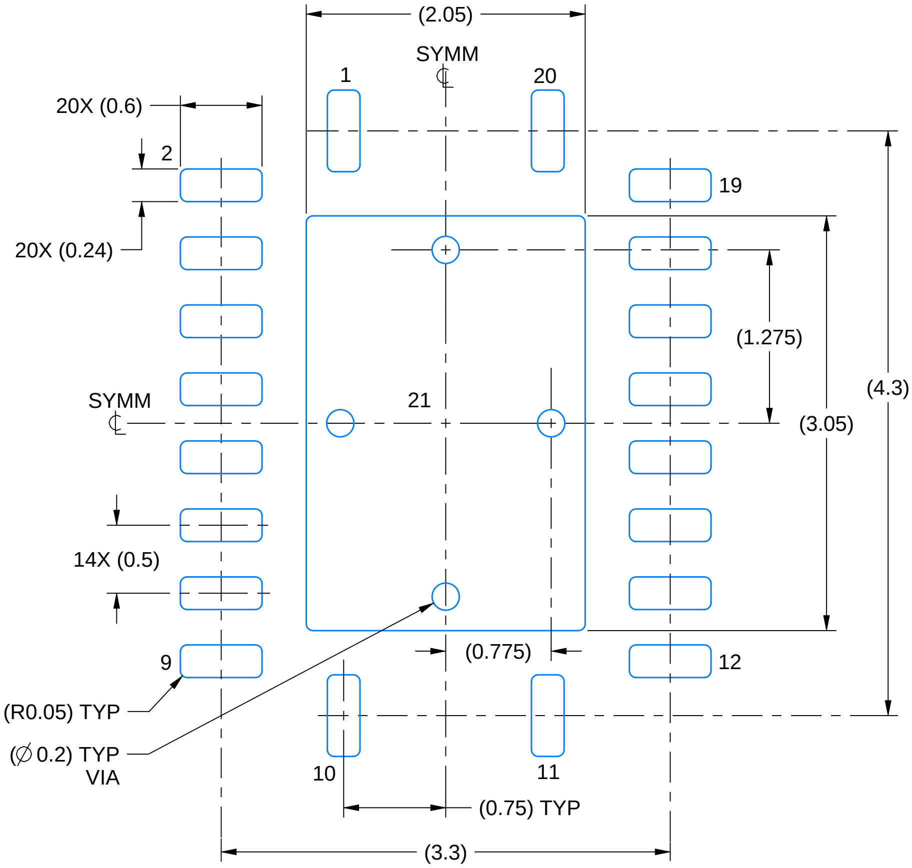




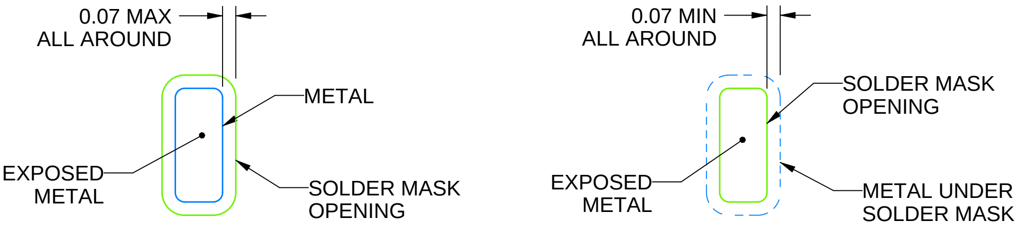
4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



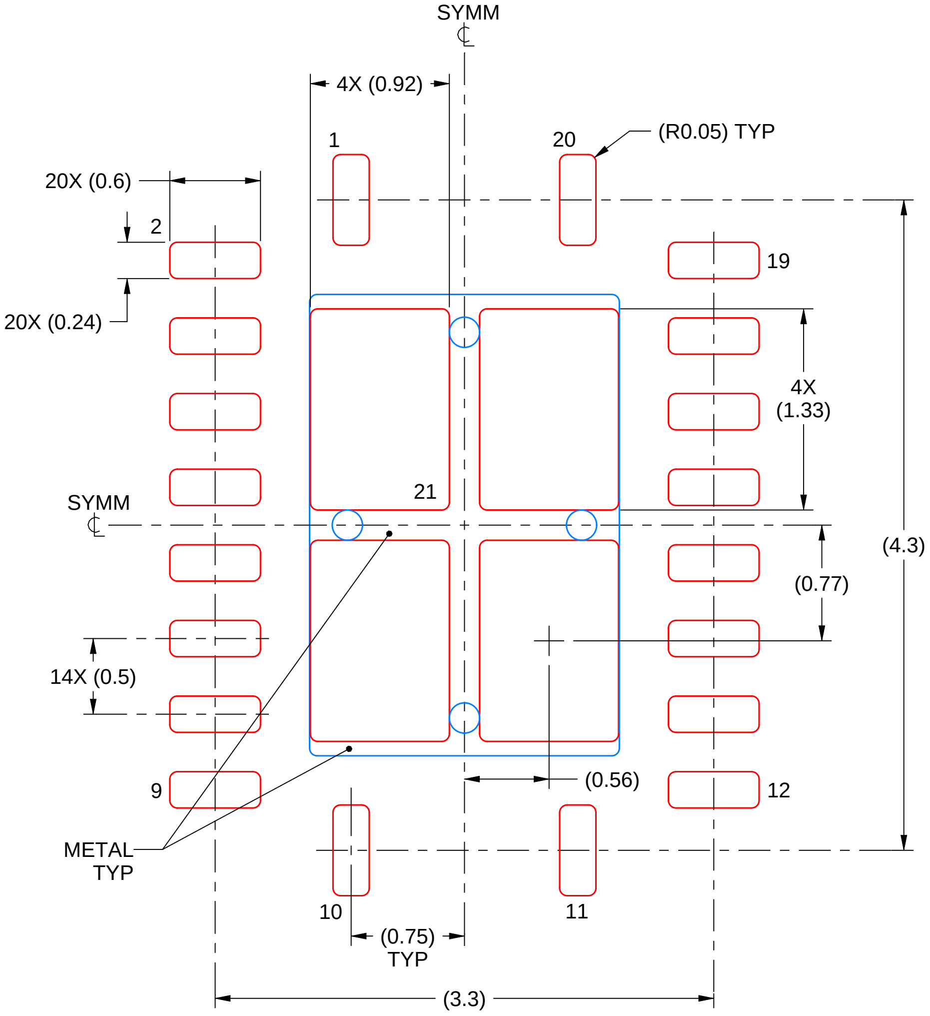
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

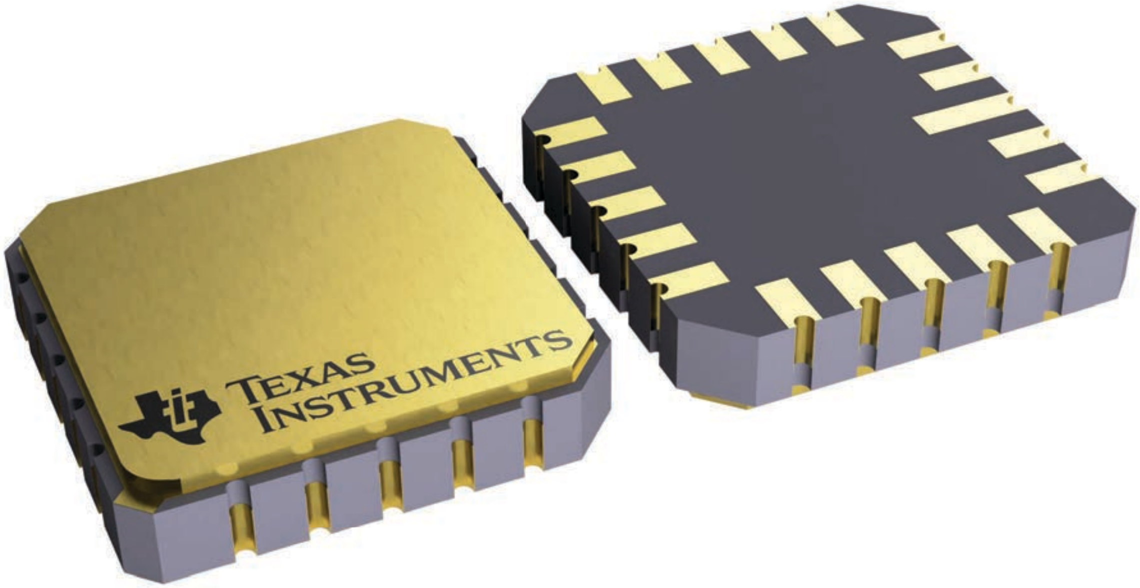
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

FK 20 **LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370\A\

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