



8K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 12/15 ns
- Low power consumption:
Operating current : 110/100/90/80mA (TYP.)
Standby current : 1mA (TYP.)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 28-pin 300 mil SOJ

GENERAL DESCRIPTION

The AS7C164A is a 65,536-bit high speed CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

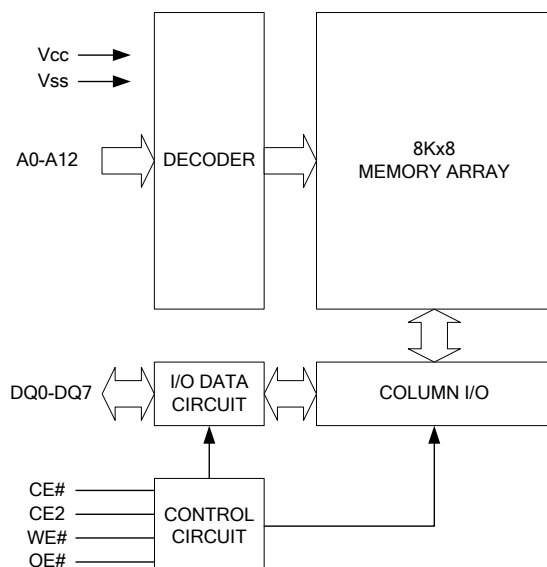
The AS7C164A is well designed for high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS7C164A operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
AS7C164A	0 ~ 70°C	4.5 ~ 5.5V	12/15ns	1mA	110/100/90/80mA

FUNCTIONAL BLOCK DIAGRAM

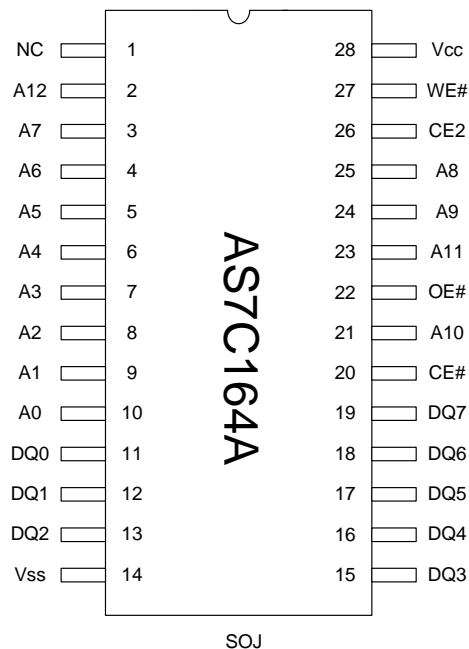


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



8K X 8 BIT HIGH SPEED CMOS SRAM

PIN CONFIGURATION**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T ^A	0 to 70(C grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC}
Read	L	H	L	H	D _{OUT}	I _{CC}
Write	L	H	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



8K X 8 BIT HIGH SPEED CMOS SRAM

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		4.5	5.0	5.5	V
Input High Voltage	V _{IH} ¹		2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ²		- 0.5	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IH} or V _{IL}	-12	90	160	mA
			-15	80	140	mA
			-	-	-	-
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-	1	5	mA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
 2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
 3. Over/Undershoot specifications are characterized, not 100% tested.
 4. Typical values are included for reference only and are not guaranteed or tested.
- Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA



8K X 8 BIT HIGH SPEED CMOS SRAM

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	AS7C164-12		AS7C164-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	12	-	15	-	ns
Address Access Time	t _{AA}	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	ns

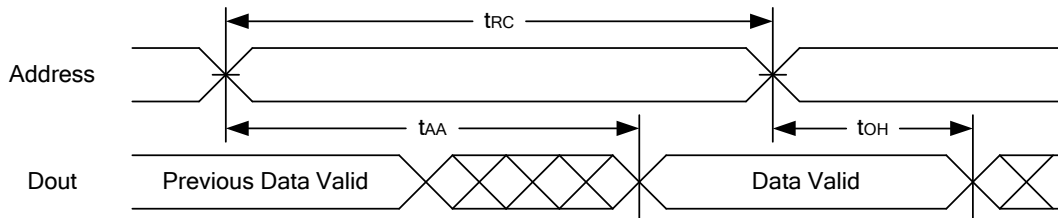
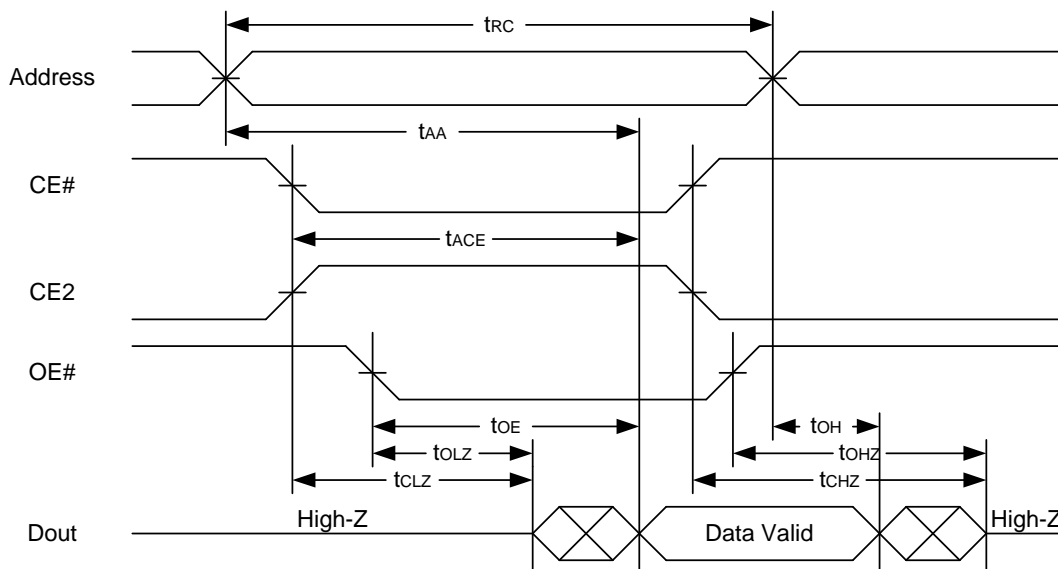
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C164-12		AS7C164-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.



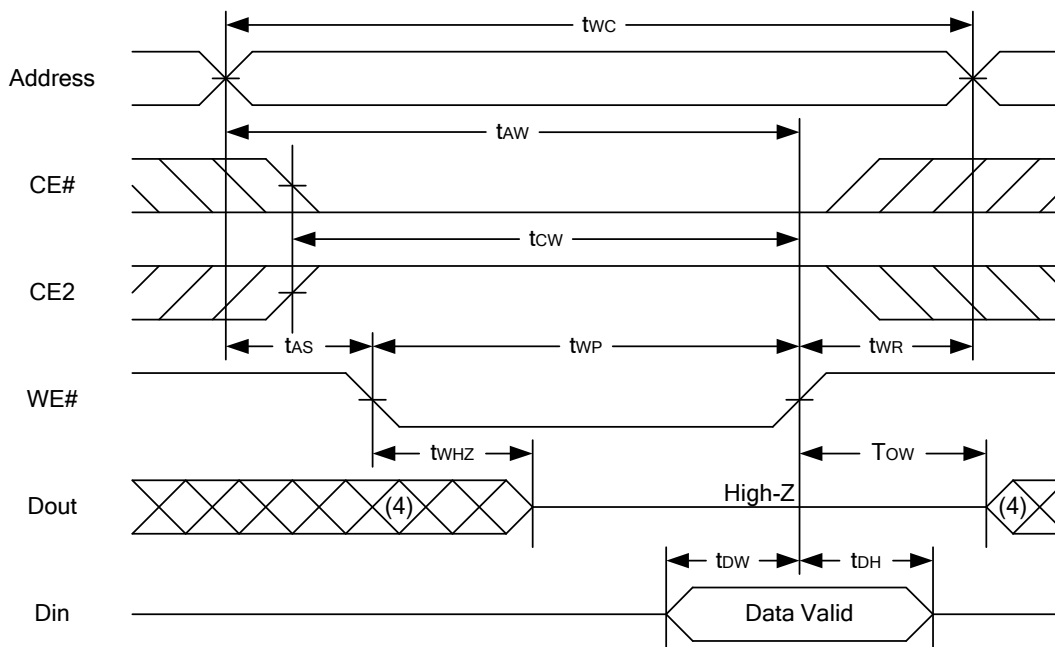
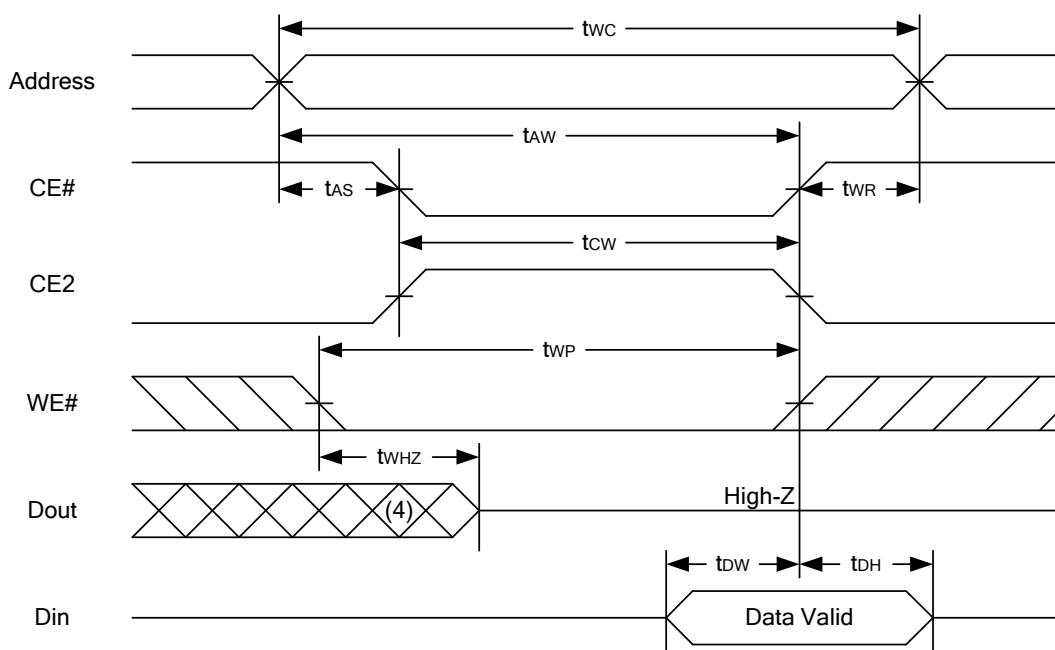
8K X 8 BIT HIGH SPEED CMOS SRAM

TIMING WAVEFORMS**READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)****Notes :**

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



8K X 8 BIT HIGH SPEED CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)****Notes :**

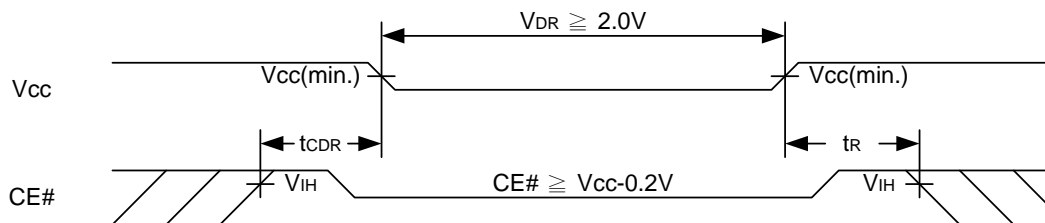
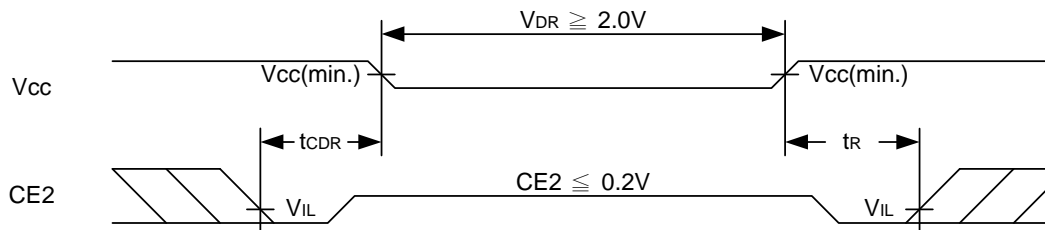
1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{wp} must be greater than $t_{whz} + t_{dw}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



8K X 8 BIT HIGH SPEED CMOS SRAM

DATA RETENTION CHARACTERISTICS

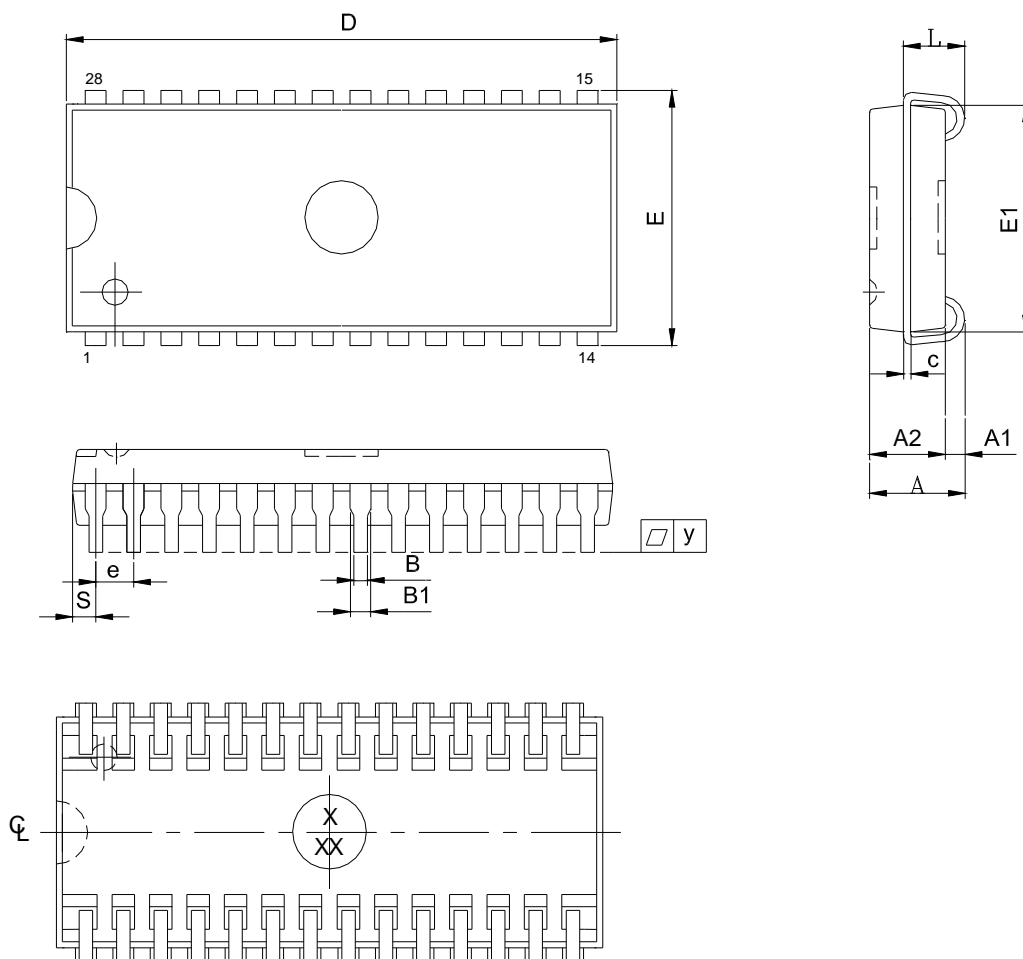
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# \geq V _{CC} - 0.2V or CE2 \leq 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# \geq V _{CC} - 0.2V or CE2 \leq 0.2V Others at 0.2V or V _{CC} -0.2V	-	0.6	3	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _r		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time**DATA RETENTION WAVEFORM****Low V_{CC} Data Retention Waveform (1)** (CE# controlled)**Low V_{CC} Data Retention Waveform (2)** (CE2 controlled)



8K X 8 BIT HIGH SPEED CMOS SRAM

28-pin 300 mil SOJ Package Outline Dimension



SYM. \ UNIT	INCH(REF)	MM(BASE)
A	0.140 (MAX)	3.556 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100±0.005	2.540±0.127
B	0.018±0.003	0.457±0.076
B1	0.028 ±0.003	0.711±0.076
c	0.010±0.003	0.254±0.076
D	0.710±0.010	18.03±0.254
E	0.337±0.010	8.560±0.254
E1	0.300±0.005	7.620±0.127
e	0.050±0.003	1.270±0.076
L	0.087±0.010	2.210±0.254
S	0.030±0.004	0.762±0.102
Y	0.003 (MAX)	0.076 (MAX)

Note : 1.S/E/D dimension is not including mold flash.

2.The end flash in package lengthwise is not more than 10 mils each side.

**8K X 8 BIT HIGH SPEED CMOS SRAM**

ORDERING INFORMATION

Package/Access Time	Temperature	12 ns	15 ns
28-pin 300 mil SOJ	Commercial	AS7C164A-12JCN	AS7C164A-15JCN

PART NUMBERING SYSTEM

AS7C		164A	-XX	J	C	X
SRAM prefix	Voltage: 5V supply	Device Number	Access Time	J = SOJ, 300 mil	Temperature Range: C = 0 ~ 70 C	N = Lead Free Part

**8K X 8 BIT HIGH SPEED CMOS SRAM**



Alliance Memory, Inc
551 Taylor Way,
San Carlos, CA 94070, USA
Phone: 650-610-6800
Fax: 650-620-9211

www.alliancememory.com

Copyright © Alliance Memory

All Rights Reserved

© Copyright 2009 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intellipart are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at anytime, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as expressly agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights, mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.