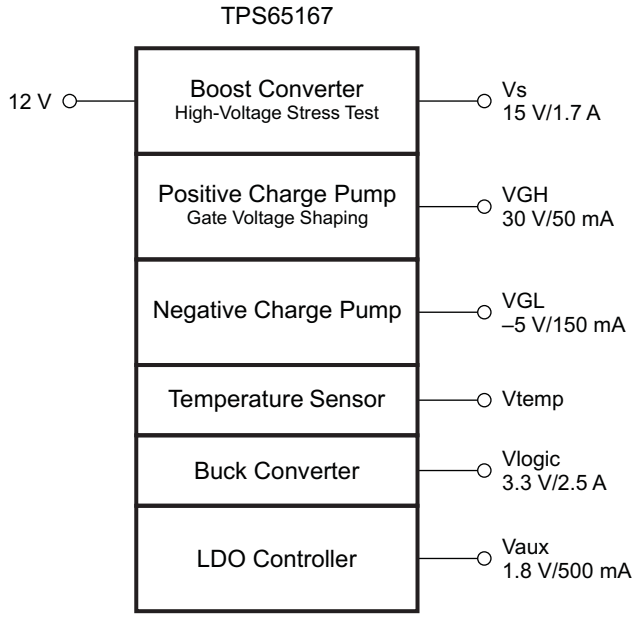
www.ti.com

SLVS760C – APRIL 2007 – REVISED MARCH 2008

# Compact LCD Bias Supply for TFT-LCD TV Panels

## FEATURES

- **6 V to 14 V Input Voltage Range**
- **Vs Output Voltage Range up to 19 V**
- **Boost Converter With 3.5-A Switch Current**
- **Boost Converter Overvoltage Protection**
- **2.5-A Step-Down Converter With 3.3-V Fixed or Adjustable Output**
- **750 kHz Fixed Switching Frequency**
- **150 mA Negative Charge Pump Driver for VGL**
- **50 mA Positive Charge Pump for VGH**
- **LDO Controller for Logic Supply**
- **Gate Voltage Shaping for VGH**
- **Temperature Sensor Output**
- **TPS65167 - High Voltage Stress Test Vs and VGH**
- **TPS65167A - High Voltage Stress Test Vs only**
- **Adjustable Sequencing**
- **Gate Drive Signal for Isolation Switch**
- **Short-Circuit Protection**
- **Internal Soft-start**
- **Thermal Shutdown**
- **Available in 6 × 6 mm 40 Pin QFN Package**




## APPLICATIONS

- **LCD TV Panel**
- **LCD Monitor**

## DESCRIPTION

The TPS65167 offers a compact power supply solution to provide all voltages required by a LCD panel for large size monitor and TV panel applications running from a 12-V supply rail.

The device generates all 3 voltage rails for the TFT LCD bias (Vs, VGL and VGH). In addition to that it includes a step-down converter and a LDO controller to provide two logic voltage rails. The device incorporates a high voltage switch that can be controlled by a logic signal from the external timing controller (TCON). This function allows gate voltage shaping for VGH. The device also features a high voltage stress test where the output voltage of VGH is set to typically 30 V and the output voltage of Vs is programmable to any higher voltage. The high voltage stress test is enabled by pulling the HVS pin high. The device consists of a boost converter to provide the source voltage Vs operating at a fixed switching frequency of 750 kHz. A fully integrated positive charge pump, switching automatically between doubler and tripler mode provides an adjustable regulated TFT gate on voltage VGH. A negative charge pump driver provides adjustable regulated output voltages VGL. To minimize external components the charge pumps for VGH and VGL operate at a fixed switching frequency of 1.5 MHz. The device includes safety features like overvoltage protection of the boost converter, short-circuit protection of VGH and VGL as well as thermal shutdown.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | High voltage Stress Test (HVS) | ORDERING | PACKAGE(2) | PACKAGE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | Available on Vs and VGH | TPS65167RHAR | 40 pin QFN | TPS65167 |
| | Available on Vs only | TPS65167ARHAR | | TPS65167A |

(1) The RHA package is available taped and reeled. Add R suffix to the device type (TPS65167RHAR) to order the device taped and reeled. The RHA package has quantities of 3000 devices per reel.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_I$ Voltage on pin | AVIN, VINB, SUPN, GD, BASE (2) | –0.3 to 16.5 | V |
| | EN, HVS, CTRL(2) | –0.3 to 6 | V |
| | FB, FBB, FBP, FBN, FBLDO, RSET(2) | –0.3 to 6 | V |
| | SW, SUP(2) | 25 | V |
| | SWB(2) | 20 | V |
| | POUT, VGH, DRN(2) | 36 | V |
| $T_J$ | Continuous power dissipation | See Dissipation Rating Table | |
| $T_{stg}$ | Operating junction temperature range | –40 to 150 | °C |
| | Storage temperature range | –65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATINGS(1)

| PACKAGE | $R_{\theta JA}$ | $T_A \le 25°C$ POWER RATING | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| 40 pin QFN | 30°C/W | 3.3 W | 1.8 W | 1.3 W |

(1) See the Texas Instruments Application report SLMA002 regarding thermal characteristics of the PowerPAD package.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 6 | | 14 | V |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |
| $C_{REG}$ | REGOUT bypass capacitor | | 4.7 | | µF |
| $C_{REF}$ | Reference (REF) bypass capacitor | | 100 | | nF |

## ELECTRICAL CHARACTERISTICS

AVIN=VINB=SUPN=12V, EN=REGOUT, Vs = 15V, Vlogic = 3.3V , Vaux = 1.8V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $V_I$ | Input voltage range | | 6 | | 14 | V |
| $I_Q$ | Quiescent current into AVIN | Not switching, FB = FB + 5% | | 1.5 | | mA |
| | Quiescent current into VINB | Not switching, FBB = FBB + 5% | | 0.15 | | mA |
| | Quiescent current into SUP | Not switching, FB = FBB = FBN = FBP = + 5% | | 275 | | µA |
| UVLO | Undervoltage lockout threshold | $V_I$ falling | 4.7 | 5.2 | 5.7 | V |
| | Undervoltage lockout threshold | $V_I$ rising | 4.9 | 5.45 | 5.9 | V |
| | Thermal shutdown | | | 155 | | °C |
| | Thermal shutdown hysteresis | | | 5 | | °C |
| **REFERENCE VOLTAGE REF** | | | | | | |
| $V_{ref}$ | Reference voltage | $V_I$ = 6 V to 14 V, $I_{ref}$ = 10 µA | 1.205 | 1.213 | 1.219 | V |
| **LOGIC SIGNALS CTRL, HVS** | | | | | | |
| $V_{IH}$ | High level input voltage | 6 V ≤ VIN ≤ 14 V | 1.4 | | | V |
| $V_{IL}$ | Low level input voltage | 6 V ≤ VIN ≤ 14 V | | | 0.4 | V |
| $I_{lkg}$ | Input leakage current | EN = CTRL = HVS = GND or 6 V | | 0.01 | 0.1 | µA |
| **SEQUENCING GDLY/EN** | | | | | | |
| | EN/GDLY Charge current | $V_{(threshold)}$ = 1.213 V | 3.6 | 4.8 | 6.2 | µA |
| | EN/GDLY threshold | | | 1.23 | | V |
| | EN/GDLY pulldown resistor | | | 4.5 | | kΩ |
| **SWITCHING FREQUENCY** | | | | | | |
| $f_s$ | Switching frequency | | 600 | 750 | 900 | kHz |
| **REGULATOR REGOUT** | | | | | | |
| $V_O$ | Regulator output voltage | Ireg = 1 mA | 4.6 | 4.8 | 5 | V |
| **BOOST CONVERTER (Vs)** | | | | | | |
| $V_O$ | Output voltage range | | | | 19 | V |
| $V_{FB}$ | Feedback regulation voltage | | 1.136 | 1.146 | 1.154 | V |
| $I_{FB}$ | Feedback input bias current | | | 10 | 100 | nA |
| $R_{DS(on)}$ | N-MOSFET on-resistance (Q1) | $I_{(SW)}$ = 500 mA | | 160 | 270 | mΩ |
| | P-MOSFET on-resistance (Q2) | $I_{(SW)}$ = 200 mA | | 14 | 20 | Ω |
| $I_{MAX}$ | Maximum P-MOSFET peak switch current | | | | 1 | A |
| $I_{LIM}$ | N-MOSFET switch current limit (Q1) | | 3.5 | 4.2 | 4.9 | A |
| $I_{lkg}$ | Switch leakage current | $V_{(SW)}$ = 15 V | | 1 | 10 | µA |
| | Line Regulation | 6 V ≤ Vin ≤ 14 V, $I_O$ = 2 mA | | 0.006 | | %/V |
| | Load Regulation | 2 mA ≤ Iout ≤ 1.8 A | | 0.06 | | %/A |
| **BOOST CONVERTER (Vs) OVERVOLTAGE PROTECTION** | | | | | | |
| | Switch overvoltage protection | Vs rising | 19.5 | 20.2 | 21 | V |
| | Switch overvoltage protection hysteresis | | | 0.6 | | V |
| **GATE DRIVE (GD) AND BOOST CONVERTER PROTECTION** | | | | | | |
| $I_{(GD)}$ | Gate drive sink current | EN = high | | 9 | | µA |
| $R_{(GD)}$ | Gate drive internal pull up resistance | | | 5 | | kΩ |
| $t_{on}$ | Gate on time during short-circuit | Vs < 4.8 V | | 1 | | ms |
| $t_{off}$ | Gate off time during short-circuit | Vs < 4.8 V | | 60 | | ms |
| **TEMPERATURE SENSOR (TEMP)** | | | | | | |
| $V_O$ | Output voltage range | | 1.2 | | 2.5 | V |
| | Drive current | | | | 200 | µA |
| $V_O$ | Output voltage at $T_A$ = 85°C | $T_A$ = 85°C, I = 200 µA, device not switching, FB = FBnominal + 5% | | 2.037 | | V |
| | Temperature accuracy | | –6 | | 6 | °C |
| | Temperature coefficient | | | 5.7 | | mV/°C |

## ELECTRICAL CHARACTERISTICS (continued)

AVIN=VINB=SUPN=12V, EN=REGOUT, Vs = 15V, Vlogic = 3.3V , Vaux = 1.8V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

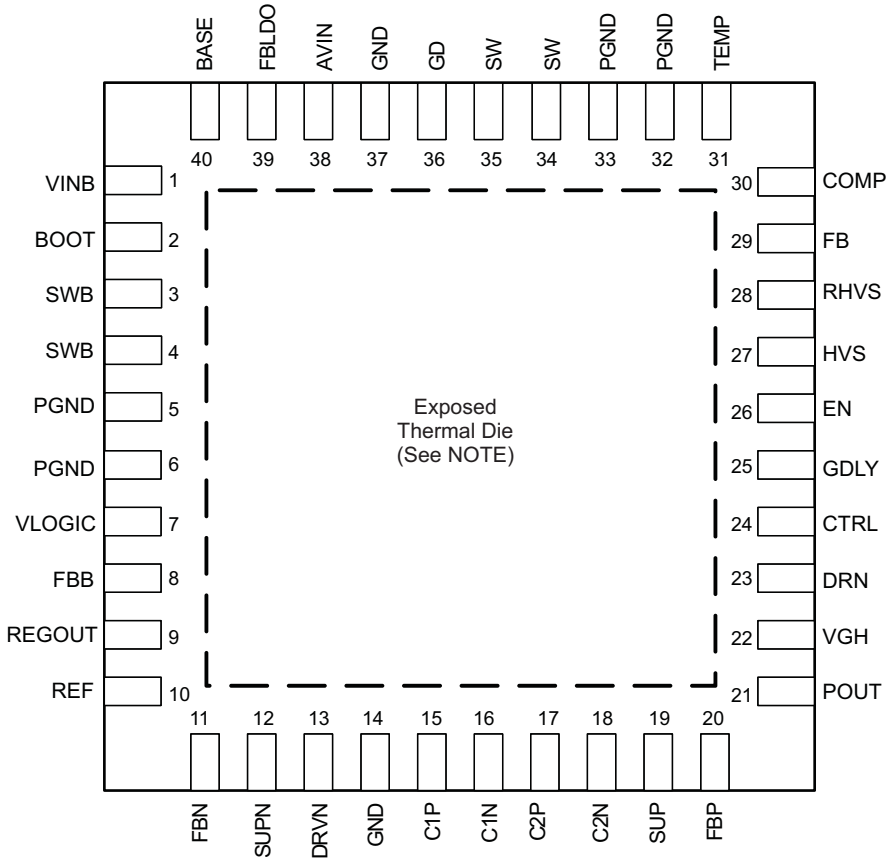
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STEP-DOWN CONVERTER (Vlogic)** | | | | | | |
| $V_O$ | Output voltage range | | 1.5 | | 5 | V |
| | 3.3V fixed output voltage accuracy | FBB = GND | –2% | 3.3 | 2% | V |
| $V_{FB}$ | Feedback regulation voltage | FBB connected to resistor divider, | –2% | 1.213 | 2% | V |
| $I_{FB}$ | Feedback input bias current | | | 10 | 100 | nA |
| $R_{DS(on)}$ | N-MOSFET on-resistance (Q1) | $I_{(SW)}$ = 500 mA | | 200 | 330 | mΩ |
| $I_{LIM}$ | N-MOSFET switch current limit (Q1) | | 2.8 | 3.5 | 4.2 | A |
| $I_{lkg}$ | Switch leakage current | $V_{(SW)}$ = 0 V | | 1 | 10 | µA |
| | Line regulation | 6 V ≤ Vin ≤ 14 V, $I_O$ = 1.8 mA | | 0.006 | | %/V |
| | Load regulation | 1.8 mA ≤ $I_O$ ≤ 2.5 A | | 0.06 | | %/A |
| **STEP-DOWN CONVERTER FEEDBACK SELECT THRESHOLD FBB** | | | | | | |
| $V_{FB}$ | Feedback select threshold | Adjustable version select | | | 0.25 | V |
| **NEGATIVE CHARGE PUMP VGL** | | | | | | |
| $V_I$ | Input supply range | | 6 | | 14 | V |
| $V_O$ | Output voltage range | | | | –2 | V |
| $V_{FB}$ | Feedback regulation voltage | | –36 | 0 | 36 | mV |
| $I_{FB}$ | Feedback input bias current | | | 10 | 100 | nA |
| $R_{DS(on)}$ | Q4 P-Channel switch $R_{DS(on)}$ | $I_O$ = 20 mA | | 4.4 | 8 | Ω |
| | Current source voltage drop[1] | $I_{(DRVN)}$ = 50 mA, $V_{(FBN)}$ = $V_{(FBNnominal)}$ –5% | | 120 | | mV |
| | | $I_{(DRVN)}$ = 100 mA, $V_{(FBN)}$ = $V_{(FBNnominal)}$ –5% | | 235 | | |
| | Line regulation | 9.5 V ≤ Vin ≤ 14 V, $I_O$ = 1 mA | | 0.098 | | %/V |
| | Load regulation | 1 mA ≤ $I_O$ ≤ 100 mA, VGL = –5 V | | 0.055 | | %/mA |
| **POSITIVE CHARGE PUMP (POUT)** | | | | | | |
| $V_O$ | Output voltage range | | | | 30 | V |
| $V_{FB}$ | Feedback regulation voltage | CTRL = GND, VGH = open | 1.187 | 1.214 | 1.238 | V |
| $I_{FB}$ | Feedback input bias current | | | 10 | 100 | nA |
| | Effective output resistance | Doubler Mode (x2); $I_{(POUT)}$ = 20 mA | | 98 | | Ω |
| | | Doubler Mode (x2); $I_{(POUT)}$ = 50 mA | | 63 | | |
| | | Tripler Mode (x3); $I_{(POUT)}$ = 20 mA | | 143 | | |
| | | Tripler Mode (x3); $I_{(POUT)}$ = 50 mA | | 91 | | |
| | Load regulation | 1 mA ≤ Iout ≤ 51 mA, VGH = 23.9 V | | 0.0022 | | %/mA |
| **HIGH VOLTAGE SWITCH VGH** | | | | | | |
| $R_{DS(on)}$ | POUT to VGH $R_{DS(on)}$ | CTRL = high, POUT = 27 V, I = 20 mA | | 10 | 18 | Ω |
| | DRN to VGH $R_{DS(on)}$ | CTRL = low, $V_{(DRN)}$ = 5 V, I = 20 mA | | 40 | 60 | |
| $I_{(DRN)}$ | DRN input current | CTRL = low, $V_{(DRN)}$ = 10 V | | 10 | | µA |
| $t_{dly}$ | CTRL to VGH propagation delay | CTRL = high to low, POUT = 27 V, $V_{(DRN)}$ = GND | | 120 | | ns |
| | | CTRL= low to high, POUT = 27 V, $V_{(DRN)}$ = GND | | 140 | | |
| $R_{(VGH)}$ | VGH pull down resistance | EN = low, I = 20 mA | | 1 | | kΩ |
| **LINEAR REGULATOR CONTROLLER Vaux** | | | | | | |
| $V_{EB}$ | Emitter voltage range | | 2.3 | | 15 | V |
| $V_{FB}$ | Feedback regulation voltage | | –2% | 1.213 | 2% | |
| $I_{(BASE)}$ | Base sink current | $V_{(BASE)}$ = 3.3 V-1V, VFBLDO = 1.15 V | 25 | | | mA |
| | | $V_{(BASE)}$ = 2.5 V-1V, VFBLDO = 1.15 V | 15 | | | |
| | Power supply rejection ratio | LDO input | | 65 | | dB |
| | Line regulation | 6V ≤ Vin ≤ 14 V, $I_{(load)}$ = 1 mA, Vaux = 1.6 V | | 0.007 | | %/V |
| | Load regulation | 1 mA ≤ $I_O$ ≤ 500 mA, $V_I$ = 3.3 V, Vaux = 1.6 V | | 0.48 | | %/A |
| **HIGH VOLTAGE STRESS TEST (HVS), RHVS** | | | | | | |

(1) The maximum charge pump output current is half the drive current of the internal current source or sink

## ELECTRICAL CHARACTERISTICS (continued)

AVIN=VINB=SUPN=12V, EN=REGOUT, Vs = 15V, Vlogic = 3.3V , Vaux = 1.8V, $T_A$ = –40°C to 85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(POUT)}$ | Positive charge pump output voltage | TPS65167, HVS = high | 29 | 30 | 31 | V |
| | RHVS pull down resistance | TPS65167A, TPS65167, HVS = high, $I_{(HVS)}$ = 100 µA | 450 | 650 | 850 | Ω |
| $I_{lkg}$ | RHVS leakage current | TPS65167A, TPS65167, HVS = low, $V_{(RHVS)}$ = 5 V | | | 100 | nA |




NOTE: The thermally enhance PowerPAD is connected to GND.

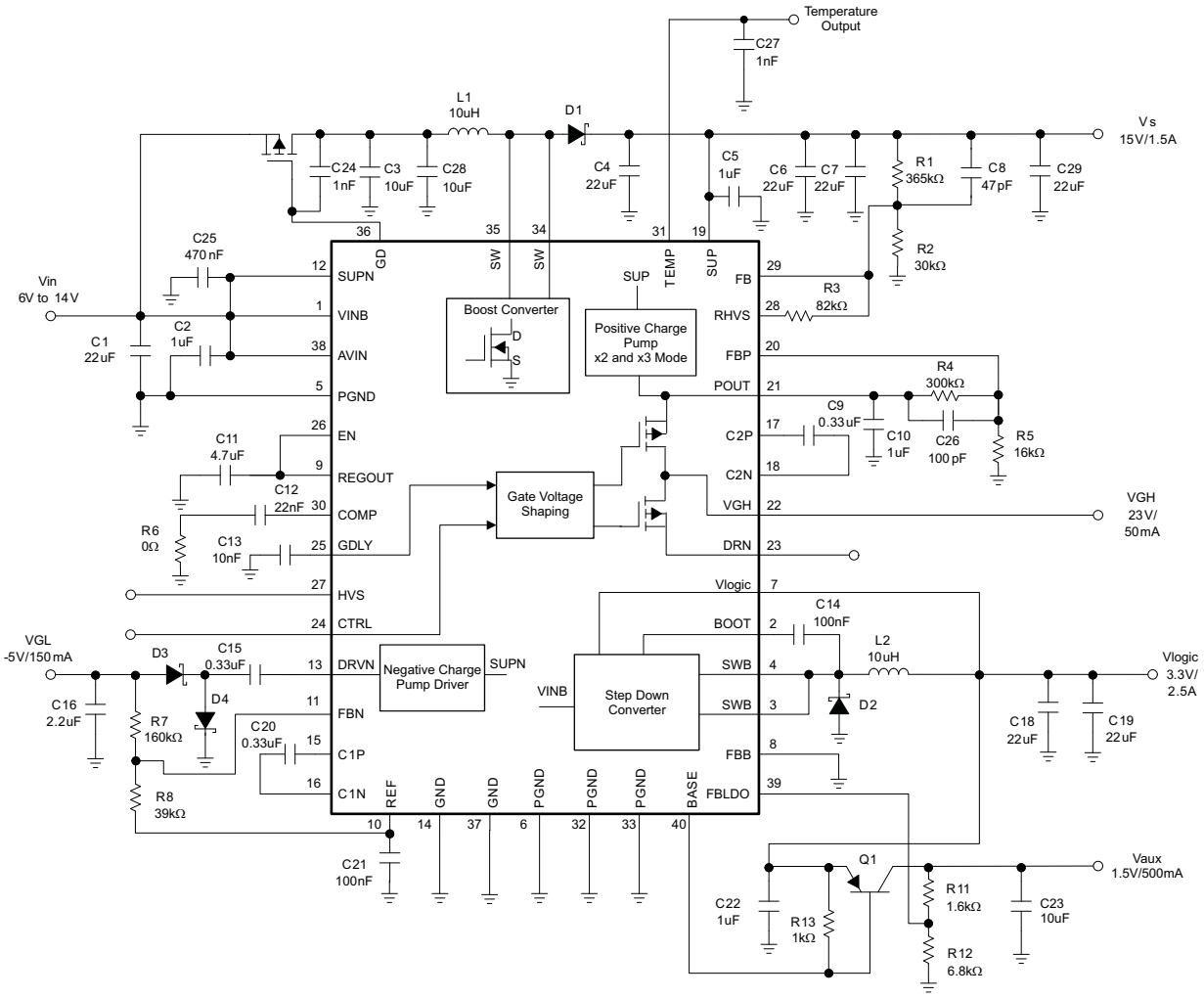
### TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VINB | 1 | I | Power input for the buck converter. |
| BOOT | 2 | I | This pin generates the gate drive voltage for the Buck converter. Connect a 100 nF from this pin to the switch pin of the step-down converter SWB. |
| SWB | 3, 4 | O | Switch pin of the step-down converter |
| PGND | 5 | | Power ground for the step-down converter |
| PGND | 6 | | Power ground for the negative charge pump |
| VLOGIC | 7 | I | Output sense of the step-down converter |
| FBB | 8 | I | Feedback pin of the step-down converter |
| REGOUT | 9 | O | Output of the internal 5V regulator. Connect a 4.7 µF bypass capacitor to this pin. |
| REF | 10 | O | Internal reference output typically 1.213 V. Connect a 100 nF bypass capacitor to this pin. |
| FBN | 11 | I | Feedback pin of negative charge pump |
| SUPN | 12 | I | Power supply pin for the negative charge pump driver. |

## TERMINAL FUNCTIONS (continued)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DRVN | 13 | I/O | Drive pin of the negative charge pump. |
| GND | 14 | | Power ground for the positive charge pump |
| C1P | 15 | | Positive charge pump flying capacitor |
| C1N | 16 | | Positive charge pump flying capacitor |
| C2P | 17 | | Positive charge pump flying capacitor |
| C2N | 18 | | Positive charge pump flying capacitor |
| SUP | 19 | I/O | Power supply pin of the positive charge pump and control voltage for the boost regulator Vs. Connect this pin with a short and wide PCB trace to the output of the boots converter |
| FBP | 20 | | Feedback of the positive charge pump |
| POUT | 21 | | Output of the positive charge pump converter |
| VGH | 22 | | Output of the high voltage switch and gate shaping function block |
| DRN | 23 | | Termination of the low side switch of the gate voltage shaping block |
| CTRL | 24 | I | Control input for the gate voltage shaping block. Connect this pin to REGOUT if the gate voltage shaping function is not used. |
| GDLY | 25 | O | Connecting a capacitor from this pin to GND allows to set the delay time between the boost converter Vs and VGH. Note that VGH is controlled by CTRL as well. |
| EN | 26 | I | This is the enable pin of the boost converter Vs, negative charge pump VGL and positive charge pump POUT. This pin is a dual function pin. EN can be held high if no start-up delay is desired or a capacitor can be connected to this pin. The capacitor determines the start-up delay time. |
| HVS | 27 | I | Logic control input to force the device into High Voltage Stress Test. With HVS = low the high voltage stress test disabled. With the TPS65167 and HVS = high the high voltage stress test is enabled for Vs and for VGH. With the TPS65167A and HVS = high the high voltage stress test is enabled for Vs only. |
| RHVS | 28 | I/O | This resistor sets the voltage of the boost converter Vs when the High Voltage Stress test is enabled. (HVS = high). With HVS = high the RHVS pin is pulled to GND which sets the voltage for the boost converter during High Voltage Stress. When HVS is disabled (HVS = low) the RHVS pin is high impedance. |
| FB | 29 | I | Feedback of the boost converter Vs |
| COMP | 30 | I/O | Compensation for the regulation loop of the boost converter generating Vs. Typically a 22 nF compensation capacitor is connected to this pin. |
| TEMP | 31 | O | This is the output of the internal device temperature sensor. The output voltage is proportional to the chip temperature. |
| PGND | 32, 33 | | Power Ground for the boost converter Vs |
| SW | 34, 35 | I/O | Switch pin of the boost converter generating Vs |
| GD | 36 | I/O | Gate drive. This pin controls the external isolation MOSFET. |
| GND | 37 | | Analog Ground for the internal reference |
| AVIN | 38 | I | Analog input voltage of the device. Bypass this pin with a 0.47 µF bypass capacitor. |
| FBLDO | 39 | I | Feedback of the LDO controller |
| BASE | 40 | I/O | BASE drive of the external PNP transistor |
| PowerPAD™ | | | Analog GND for the internal reference |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

### Table 1. Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| **Main Boost Converter (Vs)** | | | |
| η | Efficiency boost converter | vs Load currents | Figure 1 |
| | Softstart boost converter | vs Load currents | Figure 2 |
| | PWM operation | at nominal load current | Figure 3 |
| | PWM operation | at light load current | Figure 4 |
| | Overvoltage protection | | Figure 5 |
| | Short-circuit power down cycling | | Figure 6 |
| | Load transient response boost converter | | Figure 7 |
| **Step-Down Converter (Vlogic)** | | | |
| η | Efficiency buck converter | vs Load currents | Figure 8 |
| | PWM operation | at nominal load current | Figure 9 |
| | PWM operation | at light load current | Figure 10 |
| | Softstart buck converter | | Figure 11 |
| | Load transient response buck converter | | Figure 12 |
| **LDO Controller** | | | |
| Vaux | Load transient response LDO controller | | Figure 13 |
| **Negative Charge Pump Driver** | | | |
| | VGL | vs Load current - doubler stage | Figure 14 |
| **Positive Charge Pump Driver** | | | |
| | VGH | vs Load current | Figure 15 |
| **Temperature Sensor** | | | |
| | $V_{Temp}$ | vs Temperature | Figure 16 |
| **System Performance** | | | |
| | Gate voltage shaping VGH | | Figure 17 |
| | Power up sequencing | EN connected to REGOUT | Figure 18 |
| | Power up sequencing | External capacitor connected to EN | Figure 19 |
| | Power up sequencing | REGOUT vs VREF | Figure 20 |

EFFICIENCY BOOST CONVERTER (Vs)
vs
LOAD CURRENT

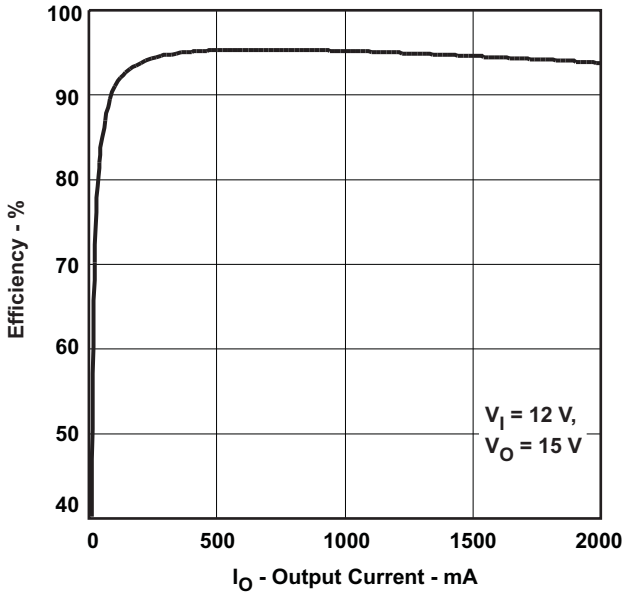



Figure 1.

SOFTSTART BOOST CONVERTER (Vs)
vs
LOAD CURRENT

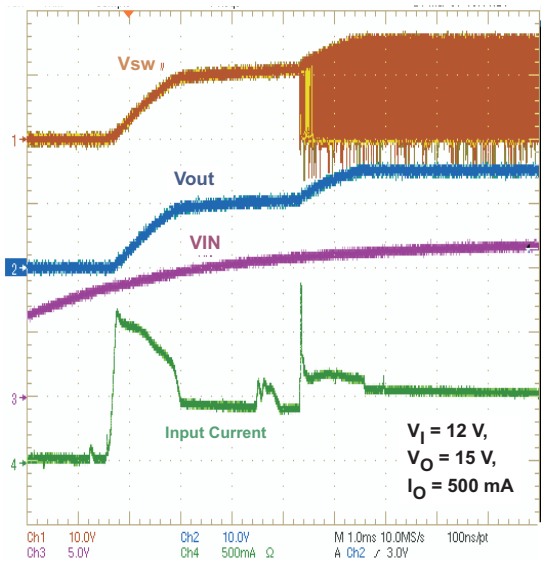



Figure 2.

PWM OPERATION AT NOMINAL LOAD CURRENT

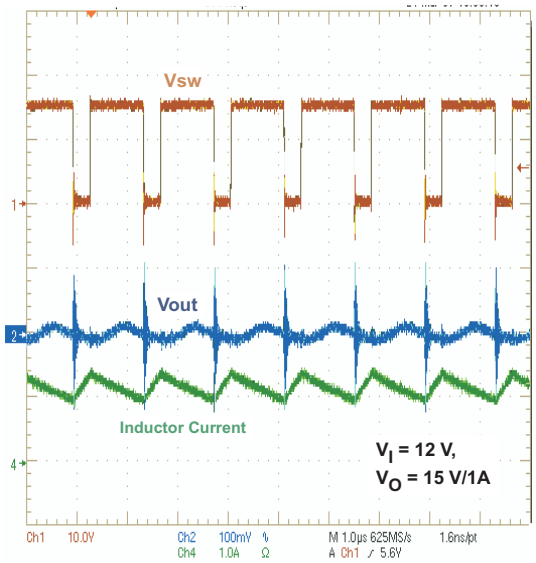



Figure 3.

PWM OPERATION AT LIGHT LOAD CURRENT

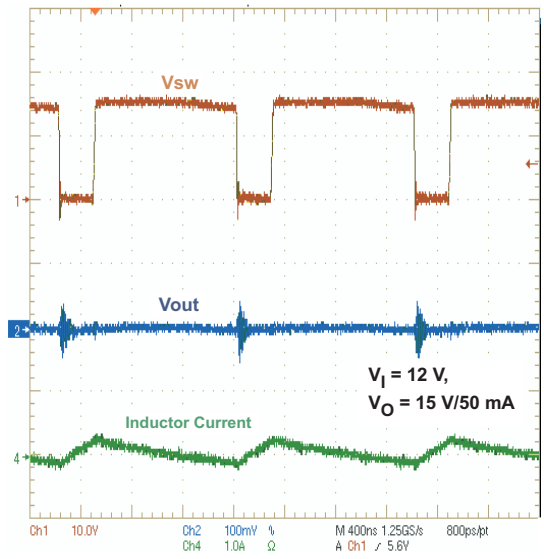



Figure 4.

**OVER VOLTAGE PROTECTION**

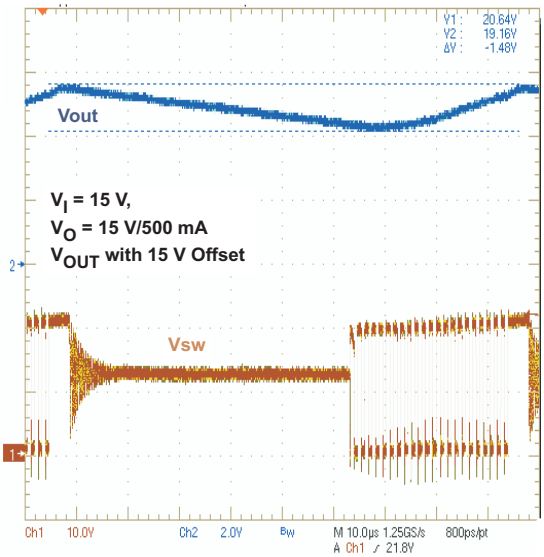



Figure 5.

**SHORT-CIRCUIT POWER DOWN CYCLING**

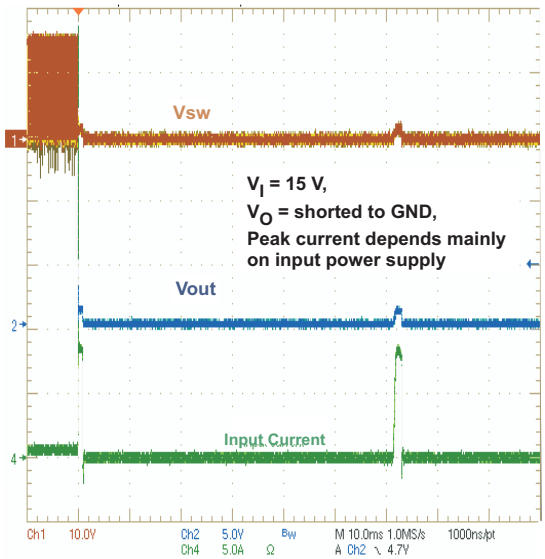



Figure 6.

**LOAD TRANSIENT RESPONSE BOOST CONVERTER**

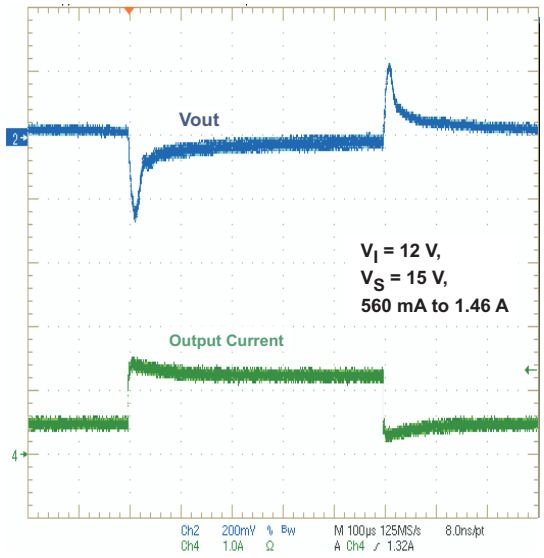



Figure 7.

**EFFICIENCY BUCK CONVERTER vs LOAD CURRENT**

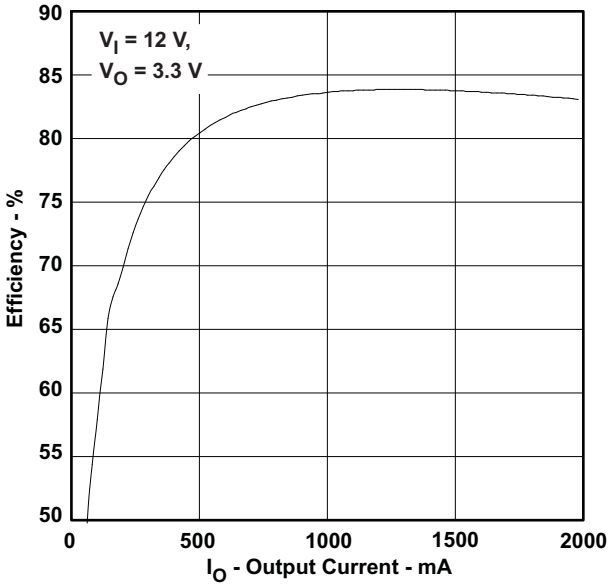



Figure 8.

**PWM OPERATION AT NOMINAL LOAD CURRENT**

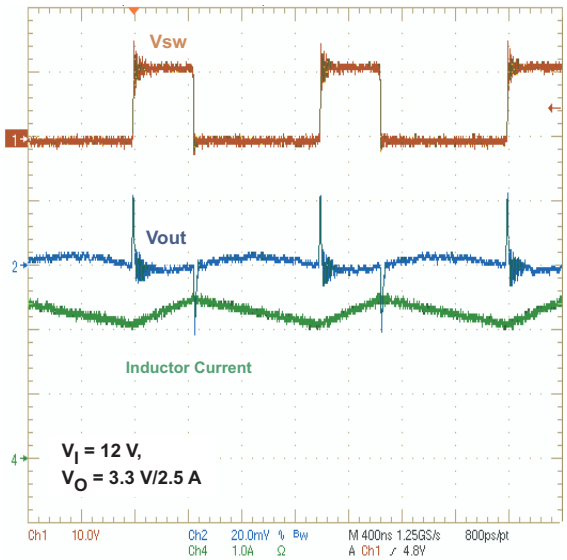



Figure 9.

**PWM OPERATION AT LIGHT LOAD CURRENT**

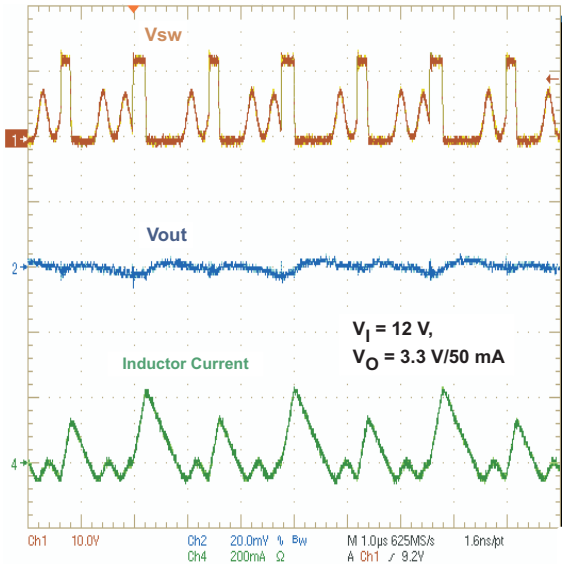



Figure 10.

**SOFTSTART BUCK CONVERTER Vlogic**

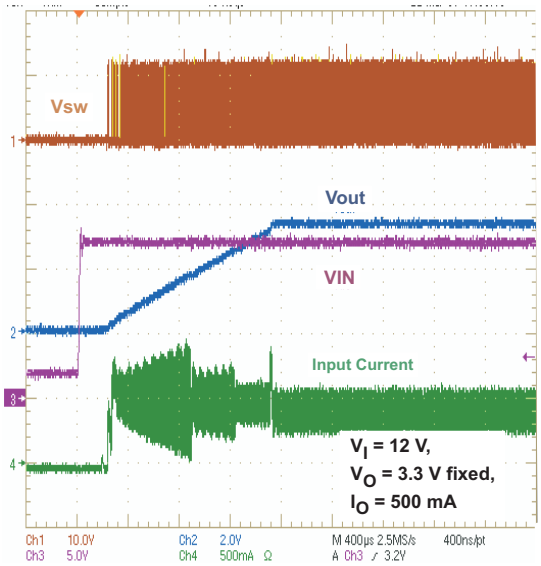



Figure 11.

**LOAD TRANSIENT RESPONSE BUCK CONVERTER**

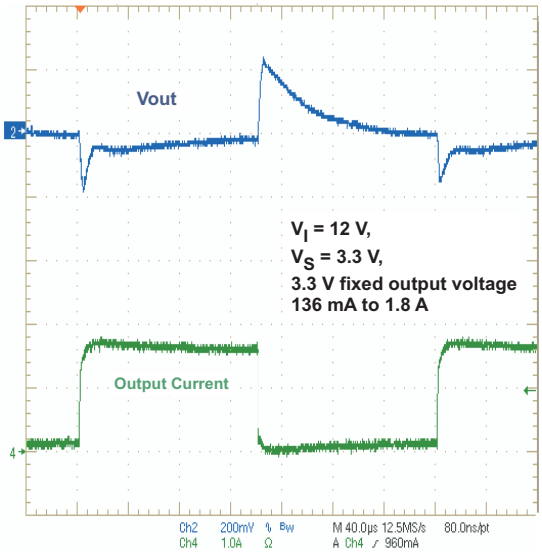



Figure 12.

LOAD TRANSIENT RESPONSE LDO CONTROLLER

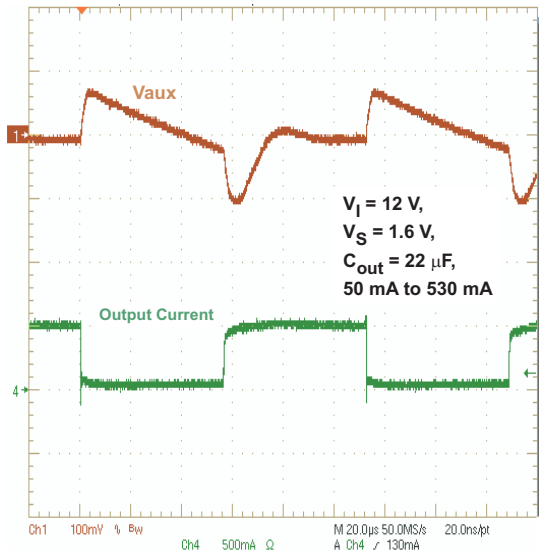



Figure 13.

VGL vs LOAD CURRENT

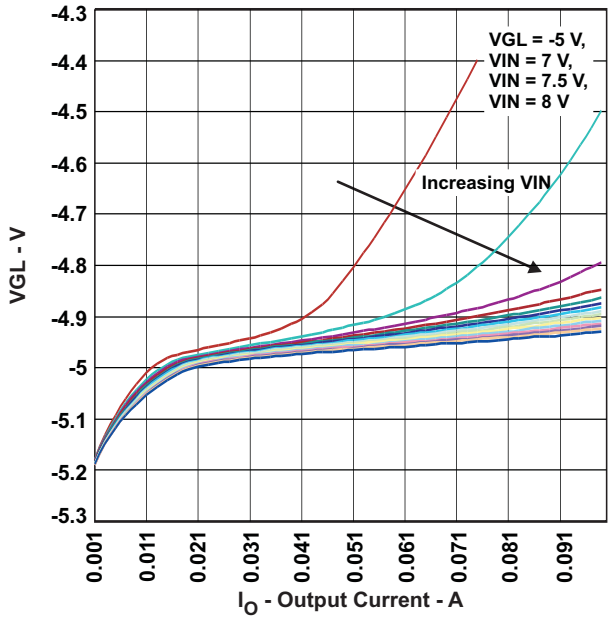



Figure 14.

VGH vs LOAD CURRENT – DOUBLER STAGE

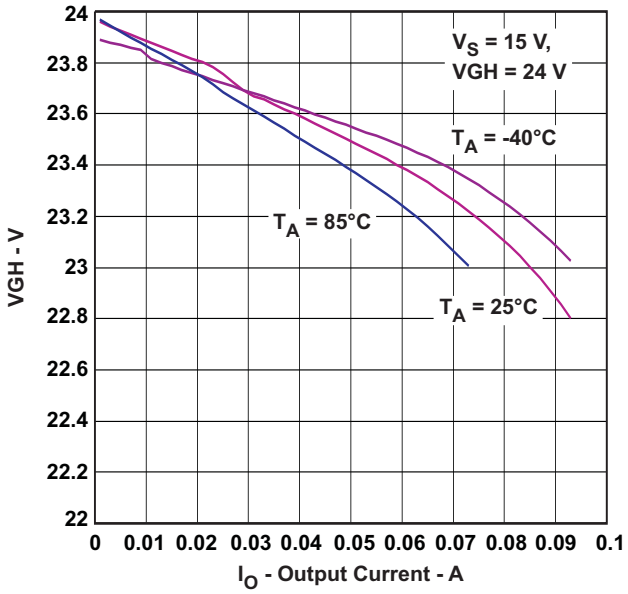



Figure 15.

$V_{temp}$ vs TEMPERATURE

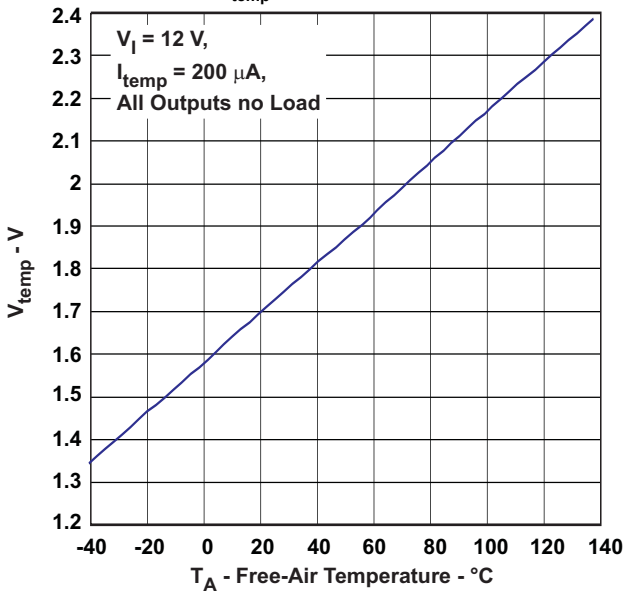
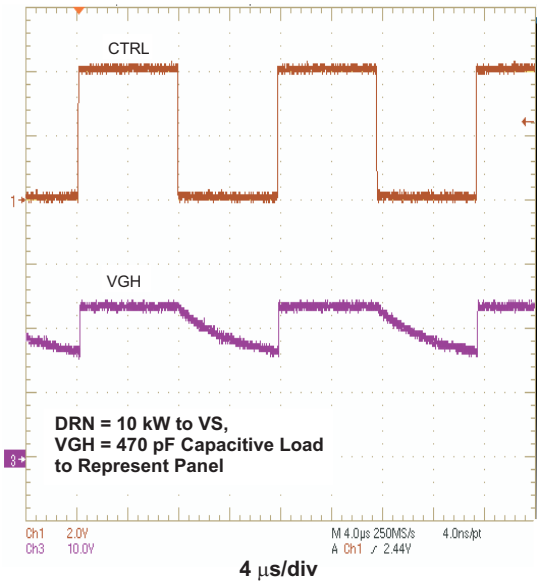



Figure 16.

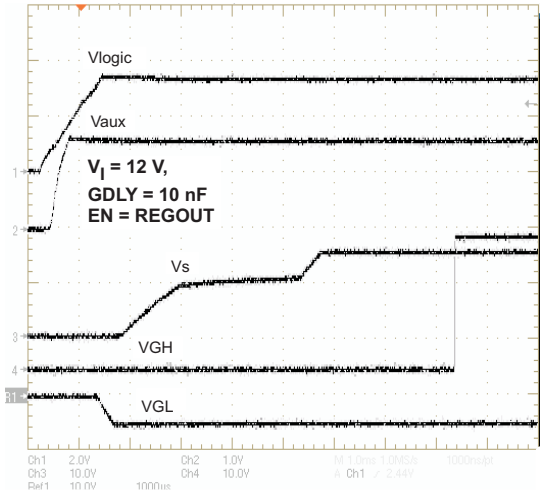
**GATE VOLTAGE SHAPING VGH**




**4 µs/div**

**Figure 17.**

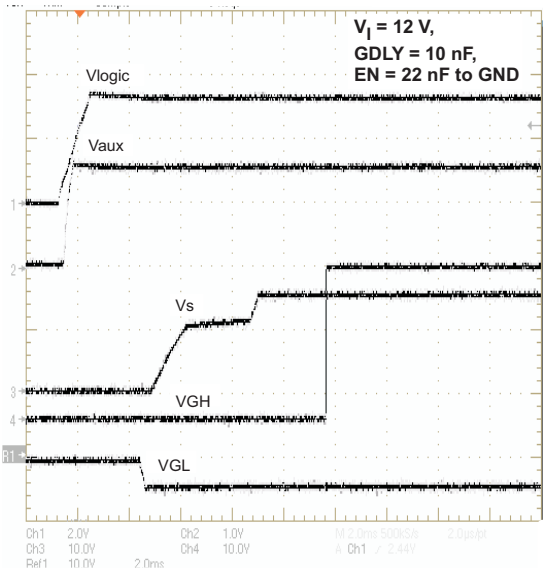
**POWER-UP SEQUENCING**




**1 ms/div**

**Figure 18.**

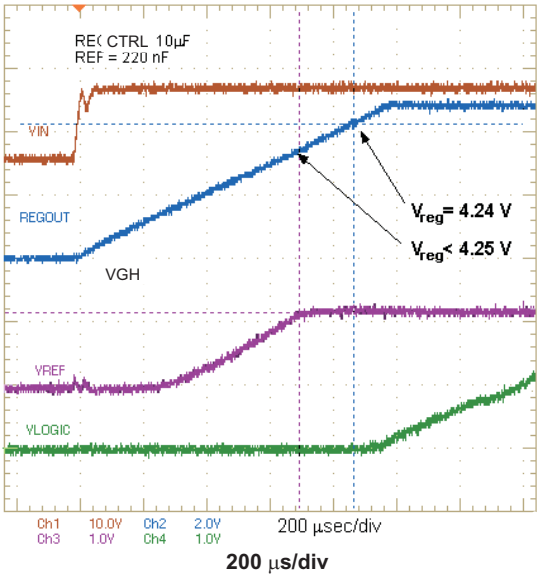
**POWER-UP SEQUENCING**




**2 ms/div**

**Figure 19.**

**POWER-UP SEQUENCING**
**REGOUT vs VREF**




**200 µs/div**

**Figure 20.**

## APPLICATION INFORMATION

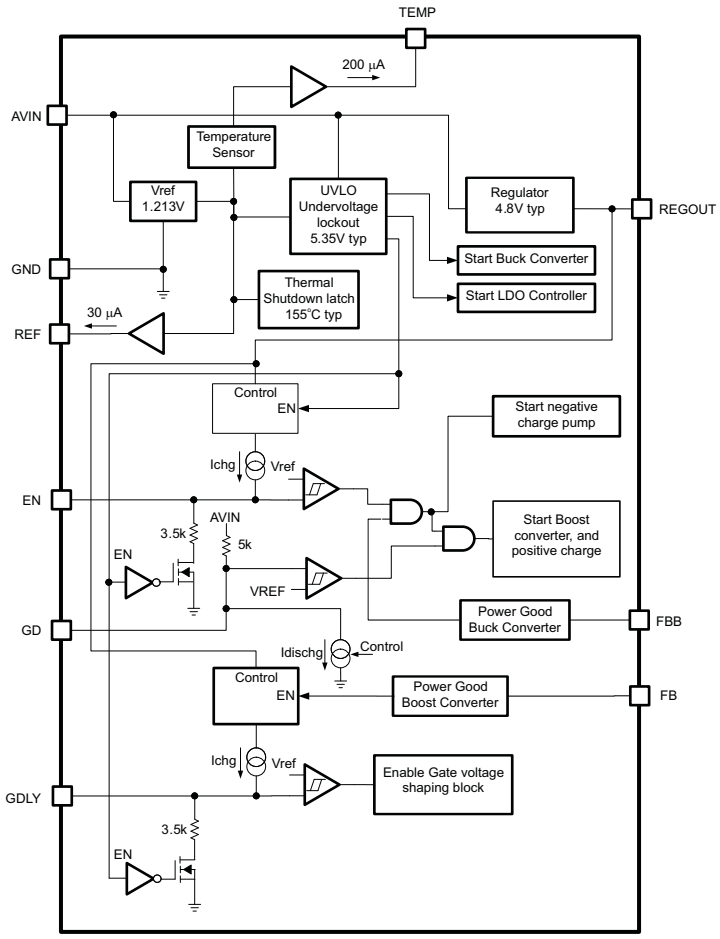



**Figure 21. Control Block TPS65167**

### Regulator REGOUT and Reference REF

The 4.8 V regulator REGOUT and reference REF is always on as long as the input voltage is above the device undervoltage lockout of typically 5.2 V. To ensure a correct start-up, the reference voltage REF needs to come up faster than the regulator voltage REGOUT. In other words as REF = 1.213 V then REGOUT must remain < 4.25 V to assure proper start-up (Figure 22).

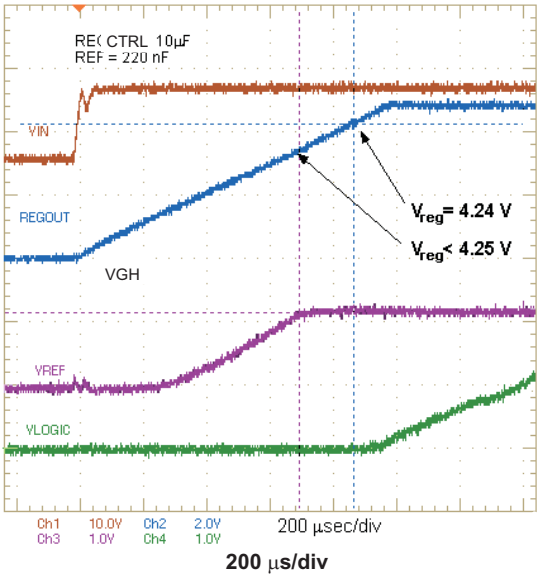



**Figure 22. Power-up Sequencing (REGOUT vs VREF)**

This is implemented by connecting a 4.7 µF bypass capacitor to REGOUT and a 100 nF bypass capacitor to the REF pin. If the bypass capacitor on the REF pin is selected larger than 100 nF, then the bypass capacitor on REGOUT needs to be increased accordingly. Refer to Table 2 to properly select a bypass capacitor.

The REF pin provides a reference output which is used to regulate the negative charge pump. In order to have a stable reference voltage, a 100 nF bypass capacitor is required, which needs to be connected directly from REF to GND (pin 37) for best noise immunity. The reference output has a current capability of 30 µA which must not be exceeded. Therefore, the feedback resistor value from FBN to REF must not be smaller than 40 kΩ.

**Table 2. Bypass Capacitor Selection**

| | REGOUT | Type/Rating | REF | Type |
|---|---|---|---|---|
| Option 1 | 4.7 µF | X7R or X5R/10V | 100 nF | x7R or X5R |
| Option 2 | 10 µF | X7R or X5R/10V | 220 nF or 100 nF | x7R or X5R |

## Temperature Sensor Output TEMP

The device provides a temperature sensor output measuring the actual chip temperature. This pin has an analog output capable of driving 200 µA. The TEMP pin requires a 1 nF output capacitor to provide a stable output voltage. At 85°C, the typical output voltage is 2.037 V with a temperature coefficient of 5.9 mV/°C. See Figure 16 for the output characteristic of the temperature output.

## Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive die temperatures. Once the thermal shutdown is exceeded, the device enters shutdown. The device can be enabled again by cycling the EN pin or input voltage to ground.

## Undervoltage Lockout

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included which shuts down the device at voltages lower than 5.2 V.

## Short circuit protection (all outputs)

All the outputs have a short circuit protection implemented.

Boost converter Vs: A short circuit is detected when the voltage on SUP, that is connected to the output falls typically below 4.5V. Then the isolation switch is opened by pulling GD high. After a delay of typically 60mS the isolation switch is closed again and restarts the output automatically. See Figure 6.

Buck converter Vlogic: During a short circuit even the output current is typically limited to the buck converter switch current limit of 3.5A and the switching frequency is reduced.

Negative charge pump VGL: As the output falls below the power good limit threshold the output current is limited to the softstart current limit of the negative charge pump.

Positive charge pump output VGH: As the output POUT falls below its power good threshold then the internal gate voltage shaping switch opens disconnecting the load from POUT. As the output POUT exceeds the power good threshold again the internal switch of the gate voltage shaping block is closed again. The VGH output cycles as long as the short circuit event remains.

LDO controller VAUX: During a short circuit event the maximum output current is given by the gain of the external transistor. Depending on the selected output transistor the power dissipation of the external transistor might be exceeded during a short circuit event. Using a base series resistor protects the IC during a short circuit event.

## Start-Up Sequencing

The device has an adjustable start-up sequencing to provide correct sequencing as required by LCD. When the input voltage exceeds the undervoltage lockout threshold, then the step-down converter and LDO controller start-up at the same time. As the enable signal (EN) goes high, the negative charge pump starts up followed by the boost converter Vs starting at the same time as the positive charge pump. See the typical curves shown in Figure 18, Figure 19, and Figure 23.

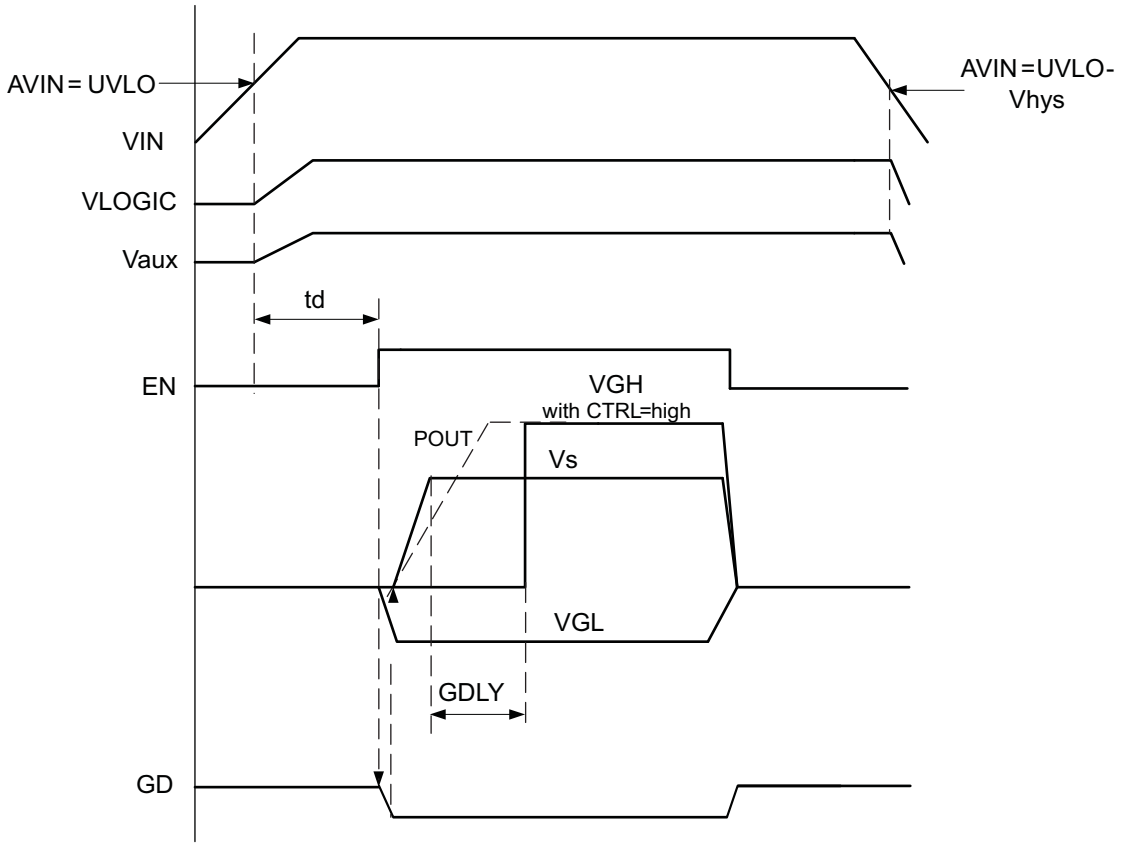



**Figure 23. Power Up Sequencing**

## Enable EN

The enable is a dual function pin. It can be used as a standard enable pin that enables the device once it is pulled high by a logic signal or connected to the REGOUT pin.

**The enable can not be connected directly to Vin due to its maximum voltage rating!**

If no logic control signal is available, it is also possible to connect a capacitor to this pin to set the delay time $t_d$ as shown in Figure 23 and Figure 19.

## Delay GDLY

The capacitor connected to GDLY sets the delay time from the point when the boost converter Vs reaches its nominal value to the enable of the gate voltage shaping block.

## Setting the Delay Times GDLY, EN delay

Connecting an external capacitor to the GDLY and EN pin sets the delay time. To set the delay time, the external capacitor is charged with a constant current source of typically 5 µA. The delay time is terminated when the capacitor voltage has reached the threshold voltage of Vth = 1.230 V. The external delay capacitor is calculated:

$$C_{dly} = \frac{5\ \mu A \times td}{Vref} = \frac{5\ \mu A \times td}{1.23\ V} \quad (1)$$

with $t_d$ = Desired delay time

Example for setting a delay time of 2.3 mS

$$C_{dly} = \frac{5\ \mu A \times 2.3\ ms}{1.23\ V} = 9.3\ nF \Rightarrow C_{dly} = 10\ nF \quad (2)$$

## Boost Converter

The main boost converter operates in Pulse Width Modulation (PWM) and at a fixed switching frequency of 750 kHz The converter uses a unique fast response, voltage-mode controller scheme with feed-forward input voltage . This achieves excellent line and load regulation (0.2% A load regulation typical) and allows the use of small external components. To add higher flexibility to the selection of external component values the device uses external loop compensation. Although the boost converter looks like a non-synchronous boost converter topology operating in discontinuous conduction mode at light load, the device will maintain continuous conduction even at light load currents. This is achieved with a novel architecture using an external Schottky diode with an integrated MOSFET in parallel connected between SW and SUP. See the Functional Block Diagram. The intention of this MOSFET is to allow the current to go below ground that occurs at light load conditions. For this purpose, a small integrated P-Channel MOSFET with typically 10 Ω $R_{DS(on)}$ is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage will carry the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with standard non-synchronous boost converter, and allows a simpler compensation for the boost converter.

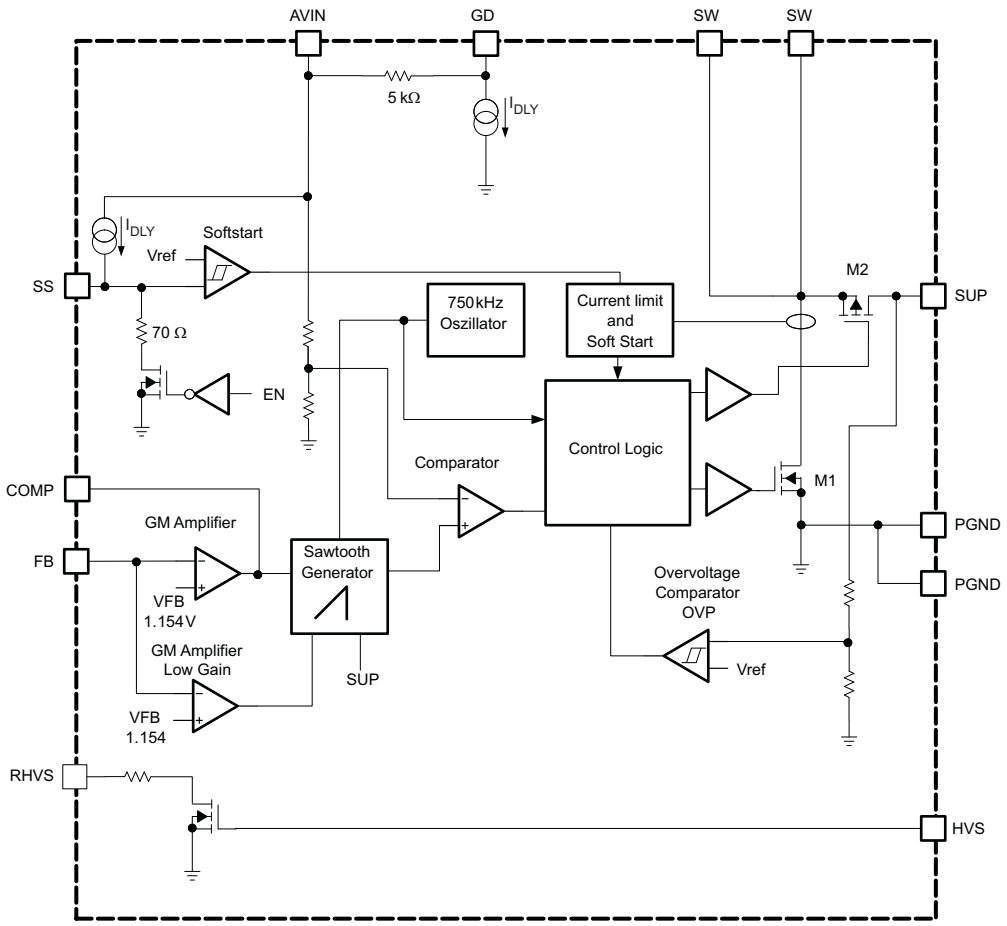



**Figure 24. Block Diagram Boost Converter**

## Softstart (Boost Converter)

The main boost converter has an internal softstart to prevent high inrush current during start-up. The device incorporates a digital softstart increasing the current limit in digital current limit steps. See Figure 2 for the typical softstart timing.

## High Voltage Stress Test (Boost converter and positive charge pump)

The TPS65167 and TPS65167A incorporates a high voltage stress test where the output voltage of the boost converter Vs and the positive charge pump POUT is set to a higher voltage compared to the nominal programmed output voltage. The High Voltage Stress test is enabled by pulling the HVS pin to high. With HVS = high, the voltage on POUT, respectively VGH, remains unchanged with the TPS65167A and the TPS65167 regulates to a fixed output voltage of 30 V. The boost converter Vs is programmed to a higher voltage determined by the resistor connected to RHVS. With HVS = high the RHVS pin is pulled to GND which sets the voltage for the boost converter during the High Voltage Stress Test. The output voltage for the boost converter during high voltage stress test is calculated as:

$$Vs_{HVS} = V_{FB} \frac{R1 + R2//R3}{R2//R3} = 1.146V \frac{R1 + R2//R3}{R2//R3}$$

$$R3 = \frac{R1 \times R2}{\left(\frac{Vs_{HSV}}{V_{FB}} - 1\right) \times R2 - R1} \quad (3)$$

With:

$Vs_{HVS}$ = Boost converter output voltage with HVS = high

$V_{FB}$ = 1.146 V

## Overvoltage Protection

The main boost converter has an overvoltage protection of the main switch M1 if the feedback pin (FB) is floating or shorted to GND causing the output voltage to rise. In such an event, the output voltage is monitored with the overvoltage protection comparator on the SUP pin. As soon as the comparator trips at typically at 20 V then the boost converter stops switching. The output voltage will fall below the overvoltage threshold and the converter continues to operate. See Figure 4.

Note: During high voltage stress test the overvoltage protection is disabled.

## Input Capacitor Selection VINB, SUP, SUPN, AVIN, Inductor Input Terminal

For good input voltage filtering, low ESR ceramic capacitors are recommended. The TPS65167 has an analog input AVIN as well as a power supply input SUP powering all the internal rails. A 1-µF bypass capacitor is required as close as possible from AVIN to GND as well as from SUP to GND. The SUPN pin needs to be bypassed with a 470-nF capacitor. Depending on the overall load current two or three 22-µF input capacitors are required. For better input voltage filtering, the input capacitor values can be increased. To reduce the power losses across the external isolation switch a filter capacitance at the input terminal of the inductor is required. To minimize possible audible noise problems, two 10-µF capacitors in parallel are recommended. More capacitance will further reduce the ripple current across the isolation switch. See Table 3 and the typical applications for input capacitor recommendations.

**Table 3. Input Capacitor Selection**

| CAPACITOR | COMPONENT SUPPLIER | COMMENTS |
|---|---|---|
| 22 µF/16 V | Taiyo Yuden EMK316BJ226ML | Pin VINB |
| 2 ×10 µF/25 V | Taiyo Yuden TMK316BJ106KL | Pin VINB (alternative) |
| 2 ×10 µF/25 V | Taiyo Yuden TMK316BJ106KL | Inductor input terminal |
| 1 µF/35 V | Taiyo Yuden GMK107BJ105KA | Pin SUP |
| 1 µF/25 V | Taiyo Yuden TMK107BJ105KA | Pin AVIN |
| 470 nF/25 V | Taiyo Yuden TMK107BJ474MA | Pin SUPN |

## Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate the converter efficiency by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. With the efficiency number it is possible to calculate the steady state values of the application.

1. Converter Duty Cycle: $$D = 1 - \frac{Vin \times \eta}{Vout}$$
2. Maximum output current: $$Iout = \left( Isw - \frac{Vin \times D}{2 \times fs \times L} \right) \times (1 - D)$$
3. Peak switch current: $$I_{swpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D}$$

With Isw = converter switch current (minimum switch current limit = 3.5 A)

fs = converter switching frequency (typical 750 kHz)

L = Selected inductor value

$\eta$ = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an estimation)

The peak switch current is the steady state peak switch current the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest. Note that the maximum output power of the device is limited by the power dissipation of the package.

### Inductor Selection (Boost Converter)

The TPS65167 typically operates with a 10-µH inductor. Main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated above with additional margin to cover for heavy load transients. The alternative more conservative approach is to choose the inductor with saturation current at least as high as the minimum switch current limit of 3.5 A. The second important parameter is the inductor dc resistance. The lower the dc resistance the higher the efficiency of the converter. The converter efficiency can vary between 2% to 10% when choosing different inductors. Possible inductors are shown in Table 4.

**Table 4. Inductor Selection Boost Converter**

| INDUCTOR VALUE | COMPONENT SUPPLIER | DIMENSIONS in mm | Isat/DCR |
|---|---|---|---|
| 10 µH | Sumida CDRH8D43-100 | 8.3 × 8.3 × 4.5 | 4 A/29 mΩ |
| 10 µH | Wuerth 744066100 | 10 × 10 × 3.8 | 4 A/25 mΩ |
| 10 µH | Coilcraft DO3316P-103 | 12.95 × 9.4 × 5.5 | 3.9 A/38 mΩ |

### Output Capacitor Selection (Boost Converter)

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value and work best with the TPS65167. Three 22-µF or six 10-µF ceramic output capacitors in parallel are sufficient for most applications. More capacitors can be added to improve the load transient regulation. See Table 5 for the selection of the output capacitor.

**Table 5. Output Capacitor Selection**

| CAPACITOR | COMPONENT SUPPLIER | COMMENTS |
|---|---|---|
| 6 × 10 µF/25 V | Taiyo Yuden TMK316BJ106KL | |
| 3 × 22 µF/25 V | TDK C4532X7R1E226M | Alternative solution |

### Rectifier Diode Selection (Boost Converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the converter. The current rating for the Schottky diode is calculated as the off time of the converter times the peak switch current of the application. The minimum switch current of the converter can be used as a worst case calculation.

$$I_{avg} = (1 - D) \times Isw = \frac{Vin}{Vout} \times 3.5\ A$$ with Isw=minimum switch current of the TPS65167 (3.5 A)

Usually a Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most of the applications. Secondly, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$$P_D = I_{avg} \times V_F = Isw \times (1 - D) \times V_F = I_{sw} = \frac{Vin}{Vout} \times V_F$$ with Isw = minimum switch current of 3.5 A (worst case calculation)

**Table 6. Rectifier Diode Selection (Boost Converter)**

| Avg. | Or | $V_{forward}$ | $R_{\theta JA}$ | SIZE | COMPONENT SUPPLIER |
|---|---|---|---|---|---|
| 3 A | 20 V | 0.36 at 3 A | 46°C/W | S.C. | MBRS320, International Rectifier |
| 2 A | 20 V | 0.44 V at 2 A | 75°C/W | SMB | SL22, Vishay Semiconductor |
| 2 A | 20 V | 0.5 at 2 A | 75°C/W | SMB | SS22, Fairchild Semiconductor |

### Setting the Output Voltage and Selecting the Feed-forward Capacitor (Boost Converter)

The output voltage is set by the external resistor divider and is calculated as:

$$V_{out} = 1.146\ V \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

Across the upper resistor a bypass capacitor is required to speed up the circuit during load transients. The capacitor is calculated as:

$$C8 = \frac{1}{2 \times \pi \times f_z \times R1} = \frac{1}{2 \times \pi \times 10000 \times R1} \quad (5)$$

A value coming closest to the calculated value should be used.

## Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. A single capacitor connected to this pin sets the low frequency gain. A 22-nF capacitor is sufficient for most of the applications. Adding a series resistor sets an additional zero and increases the high frequency gain. The formula below calculates at what frequency the resistor will increase the high frequency gain.

$$f_z = \frac{1}{2 \times \pi \times C12 \times R6} \quad (6)$$

Lower input voltages require a higher gain and; therefore, a lower compensation capacitor value. See the typical applications for the appropriate component selection.

## Gate Drive Pin (GD) and Isolation Switch Selection

The external isolation switch disconnects the output of the boost converter once the device is turned off. The external isolation switch also provides a short-circuit protection of Vs by turning off the switch in case of a short-circuit. The Gate Drive (GD) allows control of an external isolation MOSFET switch. GD pin is pulled low when the input voltage is above the undervoltage lockout threshold (UVLO) and when enable (EN) is high. The gate drive has an internal pull up resistor to AVIN of typically 5 kΩ. In order to minimize inrush current during start-up, the gate drive pin is pulled low by an internal 10µA current sink. To further reduce this inrush current, typically a 1-nF capacitor can be connected from pin GD to the boost converter inductor. A standard P-Channel MOSFET with a current rating close to the minimum boost converter switch current limit of 3.5 A is sufficient. Table 7 shows two examples coming in a small SOT23 package. The worst case power dissipation of the isolation switch is calculated as the minimum switch current limit $\times$ $R_{DS(on)}$ of the MOSFET. A standard SOT23 package or similar is able to provide sufficient power dissipation.

**Table 7. Isolation Switch Selection**

| COMPONENT SUPPLIER | CURRENT RATING |
|---|---|
| International Rectifier IRLML5203 | 3 A |
| Siliconix SI2343 | 3.1 A |

## Step-Down Converter

The non-synchronous step-down converter operates at a fixed switching frequency using a fast response voltage mode topology withfeed-forward input voltage. This topology allows simple internal compensation and it is designed to operate with ceramic output capacitors. The converter drives an internal 2.8-A N-Channel MOSFET switch. The MOSFET driver is referenced to the switch pin SWB. The N-Channel MOSFET requires a gate drive voltage higher than the switch pin to turn the N-Channel MOSFET on. This is accomplished by a boost strap gate drive circuit running of the step-down converter switch pin. When the switch pin SWB is at ground, the boot strap capacitor is charged to 8 V. This way the N-Channel Gate drive voltage is typically around 8 V.

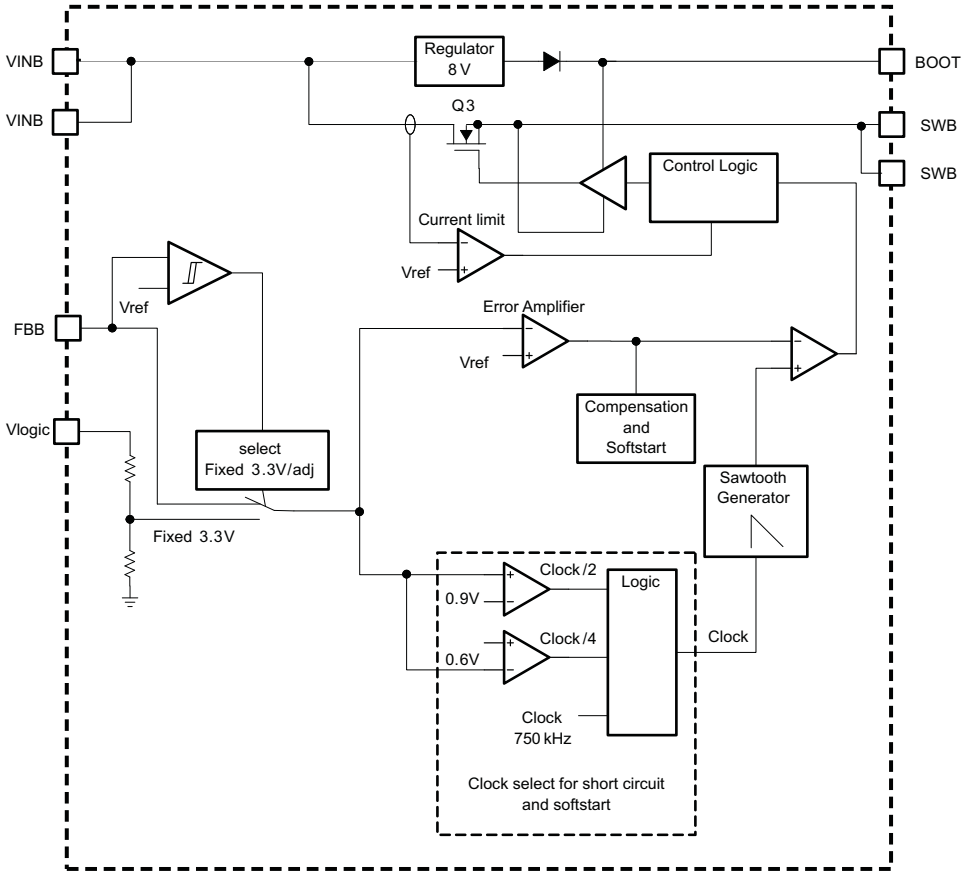



**Figure 25. Block Diagram Buck Converter**

### Soft-start (Step-Down Converter)

To avoid high inrush current during start-up, an internal soft-start is implemented. When the step-down converter is enabled, its reference voltage slowly rises from zero to its power good threshold of typically 90% of $V_{ref}$. When the reference voltage reaches this power good threshold, the error amplifier is released to its normal operation with its normal duty cycle. To further limit the inrush current during soft-start, the converter frequency is set to 1/4$^{th}$ of the switching frequency $f_s$ and $^{th}$ of $f_s$ determined by the comparator that monitors the feedback voltage. See the internal block diagram. The softstart is typically completed within 1 ms.

### Setting the Output Voltage, Adjustable or Fixed 3.3V (step-down converter)

The device supports a fixed 3.3-V output voltage when the feedback FBB is connected to GND. When using the external voltage divider any other output voltage can be programmed.

To set the adjustable output voltage of the step-down converter, use an external voltage divider to set the output voltage. The output voltage is calculated as:

$$V_{out} = 1.213\ V \times \left(1 + \frac{R9}{R10}\right) \quad (7)$$

with R10 ≈ 1.2 kΩ and internal reference voltage V(ref)typ = 1.213 V

At load currents < 1 mA, the device operates in discontinuous conduction mode. When the load current is reduced to zero, the output voltage rises slightly above the nominal output voltage. At zero load current, the device skips clock cycles but does not completely stops switching thus the output voltage sits slightly above the nominal output voltage. Therefore, the lower feedback resistor is selected to be around 1.2 kΩ to have always around 1 mA minimum load current.

### Selecting the Feed-forward Capacitor (step-down converter)

The feed-forward capacitor across the upper feedback resistor divider form a zero around 170 kHz and is calculated as:

$$C17 = \frac{1}{2 \times \pi \times 170kHz \times R9} = \frac{1}{2 \times \pi \times 170kHz \times 2k} = 468\ pF = 470\ pF \quad (8)$$

The capacitor value closest to the calculated value is selected.

### Inductor Selection (step-down converter)

The TPS65167 operates typically with a 10-µH inductor value. For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. This needs to be considered when selecting the appropriate inductor. To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that will be calculated as:

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (9)$$

With:

f = Switching Frequency (750 kHz)
L = Inductor Value (typically 10 µH)
$\Delta I_L$= Peak to Peak inductor ripple current
$I_{Lax}$ = Maximum Inductor current

The highest inductor current occurs at maximum Vin. A more conservative approach is to select the inductor current rating just for the minimum switch current limit of 2.8 A.

**Table 8. Inductor Selection (Step down converter)**

| INDUCTOR VALUE | COMPONENT SUPPLIER | DIMENSIONS in mm | Sat/DCR |
|---|---|---|---|
| 10 µH | Sumida CDRH8D43-100 | 8.3 × 8.3 × 4.5 | 4 A/29 mΩ |
| 10 µH | Wuerth 744066100 | 10 × 10 × 3.8 | 4 A/25 mΩ |
| 10 µH | Coilcraft DO3316P-103 | 12.95 × 9.4 × 5.51 | 3.9 A/38 mΩ |

### Rectifier Diode Selection (step-down converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the step-down converter. The averaged rectified forward current that the Schottky diode must be rated is calculated as the off time of the step-down converter times the minimum switch current of the TPS65167:

$$D = \frac{Vout}{Vin} \quad (10)$$

$I_{avg} = (1 - D) \times Isw = 1 - \frac{Vout}{Vin} \times 2.8\ A$ with Isw = minimum switch current of the TPS65167 (2.8 A)

A Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most of the applications. The Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$P_D = I_{avg} \times V_F = Isw \times (1 - D) \times V_F$ with Isw = minimum switch current of the TPS65167 (2.8 A)

**Table 9. Rectifier Diode Selection step-down Converter**

| CURRENT RATING Avg. | Or | $V_{forward}$ | $R_{\theta JA}$ | SIZE | COMPONENT SUPPLIER |
|---|---|---|---|---|---|
| 3A | 20V | 0.36 at 3A | 46°C/W | S.C. | MBRS320, International Rectifier |
| 2A | 20V | 0.44V at 2A | 75°C/W | SMB | SL22, Vishay Semiconductor |
| 2A | 20V | 0.5 at 2A | 75°C/W | SMB | SS22, Fairchild Semiconductor |

### Output Capacitor Selection (step-down converter)

The device is designed to work with ceramic output capacitors. Two 22-µF output capacitors are sufficient for most of the applications. Larger output capacitance improves the load transient response.

**Table 10. Output Capacitor Selection step-down Converter**

| CAPACITOR | VOLTAGE RATING | COMPONENT SUPPLIER |
|---|---|---|
| 2 × 22 µF/6.3 V | 6.3 V | Taiyo Yuden JMK212BJ226MG |

### Positive Charge Pump

The positive charge pump is a fully integrated charge pump switching automatically its gain between doubler and tripler mode. As shown in Figure 26, the input voltage of the positive charge pump is the SUP pin, that is connected to the output of the main boost converter Vs.

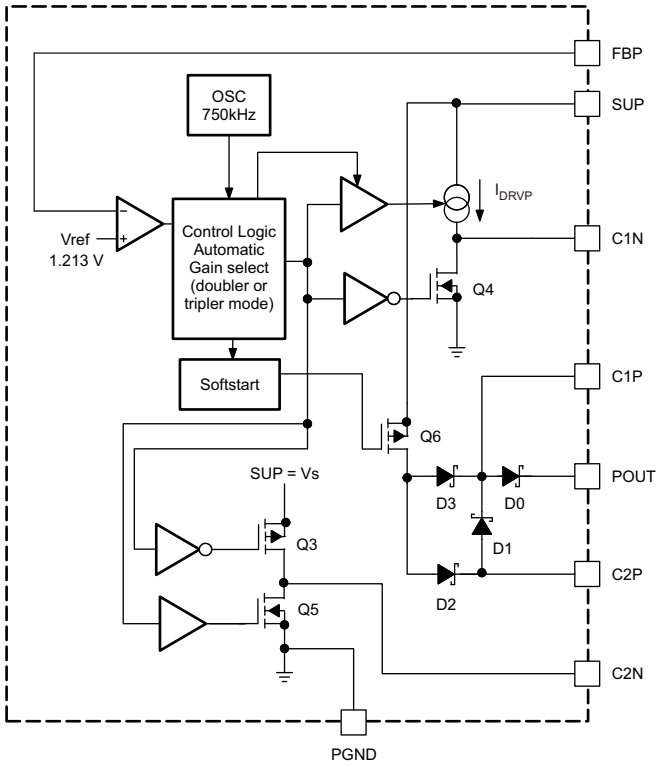



**Figure 26. Positive Charge Pump Block Diagram**

The charge pump requires two 330 nF flying capacitors and a 1 µF output capacitance for stable operation. The positive charge pump also supports a high voltage stress test by pulling the HVS pin high. This programs the output voltage to a fixed output voltage of 30 V (TPS65167 only) by using a internal voltage divider. The TPS65167A has this function disabled. In normal operation the HVS pin is pulled low and the output voltage is programmed with the external voltage divider.

$$V_{out} = 1.213\ V \times \left(1 + \frac{R4}{R5}\right) \tag{11}$$

$$R4 = R5 \times \left(\frac{V_{out}}{V_{FB}} - 1\right) = R5 \times \left(\frac{V_{out}}{1.213} - 1\right) \tag{12}$$

To minimize noise and leakage current sensitivity, keeping the lower feedback divider resistor R5 in the 20 kΩ range is recommended. A 100 pF feed-forward capacitor across the upper feedback resistor R4 is typically required. For the capacitor selection, see Table 11.

**Table 11. Output Capacitor Selection Positive Charge Pump**

| CAPACITOR | COMPONENT SUPPLIER | COMMENT |
|---|---|---|
| 330 nF/35 V | Taiyo Yuden GMK212BJ334KG | Flying capacitor C9, C20 |
| 1 µF/35 V | Taiyo Yuden GMK107BJ105KA | Output capacitor on POUT |

## High Voltage Switch Control (Gate Voltage Shaping)

The TPS65167 has a high voltage switch integrated to provide gate voltage modulation of VGH. If this feature is not required, then the CTRL pin has to be pulled high or connected to VIN. When the device is disabled or the input voltage is below the undervoltage lockout (UVLO), then both switches Q4 and Q5 are off, and VGH is discharge by a 1-kΩ resistor over Q8, as shown in Figure 27.

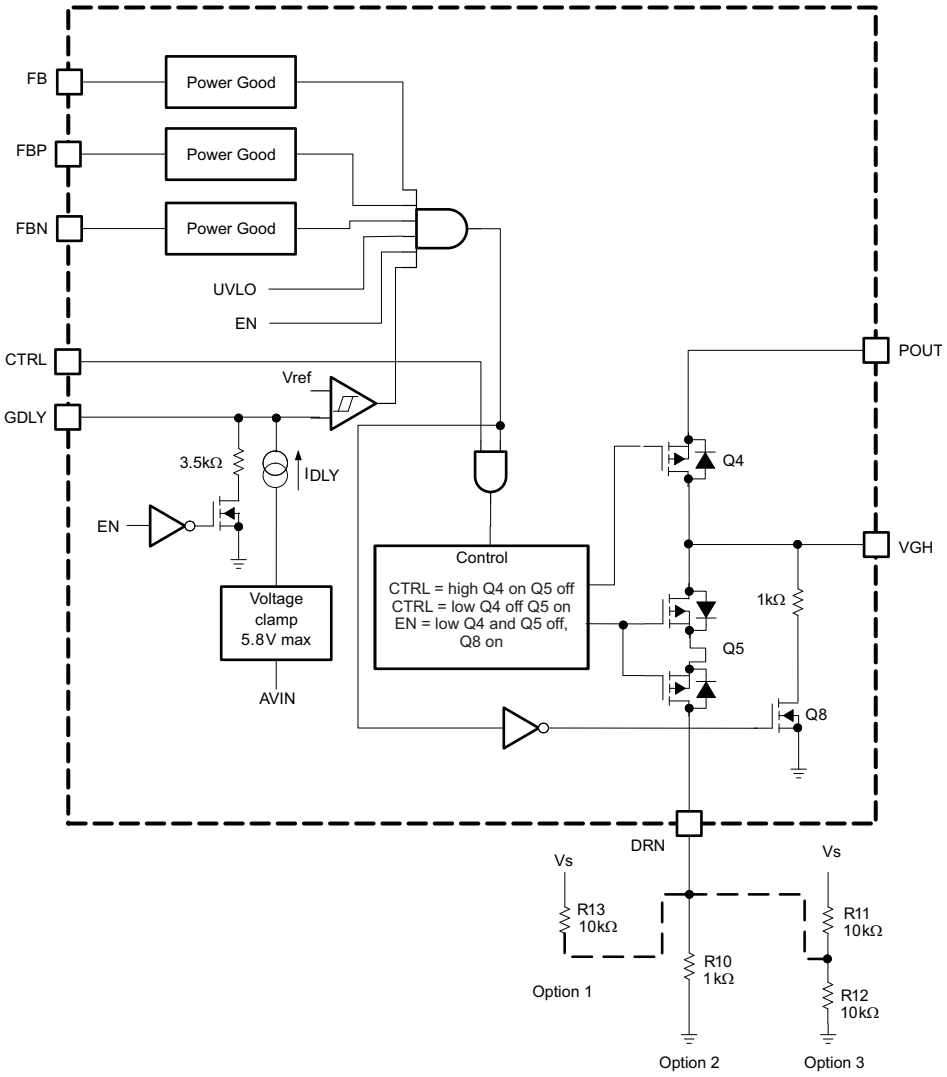
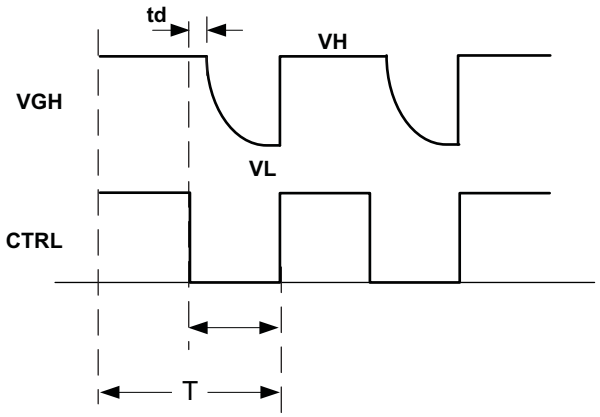



**Figure 27. High Voltage Switch (Gate Voltage Shaping) Block TPS65167**

To implement gate voltage shaping, the control signal from the LCD timing controller (TCON) is connected to CTRL. The CTRL pin is activated once the device is enabled, the input voltage is above the under voltage lockout, all the output voltages (Vs, VGL, VGH) are in regulation and the delay time set by the GDLY pin passed by. As soon as one of the outputs is pulled below its Power Good level, Q4 and Q5 are turned off, and VGH is discharged via a 1-kΩ resistor over Q8.

With CTRL=high, Q4 is turned on, and the charge pump output voltage is present at VGH. When the CTRL pin is pulled low, then Q4 is turned off, and Q5 is turned on discharging VGH. The slope and time for discharging VGH is determined by the LC Display capacitance and the termination on DRN. It is not required or recommended to connect an additional output capacitor on VGH. There are three options available to terminate the DRN pin. The chosen solution depends mainly on the LC Display capacitance and required overall converter efficiency.




Timing:

1. td is set by the capacitor CE
2. The slope is set by the resistor RE
3. VL is set by the voltage applied to VD

**Figure 28. High Voltage Switch (Gate Voltage Shaping) Timing Diagram**

Option 1 in Figure 27 discharges VGH to Vs. The lower the resistor the faster the discharge.

Option 3 in Figure 27 constantly draws current from Vs due to the voltage divider connected to Vs. The advantage of this solution is that the low level voltage VL is given by the voltage divider assuming the feedback resistor values are small and allow to discharge the LC Display capacitance during the time, toff. Therefore, the solution is not recommended for large display panels since the feedback divider resistors needs to be selected too low which draws too much current from Vs.

Option 2 does not draw any current from Vs and; therefore, is better in terms of converter efficiency. The voltage level VL where VGH is discharge to is determined by the LC Display capacitance, the resistor connected to DRN and the off time, $t_{off}$. The lower the resistor value connected to DRN the lower the discharge voltage level VL.

Adding any additional output capacitance to VGH is not recommend. If more capacitance is required, it needs to be added to POUT instead.

## High Voltage Stress Test (positive charge pump)

The TPS65167 incorporates a high voltage stress test where the output voltage of the boost converter Vs and the positive charge pump POUT are set to a higher output voltage compared to the nominal programmed output voltage. The High Voltage Stress test is enabled by pulling HVS pin to high. This sets POUT, respectively VGH to 30 V, and the output voltage of the boost converter Vs is programmed to a higher voltage determined by the resistor connected to RHVS. With HVS = high, the RHVS pin is pulled to GND which sets the voltage for the boost converter during High Voltage Stress.

The TPS65167A has the high voltage stress test for the positive charge pump POUT disabled. The high voltage stress test function is only enabled for the boost converter Vs.

## Negative Charge Pump Driver

The negative charge pump provides a regulated output voltage set by the external resistor divider. The negative charge pump inverts the input voltage applied to the SUPN pin and regulates it to the programmed voltage.

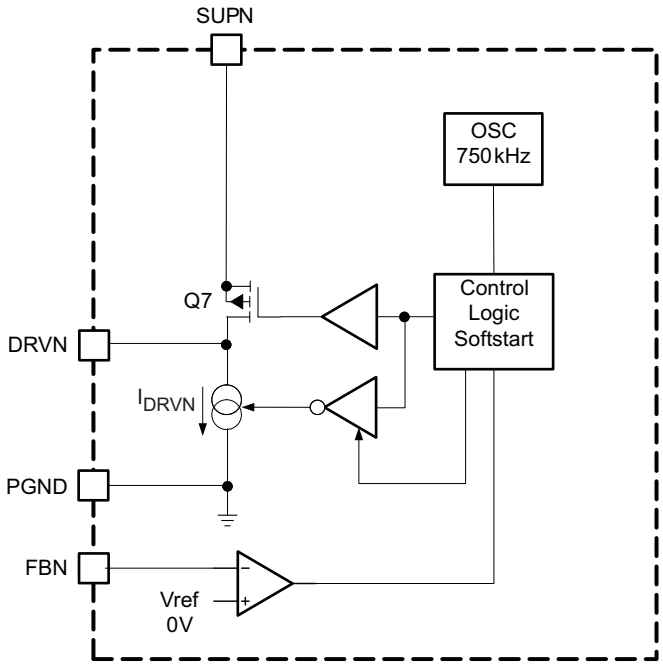



**Figure 29. Negative Charge Pump Block TPS65167**

The output voltage is VGL = (–Vin) + Vdrop. Vdrop is the voltage drop across the external diodes and internal charge pump MOSFETs.

Setting the output voltage:

$$V_{out} = -V_{REF} \times \frac{R7}{R8} = -1.213\ V \times \frac{R7}{R8} \quad (13)$$

$$R7 = R8 \times \frac{|V_{out}|}{V_{REF}} = R8 \times \frac{|V_{out}|}{1.213} \quad (14)$$

Since the reference output driver current should typically not exceed 30 µA, the lower feedback resistor value R8 should be in a range of 40 kΩ to 120 kΩ. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode has to be twice the load current of the output. For the external component selection refer to Table 12.

For a 20-mA output current, the dual Schottky diode BAV99 or BAT54 is recommended.

**Table 12. Capacitor Selection**

| CAPACITOR | COMPONENT SUPPLIER | COMMENT |
|---|---|---|
| 330 nF/35 V | Taiyo Yuden GMK212BJ334KG | Flying capacitor C15 |
| 2.2 µF/10 V | Taiyo Yuden LMK107BJ225KA | Output capacitor on VGL |
| BAV99/BAT54 | Any | Dual Schottky diode |

## LDO Controller Generating Vaux

The TPS65167 has a LDO controller using an external pass transistor. The input of the LDO controller can be the 12-V power supply input or the output of the 3.3-V logic rail, as generated by the step-down converter. The LDO controller is connected to the 3.3-V rail in order to minimize power losses across the external pass transistor.

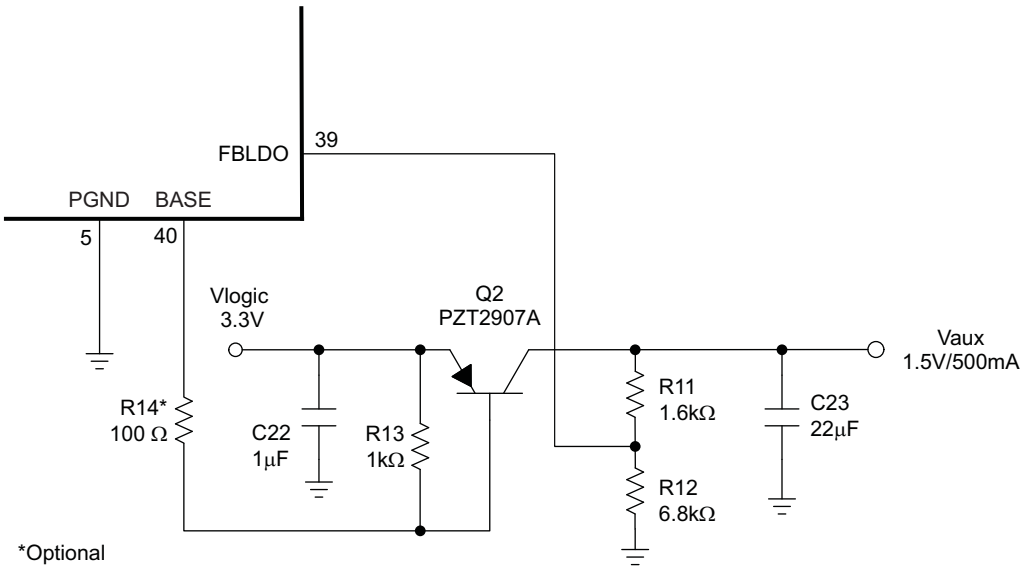



**Figure 30. LDO Controller Block TPS65167**

## Setting the output voltage, LDO controller

The output voltage of the LDO controller can be set with the resistor divider connected to the output of the LDO controller. To set the LDO controller output voltage to 1.2V the feedback FBLDO can be connected directly to the output. Any other output voltages is set using the external resistor divider and is calculated as:

$$V_{out} = 1.213\ V \times \left(1 + \frac{R11}{R12}\right) \quad (15)$$

## Input Capacitor and Output Capacitor Selection, LDO Controller

For input voltage filtering, a 1-µF input capacitor is sufficient. The output requires a least one 10-µF output capacitor for stability for load currents up to 300-mA. For load currents larger 300 mA, one 22-µF output capacitor is required. See Table 13 for the capacitor selection.

**Table 13. Output Capacitor Selection**

| CAPACITOR | Iout | COMPONENT SUPPLIER | COMMENT |
|---|---|---|---|
| 1 µF/10 V | | Taiyo Yuden LMK107BJ105KK | Input capacitor |
| 10 µF/10 V | ≤300 mA | Taiyo Yuden LMK212BJ106KG | Output capacitor |
| 22 µF/10 V | >300 mA | Taiyo Yuden LMK212BJ226MG | Output capacitor |

## Base and Emitter Base Resistor Selection

A 1-kΩ resistor (R13) is required across the emitter base of the external transistor. To limit the current into the base during a short-circuit event, a 100-Ω base resistor (R4) is required when the input is connected to the 3.3-V rail. If the input is connected to the 12-V rail, then a 1-kΩ (R4) resistor is required. R4 is optional and protects the TPS65167 in case of a short-circuit event at the output of the LDO controller.

## External Transistor Selection

The external transistor is selected based on the required output current and collector saturation voltage. The maximum collector saturation voltage is only important as the output voltage is close to the input voltage. This is the case for a 3.3 V to 2.5 V conversion where the collector saturation voltage of the external transistor is lower than 800 mV. To use low cost external transistors, the TPS65167 provides a minimum base drive current of 25 mA. The other important parameter is the maximum power dissipation the external transistor must be able to handle. The power dissipation is the output current times the input to output voltage difference. See Table 14 for the transistor selection

**Table 14. Transistor Selection**

| CAPACITOR | Iout | COMPONENT SUPPLIER | COMMENT |
|---|---|---|---|
| PZT2907A | 500 mA | Any | 3.3 V to ≤2.5 V conversion at 150 mA<br>3.3 V to ≤1.6 V conversion at 500 mA |
| BCP52 | 1A | Any | 3.3 V to ≤2.5 V conversion |
| BCP69 | 1A | Any | 3.3 V to ≤2.5 V conversion |

## PCB Layout Design Guidelines

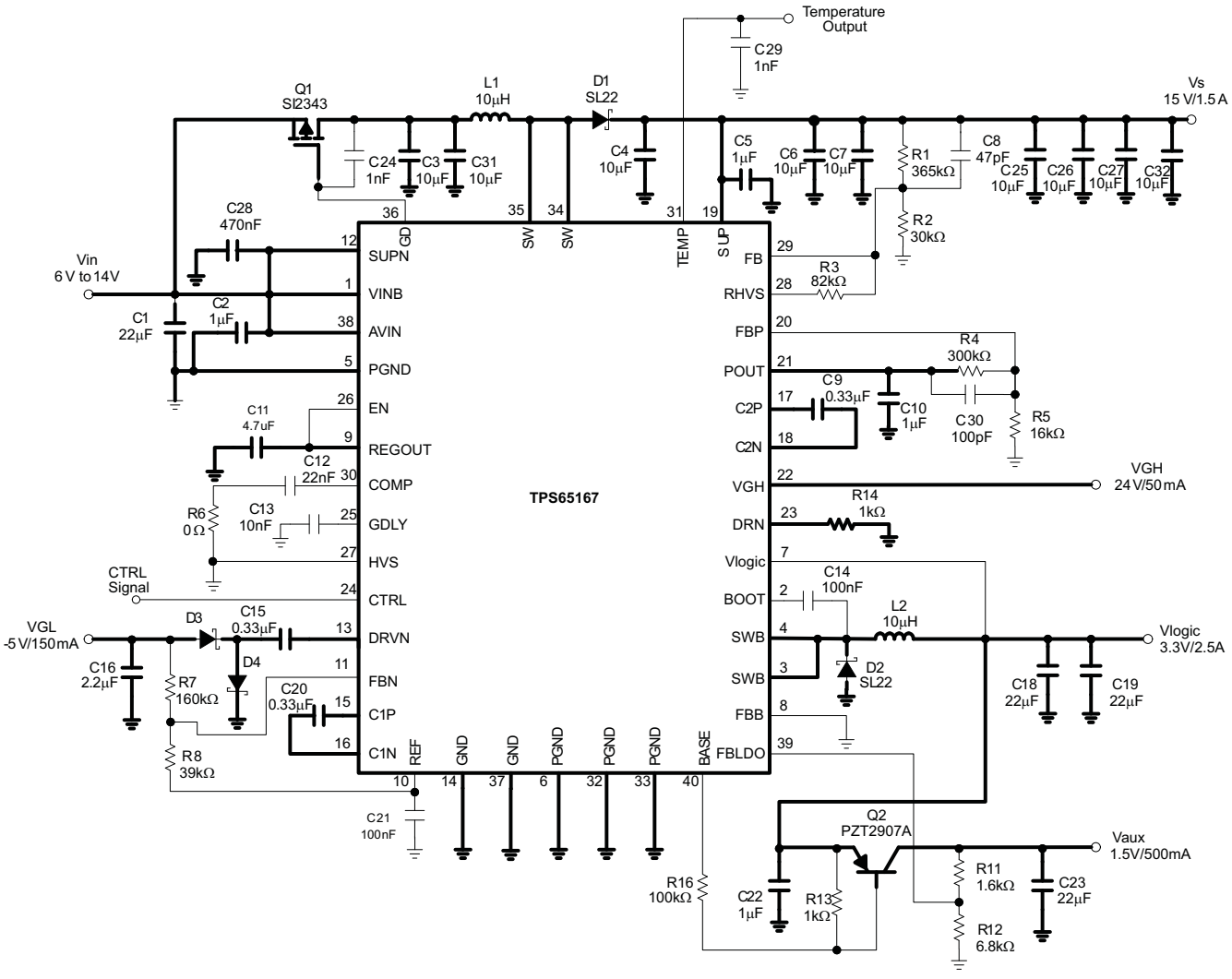



**Figure 31. PCB Layout**

1. Place the power components outlined in bold first on the PCB.

2. Route the traces outlined in bold with wide PCB traces.
3. Place a 1-µF bypass capacitor directly from the SUP pin to GND and from AVIN to GND.
4. Use a short and wide trace to connect the SUP pin to the output of the boost converter Vs.
5. Place a 470-nF bypass capacitor directly from the SUPN pin to GND.
6. Place the 100-nF reference capacitor directly from REF to GND close to the IC pins.
7. The feedback resistor for the negative charge pump between FBN and REF needs to be >40 kΩ.
8. Use short traces for the charge pump drive pin (DRVN) of VGL because the traces carry switching waveforms.
9. Place the feedback resistors of the negative charge pump away from the DRVN trace to minimize coupling
10. Place the flying capacitors as close as possible to the C1P, C1N and C2P, C2N pin.
11. Solder the PowerPad™ of the QFN package to GND and use thermal vias to lower the thermal resistance.
12. A solid PCB ground structure is essential for good device performance.

    The power pad is the analog ground connected to the internal reference

    Pin 32, 33 are the power grounds for the boost converter Vs

    Pin 5 is the power ground for the step-down converter Vlogic and internal digital circuit

    Pin 6 is the power ground for the negative charge pump VGL

    Pin 14 is the power ground for the positive charge pump POUT

    Pin 37 is the analog ground for the internal reference
13. For more layout recommendations, see the TPS65167 evaluation module (EVM)

## TYPICAL APPLICATION

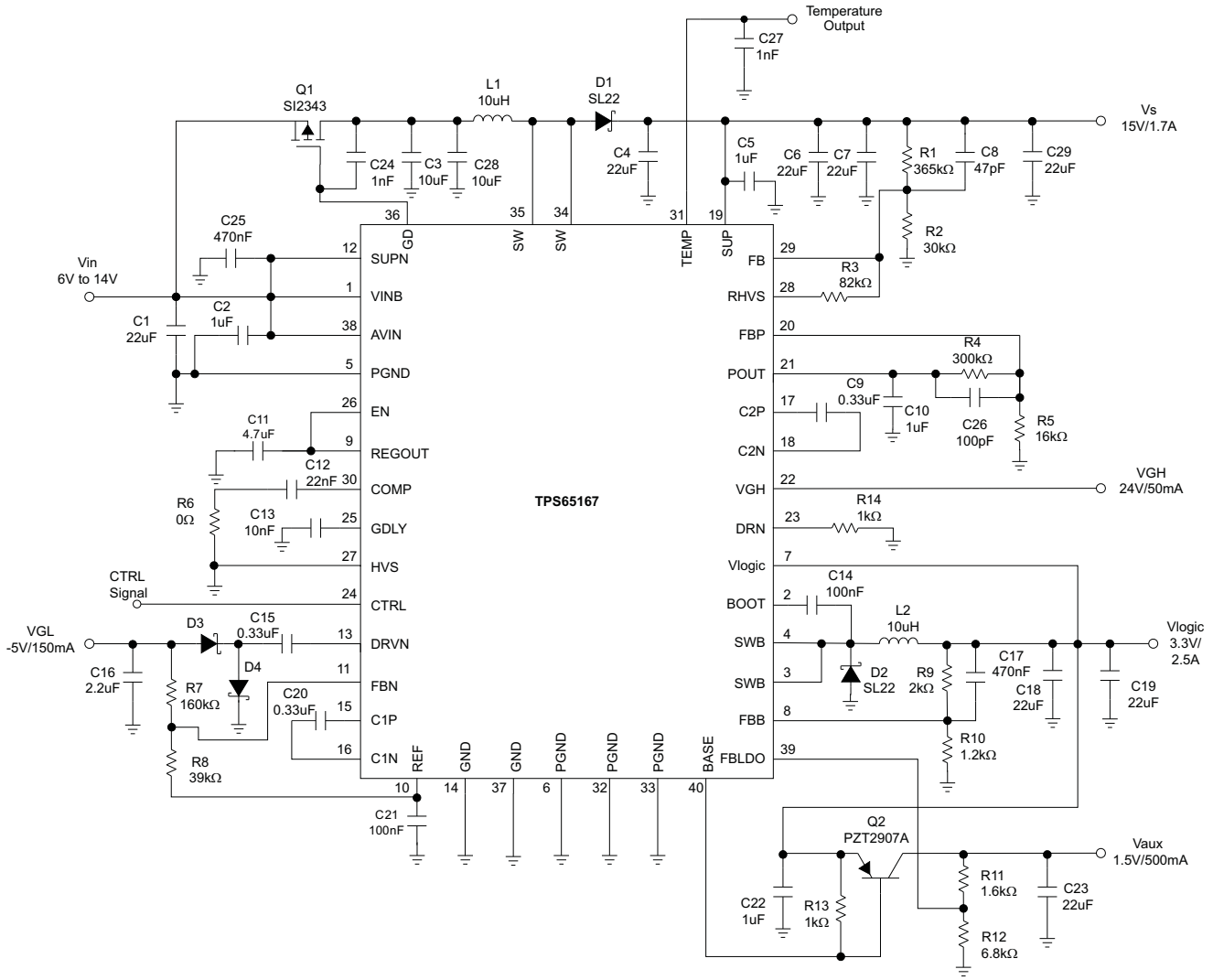



**Figure 32. Typical Application with adjustable step down converter**

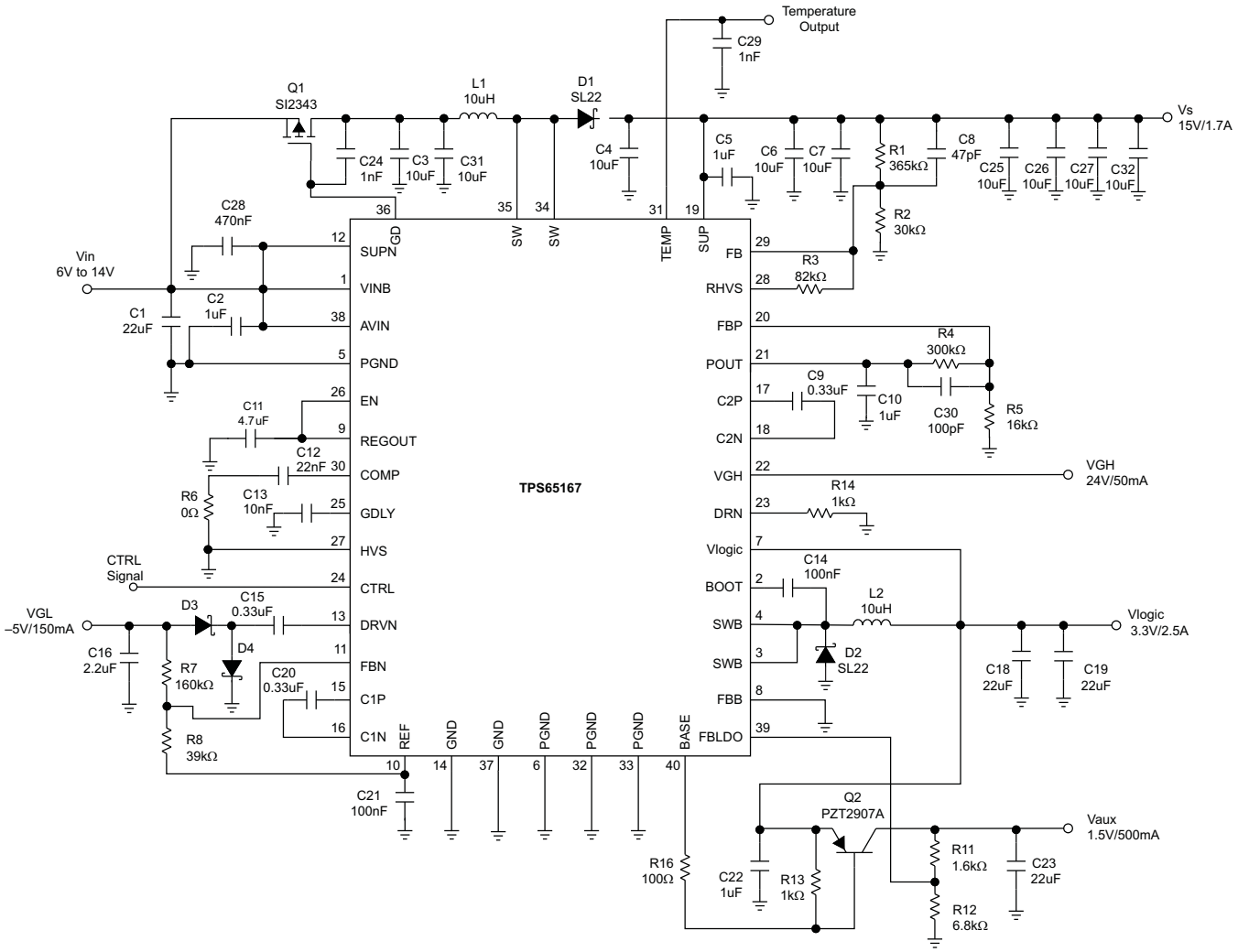



**Figure 33. Typical Application With 3.3V Fixed Output Voltage Step Down Converter**

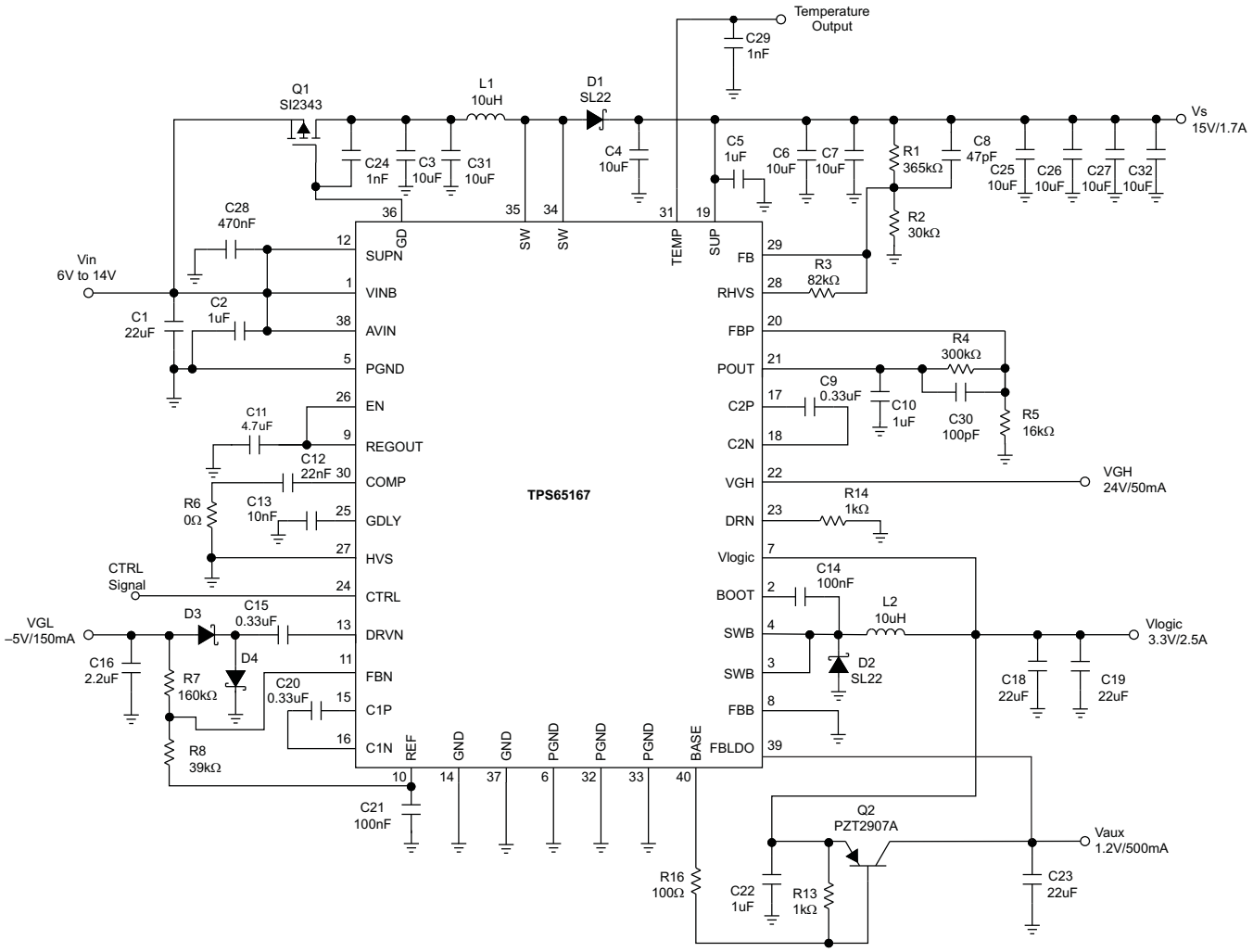



**Figure 34. Typical Application With 1.2V LDO Controller**

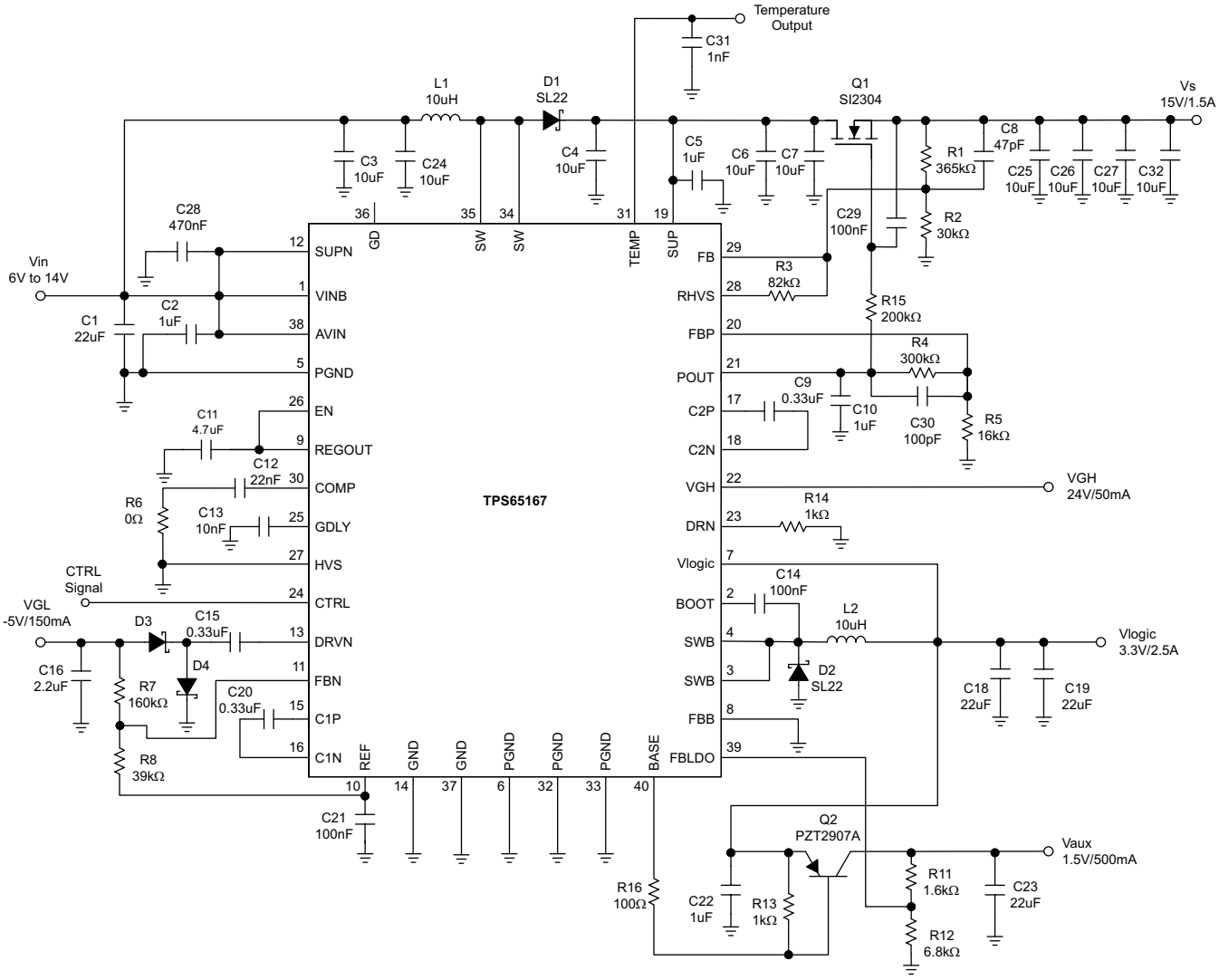



**Figure 35. Typical Application Using Isolation Switch at the Output of the Boost Converter**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65167ARHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65167A | Samples |
| TPS65167ARHARG4 | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65167A | Samples |
| TPS65167RHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65167 | Samples |
| TPS65167RHATG4 | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TPS 65167 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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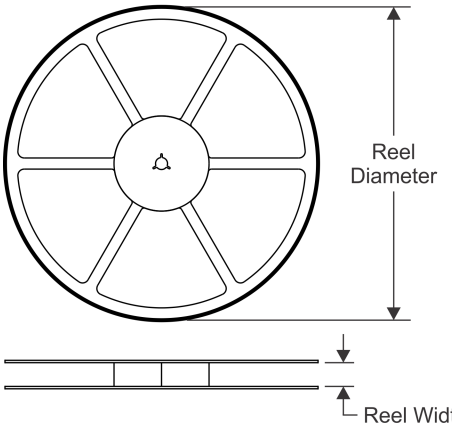
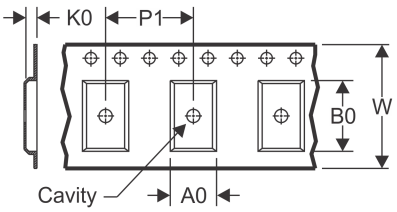
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

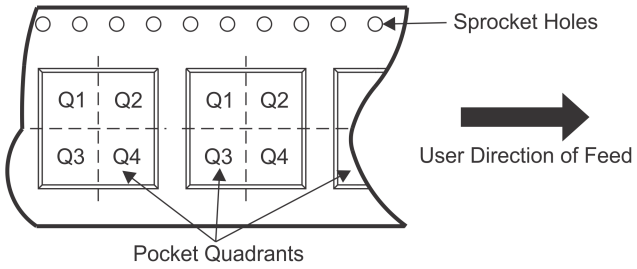



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

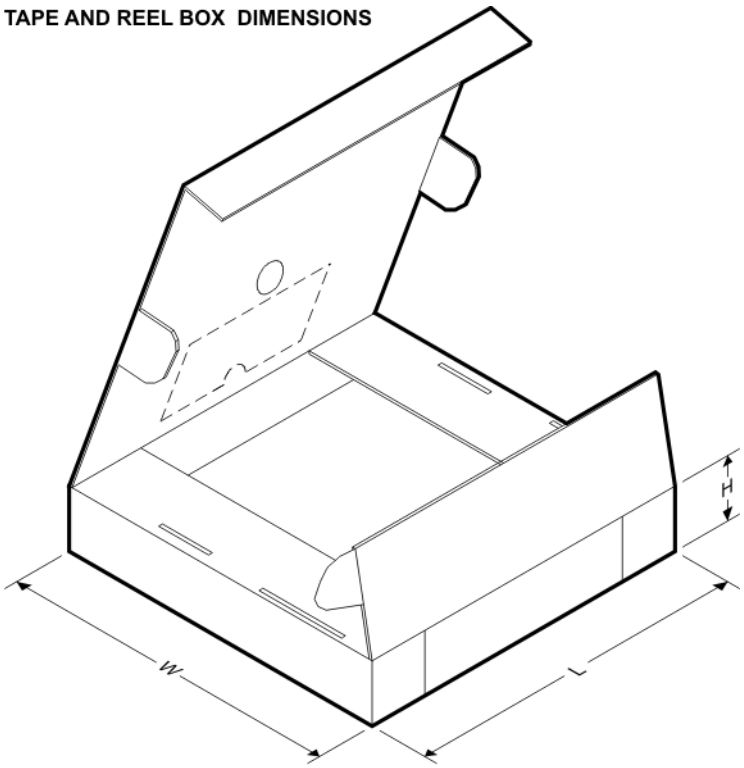
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65167ARHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65167ARHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.5 | 12.0 | 16.0 | Q2 |

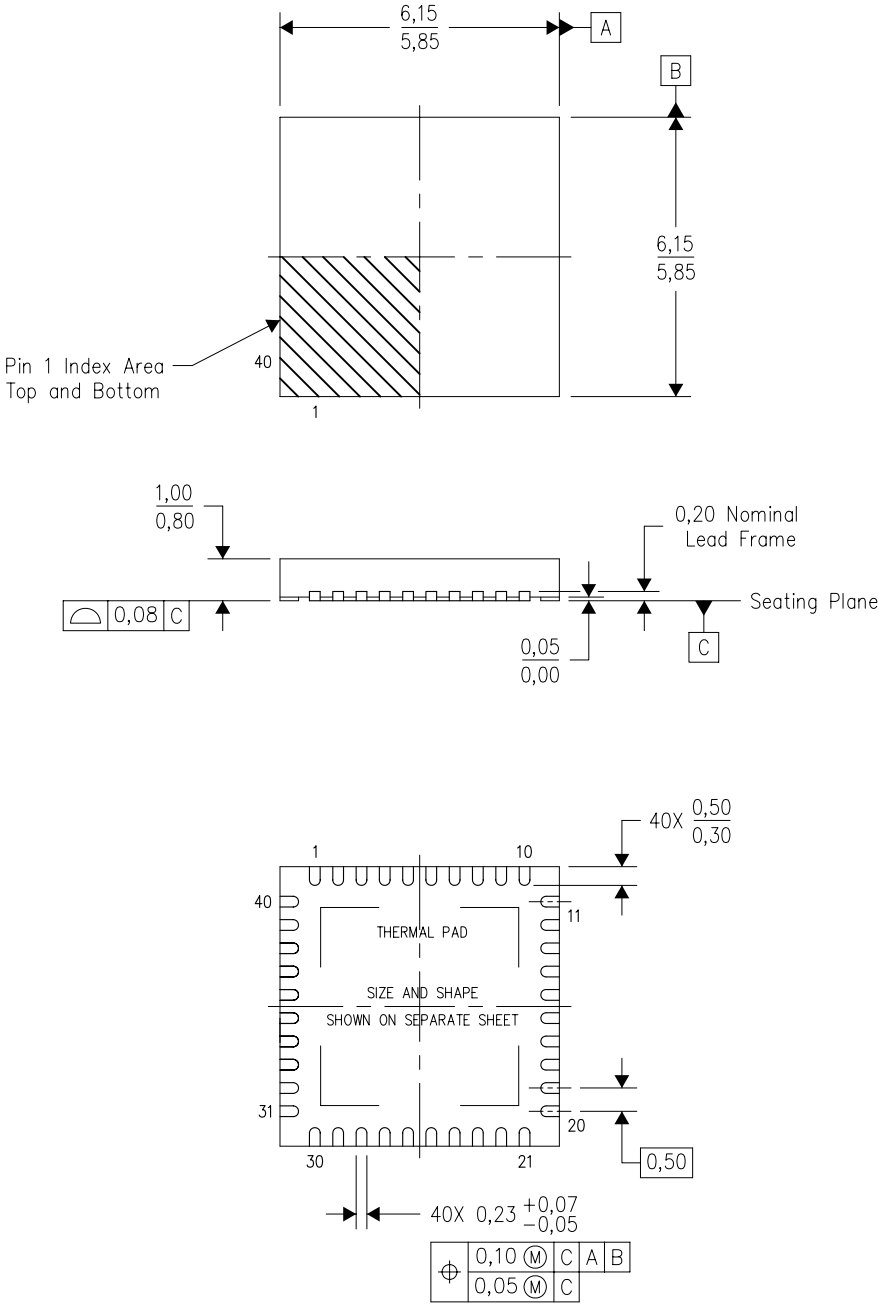
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65167ARHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS65167ARHAR | VQFN | RHA | 40 | 2500 | 367.0 | 367.0 | 38.0 |

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

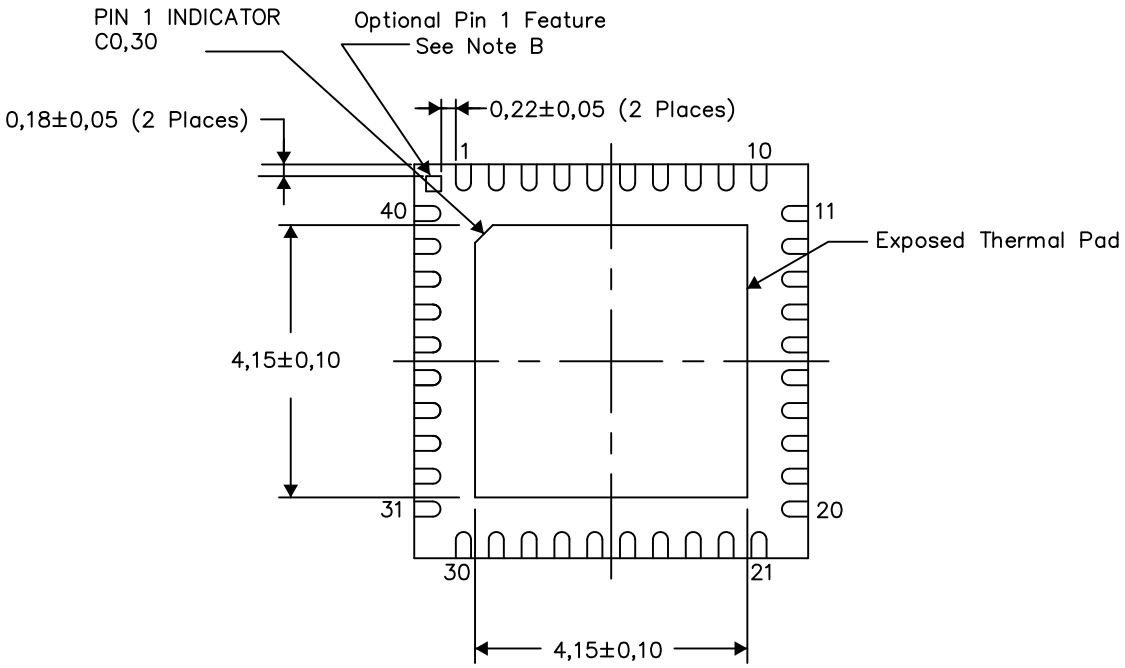
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

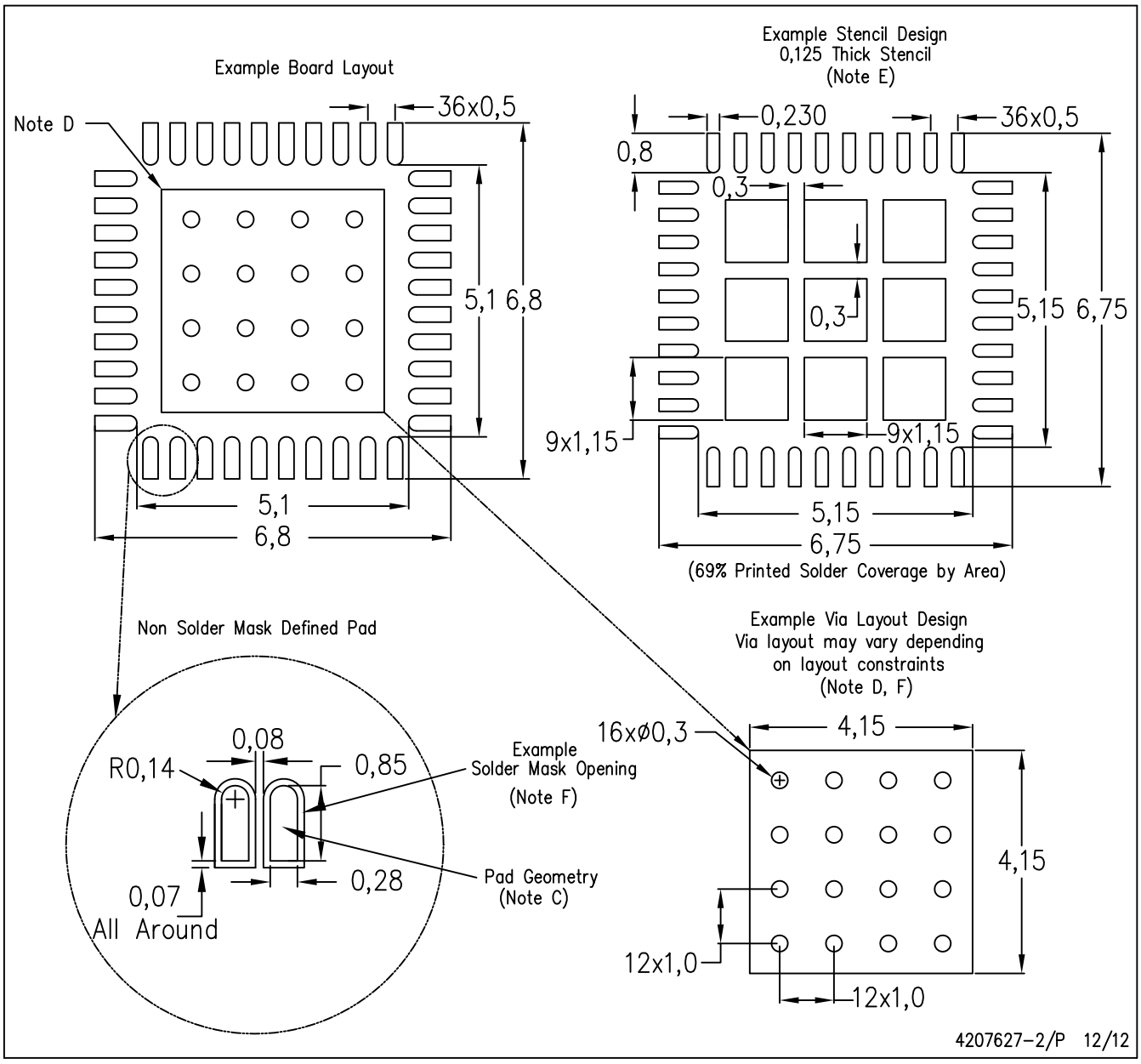
Exposed Thermal Pad Dimensions

4206355–2/U 12/12

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

# RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## IMPORTANT NOTICE

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