



CMOS Low Cost 10 Bit Multiplying D/A Converter

General Description

The MX7533 is a low cost CMOS 4-quadrant multiplying digital-to-analog converter (DAC). An advanced silicon gate CMOS process combines 10 bit linearity, low power consumption, and excellent long term stability. Thin-film resistors provide 1.4% untrimmed gain error and less than 0.1% gain change with temperature over all operating ranges.

The device operates from a single +5V to +15V supply. All digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's MX7533 is pin and functionally compatible with Analog Devices' AD7533 as well as the AD7520. It is packaged in 16-lead DIP and small outline packages.

Applications

Machine and Motion Control Systems

Automatic Test Equipment

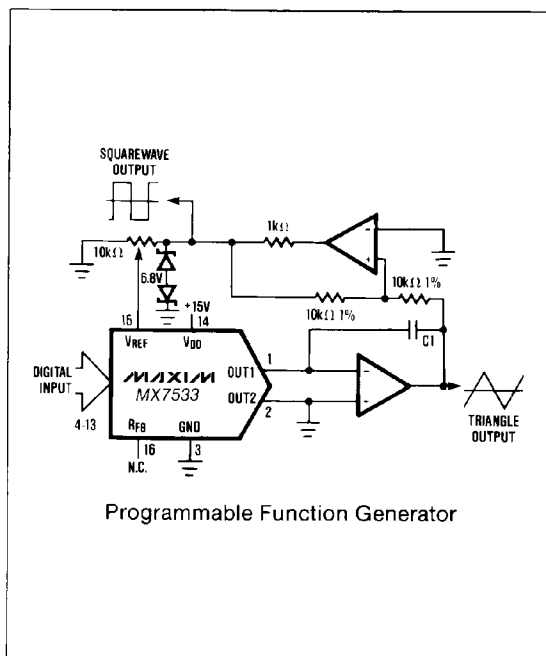
μ P Controlled Calibration Circuitry

Programmable Gain Amplifiers

Digitally Controlled Filters

Programmable Power Supplies

Typical Operating Circuit



Features

- ◆ 10 Bit Resolution
- ◆ 8, 9, and 10 Bit End Point Linearity
- ◆ Low Power Consumption - 20mW
- ◆ Four-Quadrant Multiplication
- ◆ TTL and CMOS Compatible
- ◆ Pin-For-Pin Second Source

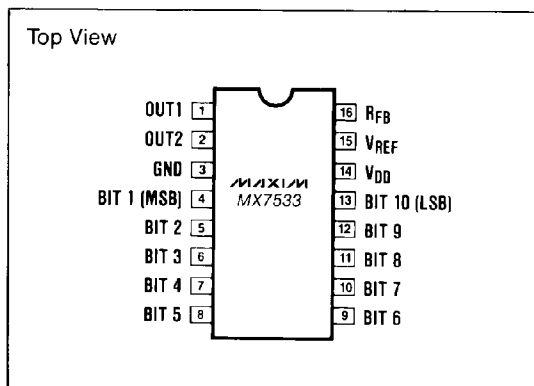
Ordering Information

PART	TEMP RANGE	PACKAGE*	ERROR
MX7533JN	0°C to +70°C	Plastic DIP	0.2%
MX7533KN	0°C to +70°C	Plastic DIP	0.1%
MX7533LN	0°C to +70°C	Plastic DIP	0.05%
MX7533JCWE	0°C to +70°C	Small Outline	0.2%
MX7533KCWE	0°C to +70°C	Small Outline	0.1%
MX7533LCWE	0°C to +70°C	Small Outline	0.05%
MX7533J/D	0°C to +70°C	Dice	0.2%
MX7533AQ	-25°C to +85°C	CERDIP**	0.2%
MX7533BQ	-25°C to +85°C	CERDIP**	0.1%
MX7533CQ	-25°C to +85°C	CERDIP**	0.05%
MX7533AD	-25°C to +85°C	Ceramic	0.2%
MX7533BD	-25°C to +85°C	Ceramic	0.1%
MX7533CD	-25°C to +85°C	Ceramic	0.05%
MX7533SQ	-55°C to +125°C	CERDIP**	0.2%
MX7533TQ	-55°C to +125°C	CERDIP**	0.1%
MX7533UQ	-55°C to +125°C	CERDIP**	0.05%
MX7533SD	-55°C to +125°C	Ceramic	0.2%
MX7533TD	-55°C to +125°C	Ceramic	0.1%
MX7533UD	-55°C to +125°C	Ceramic	0.05%

* All devices — 16 lead packages.

**** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.**

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	-0.3V, +17V
V_{REF} to GND	$\pm 25V$
R_{FB} to GND	$\pm 25V$
Digital Input Voltage to GND	-0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1)	-0.3V, V_{DD}
Power Dissipation	
Plastic DIP (Derate 8.3mW/°C above +70°C)	670mW
Ceramic, CERDIP, Small Outline (Derate 6mW/°C above +75°C)	450mW

Operating Temperature Range	
Commercial J/K/L	0°C to +70°C
Industrial A/B/C	-25°C to +85°C
Military S/T/U	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10 secs)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = GND$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				10			Bits
Relative Accuracy (Note 2)		MX7533J/A/S MX7533K/B/T MX7533L/C/U				± 0.2 ± 0.1 ± 0.05	% FSR
Gain Error (Note 2,3)		Digital Inputs = V_{INH}	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			± 1.4 ± 1.5	% FSR
Power Supply Rejection (Note 4) Δ Gain/ ΔV_{DD}	PSRR	$V_{DD} = +14V$ to $+17V$	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			0.005 0.008	%/% V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL} , $V_{REF} = \pm 10V$	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			± 50 ± 200	nA
		OUT2, Digital Inputs = V_{INH} , $V_{REF} = \pm 10V$	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			± 50 ± 200	
V_{REF} Input Resistance	R_{REF}	$T_A = +25^{\circ}C$		5	10	20	k Ω
V_{REF} Resistance Tempco					-300		ppm/ $^{\circ}C$
DYNAMIC PERFORMANCE							
Output Current Settling Time (Note 5)		To 0.05% of FSR, $R_L = 100\Omega$, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH} .	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			600 800	ns
Feedthrough Error (Note 4)		Digital Inputs = V_{INL} , $V_{REF} = \pm 10V$, 100KHz Sinewave	$T_A = +25^{\circ}C$ T_{MIN} to T_{MAX}			± 0.05 ± 0.1	% FSR
Output Capacitance (Note 4)	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 35	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			35 100	
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}				± 1	μA
Input Capacitance (Note 4)						5	pF
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	+15V $\pm 10\%$ for Rated Accuracy		+13.5		+16.5	V
		Accuracy Not Guaranteed (Note 4)		+5		+16.5	
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.

Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = $-(V_{REF} - 1LSB)$ in unipolar mode.

Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.

Note 4: Guaranteed by design but not 100% tested.

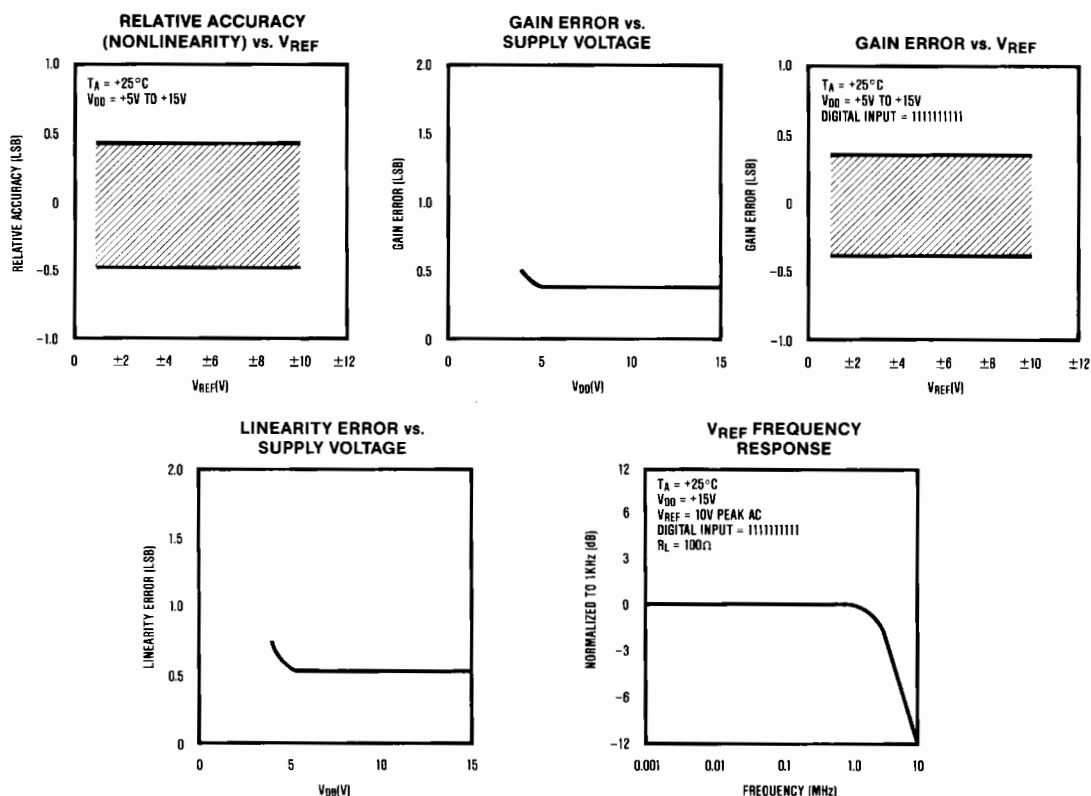
Note 5: Guaranteed by design and sample tested at +25°C to ensure compliance.

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Typical Operating Characteristics



Detailed Description

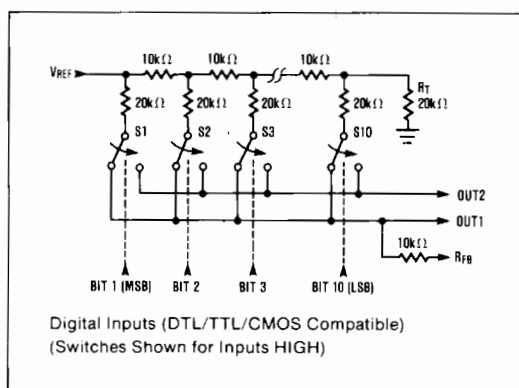


Figure 1. MX7533 Functional Diagram

The basic MX7533 DAC circuit consists of a thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binary weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and an external reference. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 10k Ω and does not change with digital input code. The $I_{REF}/1024$ current source, which is actually the ladder termination resistor (R_T , Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

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Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must

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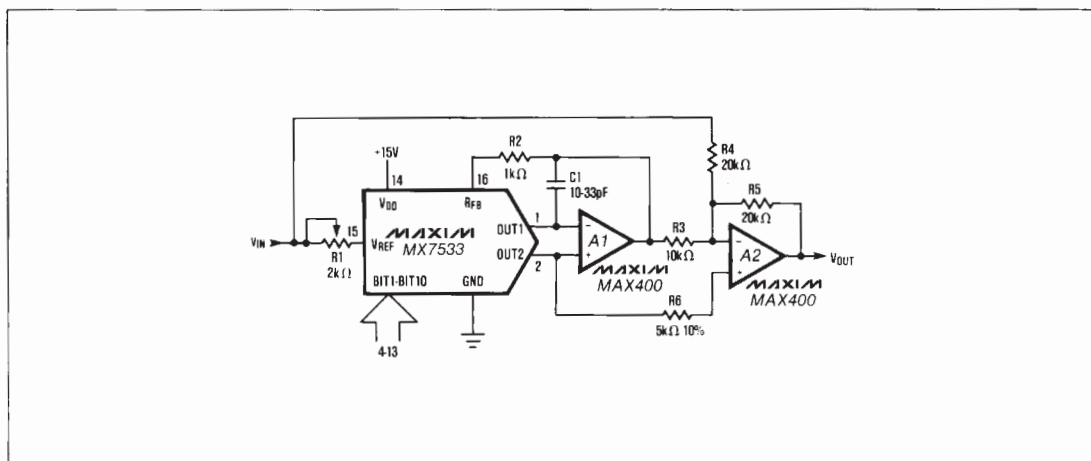


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF} , and the DAC outputs.

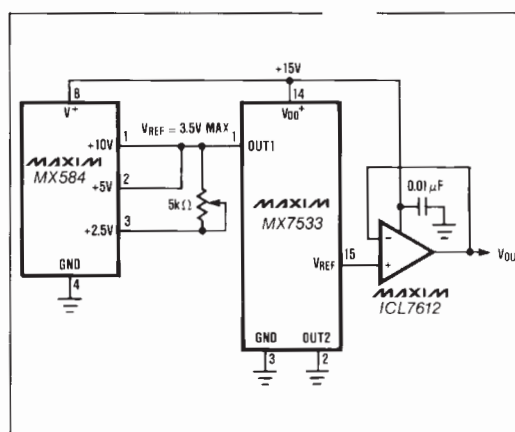


Figure 6. Voltage Mode Operation

Table 1: Code Table —
Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF} (\frac{1}{4} + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF} (\frac{1}{2} - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Table 2: Code Table —
Bipolar (Offset Binary) Operation

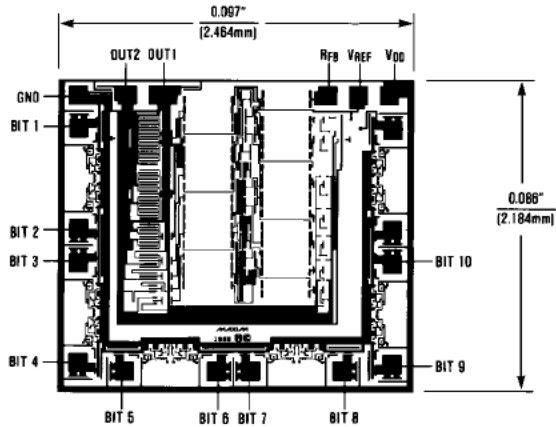
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF} (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF} (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

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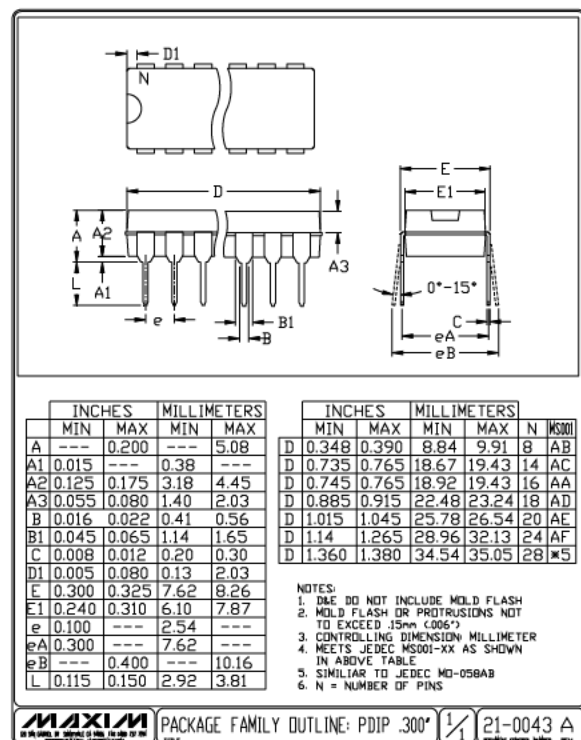
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Chip Topography



Package Information

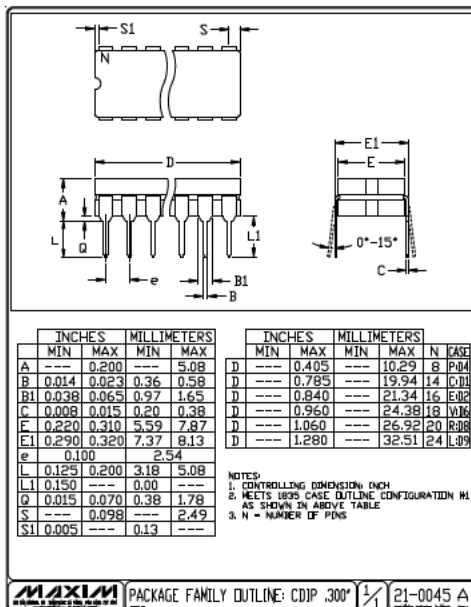
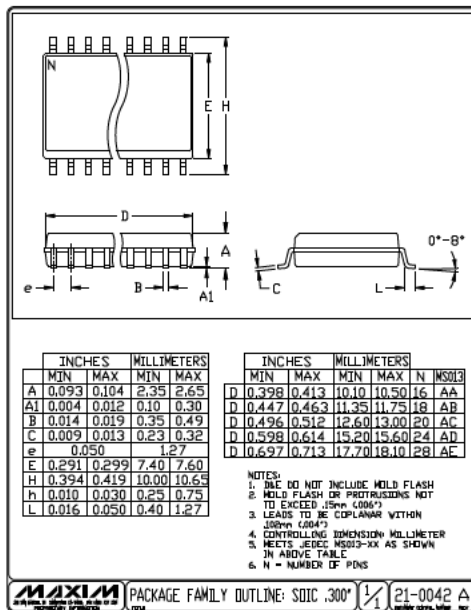


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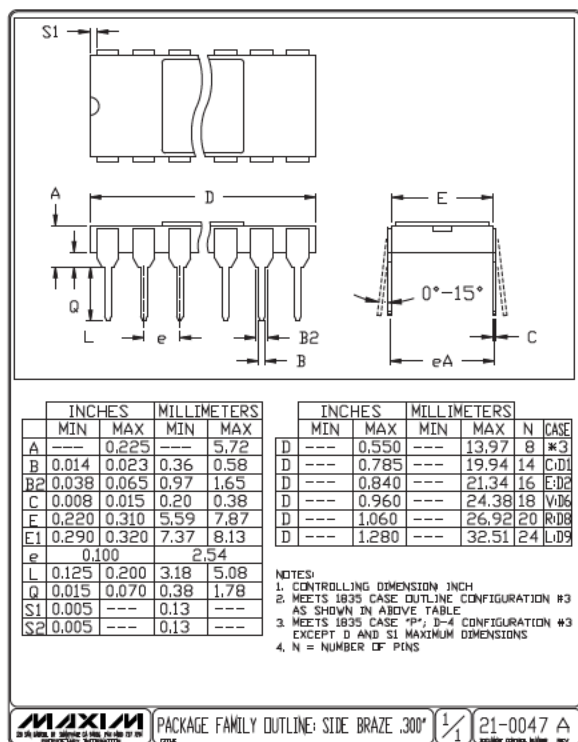


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Package Information (continued)



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