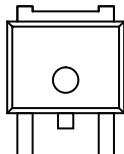


## Automotive N-Channel 60 V (D-S) 175 °C MOSFET

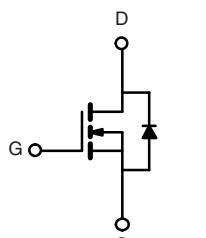
PRODUCT SUMMARY <sup>d</sup>	
$V_{DS}$ (V)	60
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.042
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.060
$I_D$ (A)	15
Configuration	Single

TO-252



Drain Connected to Tab

Top View



N-Channel MOSFET

### FEATURES

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested
- AEC-Q101 Qualified
- Package with Low Thermal Resistance
- Material categorization:  
For definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
FREE

### ORDERING INFORMATION

Package	TO-252
Lead (Pb)-free and Halogen-free	SQD15N06-42L-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	60	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25$ °C <sup>a</sup>	$I_D$	15	A
	$T_C = 125$ °C		10	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	15	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	50	
Single Pulse Avalanche Current	$L = 0.1$ mH	$I_{AS}$	18	mJ
Single Pulse Avalanche Energy		$E_{AS}$	16.2	
Maximum Power Dissipation <sup>b</sup>	$T_C = 25$ °C	$P_D$	37	W
	$T_C = 125$ °C		11	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	°C

### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	50	°C/W
Junction-to-Case (Drain)		$R_{thJC}$	4	

#### Notes

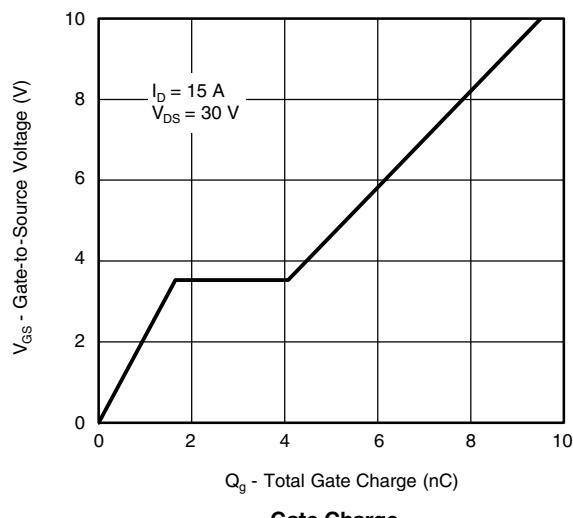
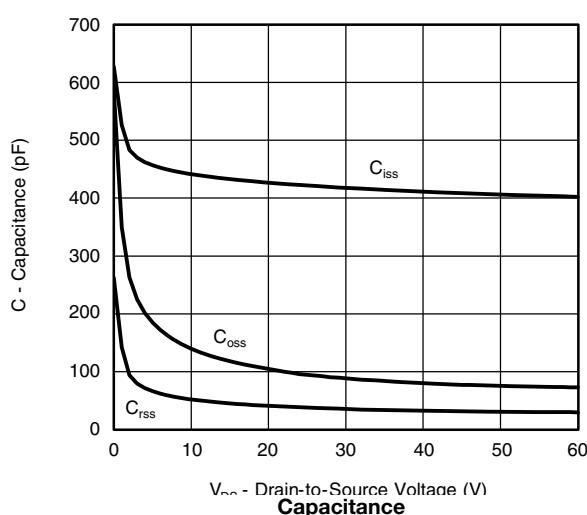
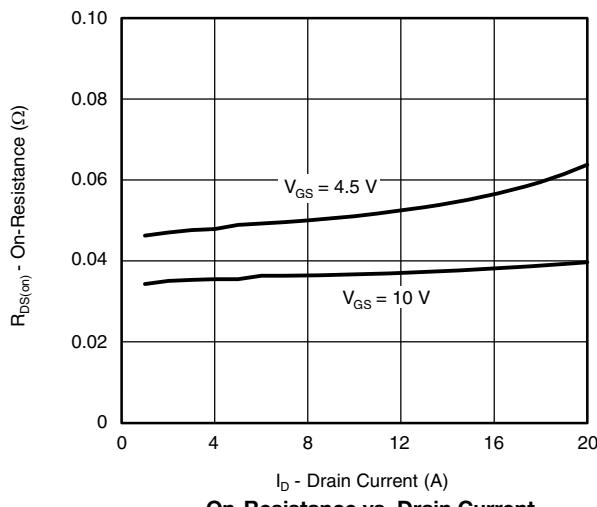
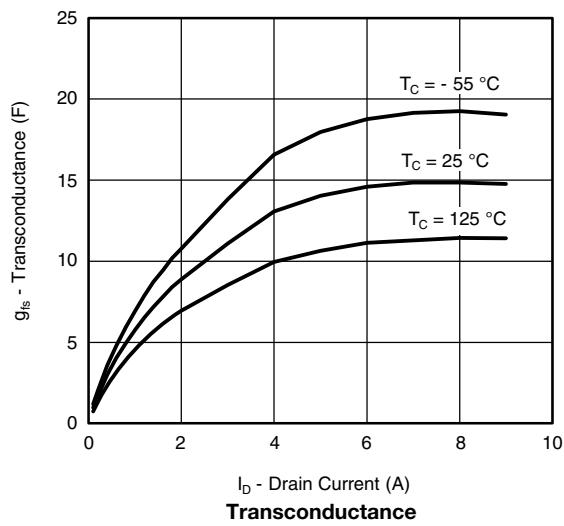
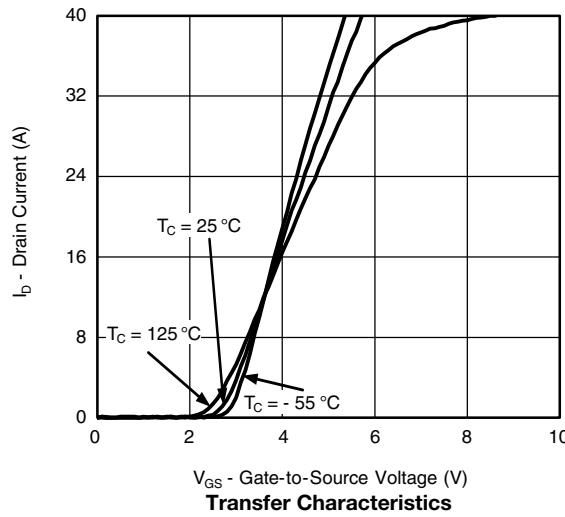
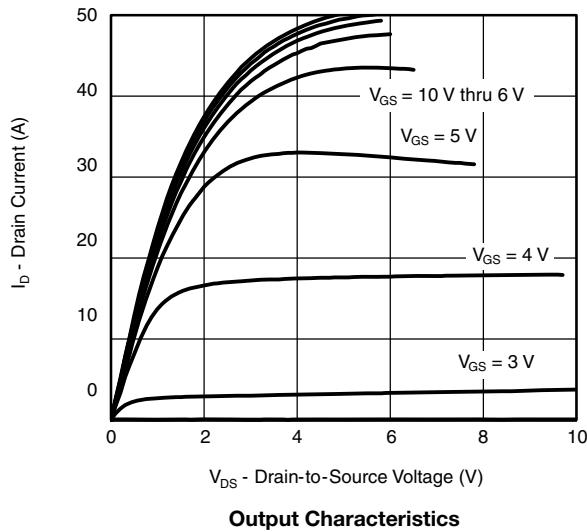
- Package limited.
- Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %.
- When mounted on 1" square PCB (FR-4 material).

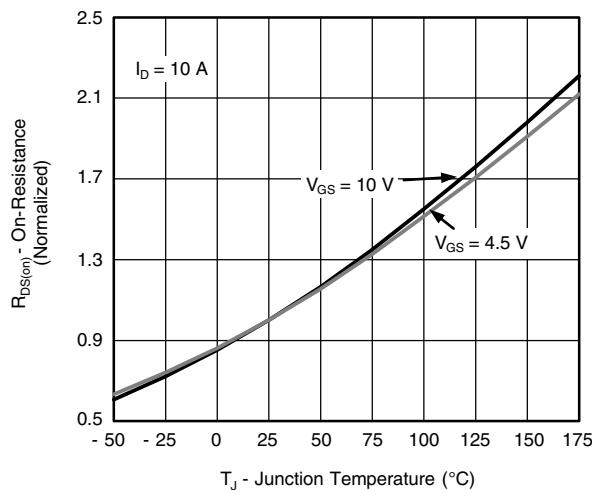
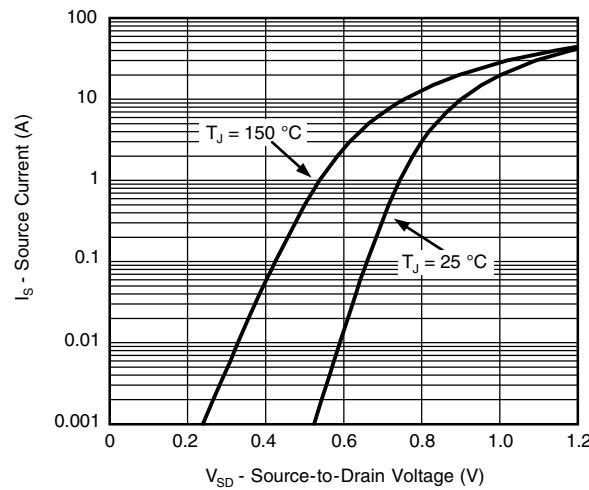
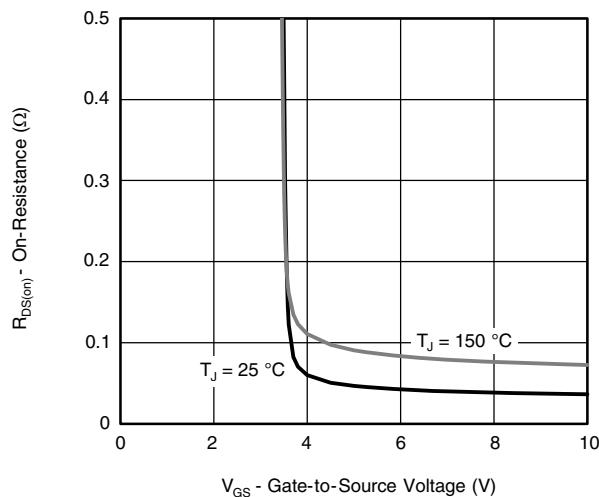
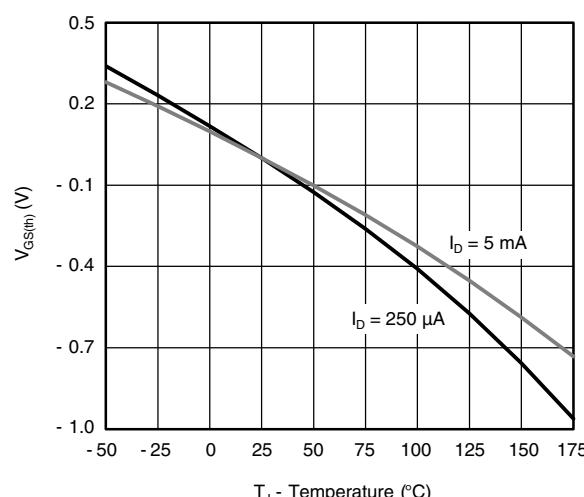
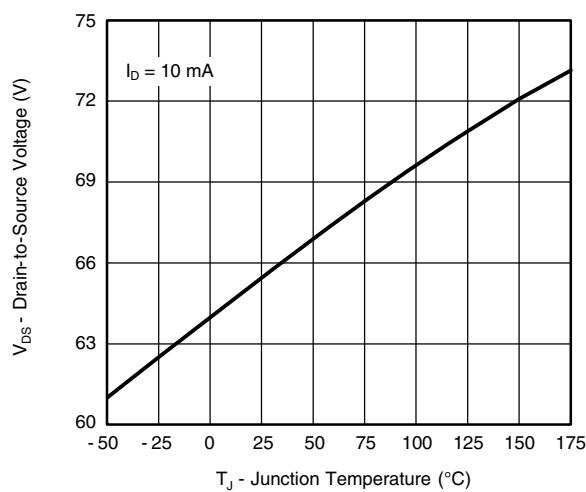
<b>SPECIFICATIONS</b> ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		60	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		1.5	2	2.5		
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1	$\mu\text{A}$	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$ , $T_J = 125^\circ\text{C}$	-	-	50		
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$ , $T_J = 175^\circ\text{C}$	-	-	150		
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	30	-	-	A	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	-	0.036	0.042	$\Omega$	
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$ , $T_J = 125^\circ\text{C}$	-	-	0.075		
		$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$ , $T_J = 175^\circ\text{C}$	-	-	0.090		
		$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$ , $T_J = 125^\circ\text{C}$	-	0.092	-		
		$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$ , $T_J = 175^\circ\text{C}$	-	0.110	-		
		$V_{GS} = 4.5\text{ V}$	$I_D = 10\text{ A}$	-	0.048	0.060		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 6\text{ A}$		-	11	-	S	
<b>Dynamic<sup>b</sup></b>								
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$	-	425	535	pF	
Output Capacitance	$C_{oss}$			-	95	120		
Reverse Transfer Capacitance	$C_{rss}$			-	40	50		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}$ , $I_D = 15\text{ A}$	-	9.5	15	nC	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	1.7	-		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	2.5	-		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1.8	3.6	5.4	$\Omega$	
Turn-On Delay Time <sup>c</sup>	$t_{d(\text{on})}$	$V_{DD} = 30\text{ V}$ , $R_L = 2\text{ }\Omega$ $I_D \geq 15\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$		-	5	8	ns	
Rise Time <sup>c</sup>	$t_r$			-	10	15		
Turn-Off Delay Time <sup>c</sup>	$t_{d(\text{off})}$			-	13	20		
Fall Time <sup>c</sup>	$t_f$			-	8	12		
<b>Source-Drain Diode Ratings and Characteristics<sup>b</sup></b>								
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	50	A	
Forward Voltage	$V_{SD}$	$I_F = 10\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.9	1.2	V	
Reverse Recovery Time	$t_{rr}$	$I_F = 15\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		-	29	60	ns	

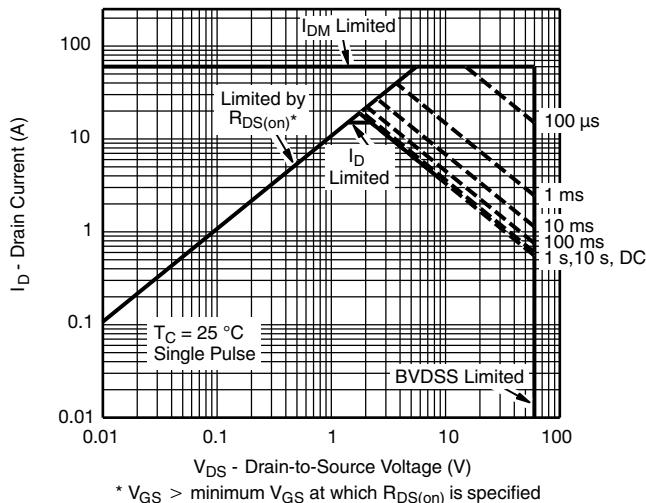
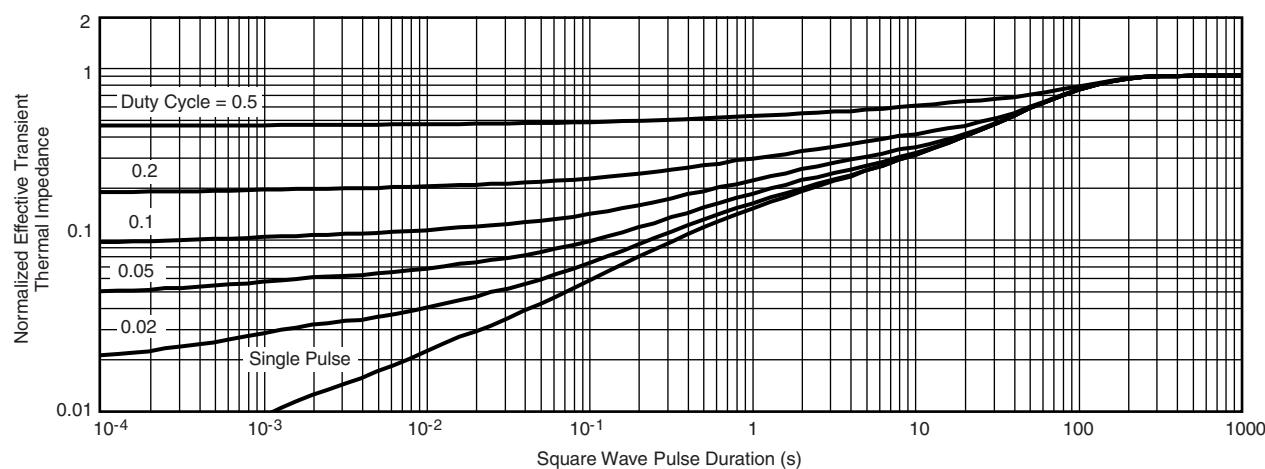
**Notes**

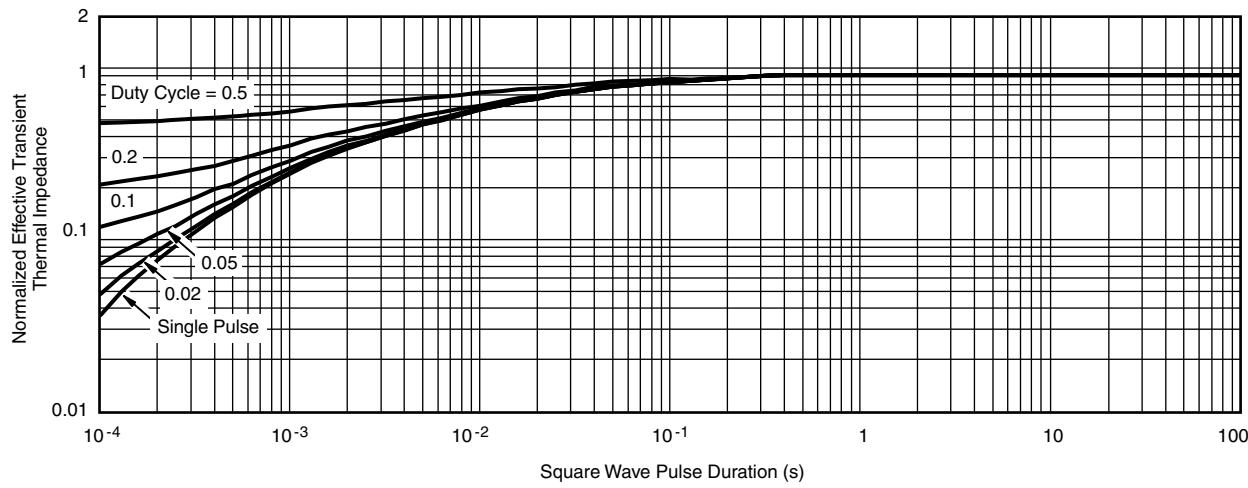
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)


**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**On-Resistance vs. Junction Temperature**

**THERMAL RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Safe Operating Area**

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

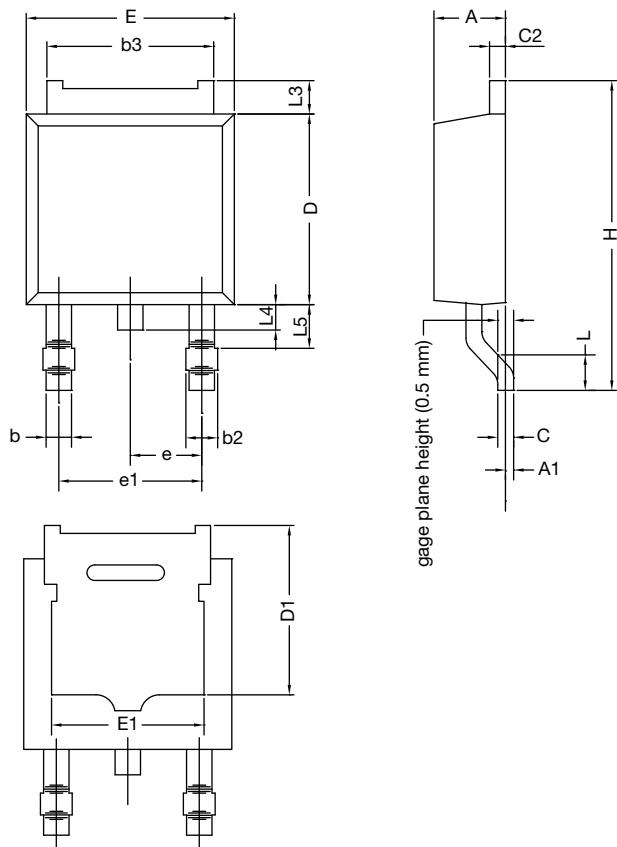
**THERMAL RATINGS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25^\circ\text{C}$ )

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?68880](http://www.vishay.com/ppg?68880).

### TO-252AA Case Outline

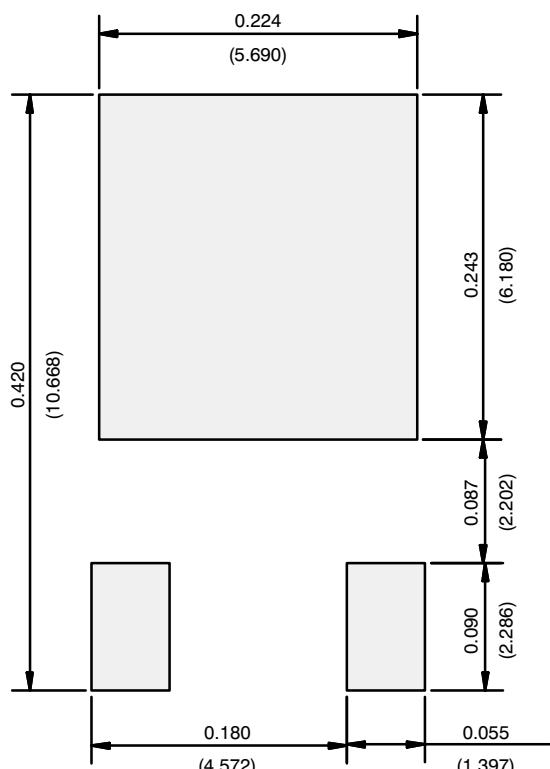


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0592-Rev. A, 02-Sep-13  
DWG: 6019

#### Note

- Dimension L3 is for reference only.

**RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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