BU-65539

MIL-STD-1553 BC/RT/MT INTERFACE CARD

DESCRIPTION

The BU-65539 provides full, intelligent interfacing between a dual redundant MIL-STD-1553B Data Bus and the IBM® PC AT Bus. Software controls the BU-65539's operation as either a 1553 Bus Controller (BC), Remote Terminal (RT), or Bus Monitor (MT).

The BU-65539 is packaged on a half-size IBM PC/AT printed circuit card, and features DDC's Miniature Advanced Communication Engine (Mini-ACE). As such, it includes dual transceiver and encoder/decoder, complete 1553B protocol, 64K words of shared RAM and memory management logic for all three modes.

Background Mode Operation prevents inadvertent access to the card during power-on self-test.

On-board Interrupt Mask and Interrupt Status Registers support flexible operation for both interrupt and polling applications.

The memory management scheme for RT mode provides an option for separation of broadcast data plus a circular buffer option for individual RT subaddresses to offload the PC host CPU.

Additional features include a wrap-around Built-In-Test, register programmable interrupt level, software programmable RT address selection and a free "C" software subroutine library. Its full compliance with MIL-STD-1553A and B makes it an excellent choice for real-time simulation, test, and system integration applications.

Make sure the next Card you purchase has...

DDC® on Board

FEATURES

- Half-Size IBM PC/AT ISA Compatible 16-Bit Interface Card
- 1553B Notice 2 Dual Redundant BC\RT\MT (STANAG 3838 Compliant)
- 64K x 16 Shared RAM
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Flexible RT Data Buffering
- Monitor Command Filtering
- Simultaneous RT/Monitor
- Flexible Interrupt Generation
- Software Support for DOS, Windows® 3.1, 9X, 2000 and Windows NT®

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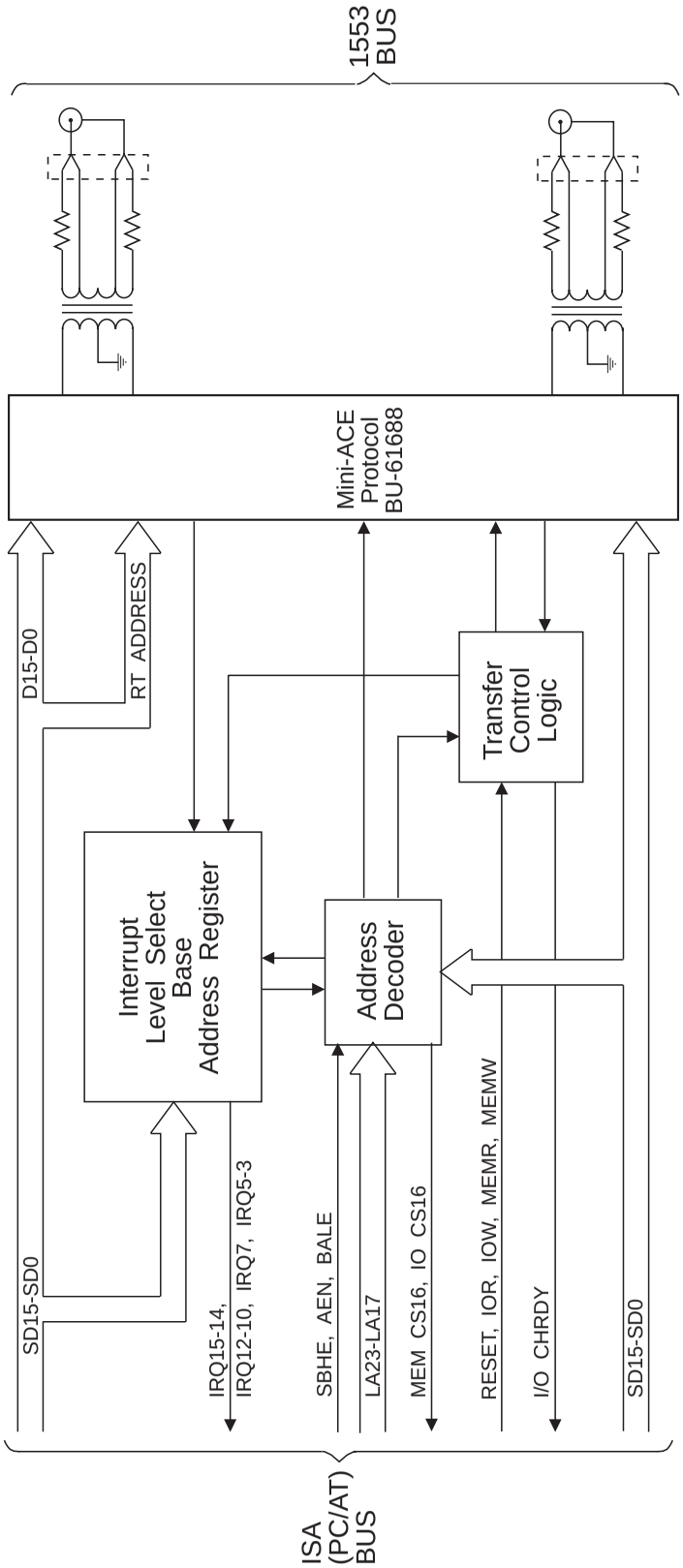


FIGURE 1. BU-65539 BLOCK DIAGRAM

TABLE 1. BU-65539 SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS				
+5 V Supply Voltage	-0.3		7.0	V
RECEIVER				
Threshold Voltage, Transformer Coupled, Measured on Stub			0.860	Vp-p
Common Mode Voltage			10	Vpeak
TRANSMITTER				
Differential Output Voltage				
• Direct Coupled Across 35 ohms, Measured on Bus	6	7	9	Vp-p
• Transformer Coupled, Measured on Stub	18	21	27	Vp-p
Output Noise, Differential (Direct Coupled)			10	mVp-p, diff
Output Offset Voltage, Direct Coupled Across 70 ohms	-250	150	250	mV
Rise/Fall Time	100		300	nsec
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
• + 5 V	4.5		5.5	V
Current Drain				
• + 5 V				
Idle		245	350	mA
25% Transmitter Duty Cycle		395	500	mA
50% Transmitter Duty Cycle		510	650	mA
100% Transmitter Duty Cycle		740	950	mA
POWER DISSIPATION				
Total PC Card				
• Idle		1.2	1.9	W
• 25%Transmitter Duty Cycle		2.0	2.8	W
• 50% Transmitter Duty Cycle		2.6	3.6	W
• 100% Transmitter Duty Cycle		3.7	5.2	W
1553 MESSAGE TIMING				
RT Response Timeout	4		7	µsec
Completion of CPU Write (BC Start-to Start of FIRST BC Message)		2.5		µsec
BC Intermessage Gap (See Note 1)		9.5		µsec
BC/RT/MT Response Timeout (See Note 2)				
• 18.5 nominal	17.5	18.5	19.5	µsec
• 22.5 nominal	21.5	22.5	23.5	µsec
• 50.5 nominal	49.5	50.5	51.5	µsec
• 128.0 nominal	127	129.5	131	µsec
Transmitter Watchdog Timeout		668		µsec
THERMAL				
Operating Temperature	0		55	°C
Storage Temperature	-20		65	°C
PHYSICAL CHARACTERISTICS				
Size	6.800 x 4.5 (172.72 x 114.3)			in (mm)
Weight	4.8 (136)			oz (gm)

Notes:
(1) Typical value for minimum intermessage gap time. Under software control, may be lengthened to (65,535 ms minus message time), in increments of 1 µs.
(2) Software programmable (4 options). Includes RT-to-RT Timeout (Mid-Parity of Transmit Command to Mid-Sync of Transmitting RT Status).

FUNCTIONAL OVERVIEW

GENERAL

The BU-65539 provides a user-friendly interface between the serial MIL-STD-1553B Notice 2 Bus and a PC/AT ISA bus. The operating modes of the BU-65539 are controlled through the use of 24 on-board registers, 1553 message traffic is stored and retrieved using the shared, memory mapped, on-board 64K words of RAM. The various registers control and operate the BU-65539. They include the Configuration Registers, Start/Reset Register, Time Tag Register, Interrupt Mask Register, Interrupt Status Register, Subaddress Control Word Register, Memory Base Address Register, and Control/RT Address Register. The Configuration Registers define the operating mode and memory management features. The Start/Reset Register provides various reset and BC/MT start functions. The Interrupt Mask Register enables desired interrupts, with the interrupt priority level being jumper programmable by the user. The cause of interrupts may be determined by a single READ operation, by means of the Interrupt Status Register. The Control/RT Address Register is used to program the RT address and miscellaneous functions. The Time Tag Register features programmable resolution and is used to time tag messages in BC or RT modes. The Memory Base Address Register supports a software programmable base memory address and controls the background mode operation.

The BU-65539's 64K x 16 of static RAM is shared by the PC host and the 1553 Bus with memory arbitration handled automatically by the BU-65539. The BU-65539 will withhold the wait signal (assert to logic “0”) to the PC backplane while a word is being transferred to or from the 1553 Bus. Since the memory arbitration is handled by simply stretching the handshake cycle, the wait state is transparent to the PC host processor's software. A maximum wait of 2.60 µs can occur.

In addition to storing the 1553 message data, the RAM implements the Stacks and Look-Up Tables required for the different modes of operation. For RT mode, there is a programmable option to separate broadcast message data from nonbroadcast data. This provides compliance to MIL-STD-1553B Notice 2. In addition, for RT mode, there is the choice of storing either a single message, a double buffer data structure or a circular buffer data structure. The size of the circular buffer is programmable up to 8192 words, on a Tx/Rx/Bcst-subaddress basis. A global double buffering mechanism is available to prevent partially updated information from being transferred to or from the 1553 Bus.

The BU-65539 supports programmable command illegalization for RT mode. This allows individual Command Words to be illegalized as a function of T/$\overline{R}$ bit, subaddress, and word count/mode code. Since the illegalization scheme is RAM based, it is inherently self-testable.

A Descriptor Stack is maintained for both BC, RT and MT modes. This records the status of each message, the time the message was transmitted or received, and contains either the received 1553 command and Data Block Pointer (in RT or MT mode) or the actual address of the 1553 message block (in BC mode). In RT mode, a Lookup Table is provided to define the addresses of the data blocks to be used when receiving or transmitting messages for the individual subaddresses.

The BU-65539 RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838 (including EFAbus), and the McAir A3818, A5232, and A5690 protocols.

The BU-65539 implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective message monitor.

SOFTWARE LIBRARY

The Software Library is provided free with the BU-65539 series boards. The library provides a set of subroutines written in "C". The subroutine library eliminates the need to write low-level code by providing a set of routines to initialize and control the board as well as to read and write data structures in real time. This frees the programmer from the low-level tasks of managing address maps and bit-level structures.

MEMORY MANAGEMENT

The BU-65539 incorporates complete memory management and processor interface logic. The software interface to the host processor is implemented by means of 24 on board registers plus 64K words of RAM. For all three modes, a stack area of RAM is maintained. In BC mode, the stack allows for the scheduling of multimessage frames. For all three modes, the stack provides a real-time chronology of all messages processed. In addition to the stack processing, the memory management logic performs storage, retrieval, and manipulation functions involving pointer and message data structures for all three modes.

The BU-65539 provides a number of programmable options for RT mode memory management. In compliance with MIL-STD-1553B Notice 2, received data from broadcast messages may be optionally separated from nonbroadcast received data. For each transmit, receive or broadcast subaddress, either a single-message data block or a variable-sized (128 to 8192 words) circular buffer may be allocated for data storage. In addition to helping ensure data consistency, the circular buffer feature provides a means of greatly reducing host processor overhead for bulk data transfer applications. End-of-message interrupts may be enabled either globally, following error messages, on a Tx/Rx/Bcst-subaddress basis, or when any particular Tx/Rx/Bcst-subaddress circular buffer reaches its lower boundary.

INTERRUPTS

The BU-65539 provides many programmable options for interrupt generation and handling. Interrupts may be generated on IRQ levels 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. The IRQ output from the BU-65539 is an active low pulse, 500 ns in duration, driven with an open-collector driver. The processor should detect the interrupt conditions on the rising edge of the pulse. This configuration will allow for multiple BU-65539 cards on the same interrupt level. **The Mini-ACE's level mode interrupt feature may not be used with the BU-65539.**

Individual events are enabled by the Interrupt Mask Register. The host processor may easily determine the cause of the interrupt by reading the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

The BU-65539 provides maskable interrupts and 15-bit Interrupt Status Register for end of message, end of BC message list, erroneous messages, Status Set (BC mode), Time Tag Register Rollover, RT Address Parity Error conditions, BC retry, data stack rollover, command stack rollover, transmitter watchdog timeout, or RAM parity error. The Interrupt Status Register allows the host processor to determine the cause of all interrupts by means of a single READ operation.

INTERNAL COMMAND ILLEGALIZATION

The BU-65539 offers the option to illegalize commands in RT mode. The illegalization architecture allows for any subset of the 4096 possible combinations of broadcast/own address, T/$\overline{R}$ bit, subaddress, and word count/mode code to be illegalized. The BU-65539 illegalization scheme is under software control of the host processor. As a result, it is inherently self-testable.

INTERNAL TIME TAG

The BU-65539 includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 µs per LSB. Another option allows the Time Tag Register to be incremented under software control. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both BC and RT modes.

Additional options are provided to clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command. Another option enables an interrupt request and a bit in the Interrupt Status Register to be set when the Time Tag Register rolls over from FFFF to 0000(hex). Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4-second time intervals, for 64 µs/LSB resolution, down to 131 ms intervals, for 2 µs/LSB resolution. Another programmable option for RT mode is for the Service Request Status Word bit to be automatically cleared following the BU-65539's response to a Transmit Vector Word mode command.

ADDRESSING, INTERNAL REGISTERS, MEMORY MANAGEMENT, AND INTERRUPTS

ADDRESSING THE BU-65539

The BU-65539 makes use of both I/O space and memory space on the ISA bus. The 64K words and the 24 internal ACE registers are memory mapped into the ISA memory space (refer to TABLE 2).

The BU-65539 contains a single 16-bit control register which is used to program the base address of the ACE's memory/registers and to select the card's interrupt level.

MEM23 through MEM16 are used to program the memory base address of the BU-65539's shared memory. These bits correspond to address bits LA23 through LA16 on the ISA backplane. The MEMENA bit is used to enable access to the shared memory. Programming MEMENA to logic "1" will enable the RAM allowing the host processor to access the shared memory/registers while programming a logic "0" will disable the shared memory/registers. The MEMENA bit defaults to logic "0" following a system reset (asserted from the ISA backplane on pin B02).

The IRQ3 through IRQ0 bits are used to select the BU-65539's interrupt level. Interrupt levels 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 may be selected. Selecting interrupt levels 0, 1, 2, 8, or 13 will disable interrupt capability (these levels are not implemented). The interrupt level defaults to "0" following a system reset (i.e. interrupts are disabled).

All pointers used on the BU-65539 are assumed to be word addresses, however the ISA address is normally defined using byte addressing. For example, to access the the Area A Stack Pointer at word address 0100 (hex), a byte address of 0200 (hex) must be used (i.e. the byte address is determined by multiplying the word address by two).

MEMORY ADDRESS MAP

The software interface of the BU-65539 to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus 64K X 16 of shared memory. Both the registers and the shared memory reside in the ISA memory space.

TABLE 2. MEMORY ADDRESS MAPPING

HEX ADDRESS	DESCRIPTION/ACCESSIBILITY
0000, 0001	1553 RAM word location 0000
•	•
•	•
•	•
04BE, 04BF	1553 RAM word location 025F
04C0, 04C1	Interrupt Mask Register (RD/WR)
04C2, 04C3	Configuration Register # 1 (RD/WR)
04C4, 04C5	Configuration Register # 2 (RD/WR)
04C6, 04C7	Start/Reset Register (WR)
04C8, 04C9	BC Control Word/RT Subaddress Control Word Register (RD/WR)
04CA, 04CB	Time Tag Register (RD/WR)
04CC, 04CD	Interrupt Status Register (RD)
04CE, 04CF	Configuration Register #3
04D0, 04D1	Configuration Register #4
04D2, 04D3	Configuration Register #5
04D4, 04D5	Data Stack Address Register (RD/WR)
04D6, 04D7	BC Frame Time Remaining Register (RD)*
04D8, 04D9	BC Time Remaining to Next Message Register (RD)*
04DA, 04DB	BC Frame Time*/RT Last Command/MT Trigger Word* Register (RD/WR)
04DC, 04DD	RT Status Word Register (RD)
04DE, 04DF	RT BIT Word Register (RD)
04E0, 04E1 • • • 04EE, 04EF	Test Mode Register 0 • • • Test Mode Register 7
04F0, 04F1 • • • 04FE, 04FF	Reserved • • • Reserved
0500, 0501 • • • FFFE, FFFF	64K x 16 Shared RAM (RD/WR) • • • 64K x 16 Shared RAM (RD/WR)

NOTE: All addresses shown above are assumed to be BYTE offsets.

BUS CONTROLLER (BC) ARCHITECTURE

The BC protocol of the BU-65539 implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/$\overline{R}$ bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The BU-65539's BC response timeout value is programmable with choices of 18, 22, 50, and 130 µs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

FIGURE 2 illustrates BC intermessage gap and frame timing. The BU-65539 may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled using a programmable BC frame timer. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 ms. In addition to BC frame time, message gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 µs.

BC MEMORY ORGANIZATION

It is important to note that the only fixed locations for the BU-65539 in the Standard BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 (hex) and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K shared RAM address space

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words).

Note, however, that this example assumes the disabling of the 256-word boundaries.

BC MEMORY MANAGEMENT

FIGURE 3 illustrates the BU-65539's BC memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for two sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the BU-65539's internal 1553 memory management logic may access only the various

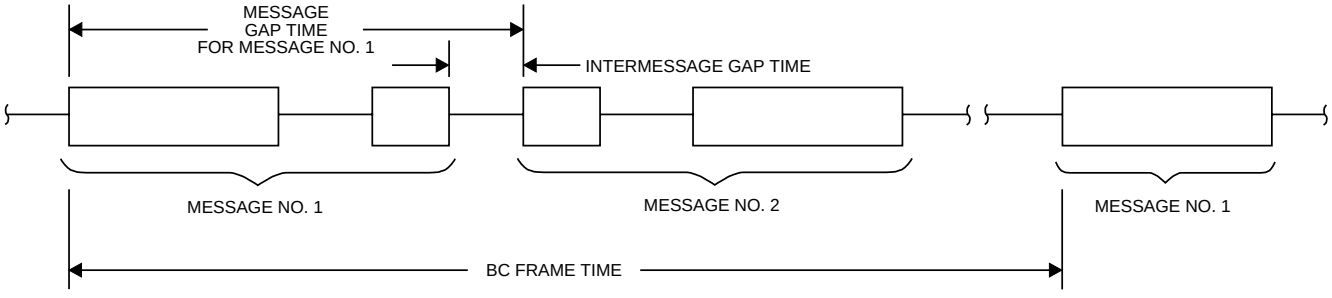


FIGURE 2. BC MESSAGE GAP AND FRAME TIMING

data structures within the “active” area. FIGURE 3 delineates the “active” and “inactive” areas by the nonshaded and shaded areas, respectively; however, at any point in time, **both the “active” and “nonactive” areas are accessible by the host processor.** In most applications, the host processor will access the “nonactive” area, while the 1553 bus processes the “active” area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

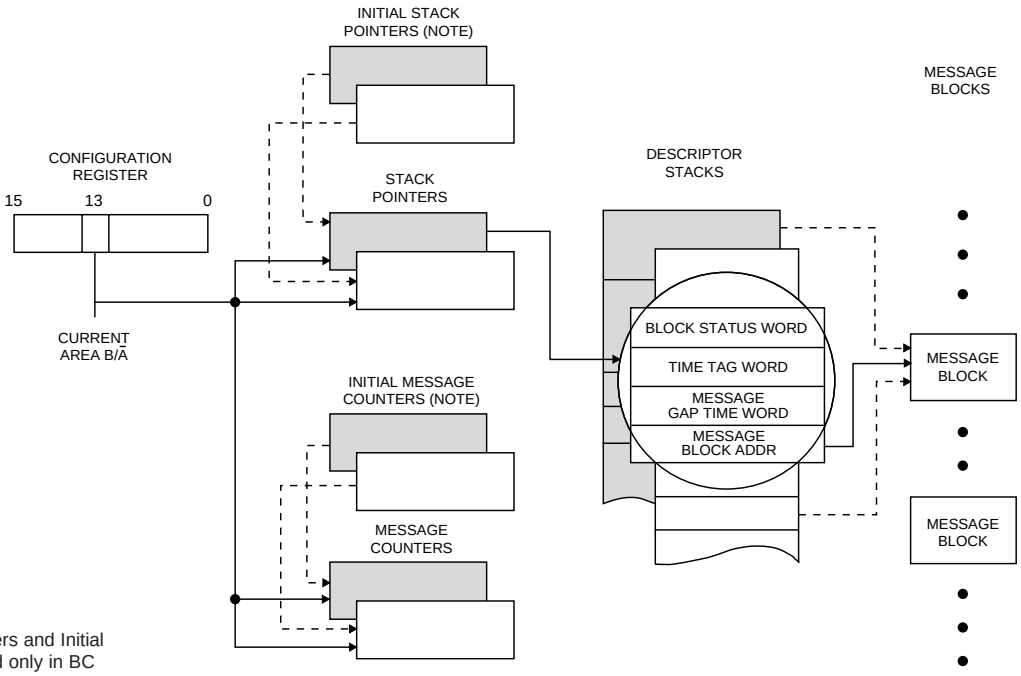
In the BC Frame Auto-Repeat mode, the Initial Stack Pointer and Initial Message Counter locations must be loaded by the host prior to the processing of the first frame. The single frame mode does not use these two locations.

The third and fourth words of the BC block descriptor are the Intermessage Gap Time and the Message Block Address for the respective message. These two memory locations must be written by the host processor prior to the start of message processing. Use of the Intermessage Gap Time is optional. The Block Address pointer specifies the starting location for each message block. The first word of each BC message block is the BC Control Word.

At the start and end of each message, the Block Status and Time Tag Words write to the message block descriptor in the stack. The Block Status Word includes indications of message in process or message completion, bus channel, Status Set, response timeout, retry count, Status address mismatch, loop test (on-line self-test) failure, and other error conditions. The 16-bit Time Tag Word will reflect the current contents of the internal Time Tag Register. This read/writable register, which operates for all three modes, has programmable resolution of from 2 to 64 µs/LSB. In addition, the Time Tag register may be clocked from an external source.

BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD

In BC mode, the BU-65539 supports all MIL-STD-1553 message formats. For each 1553 message format, the BU-65539 mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. **Note that for all of the message formats, the BC Control Word is located in the first location of the message block.**



Note: Initial Stack Pointers and Initial Message Counters used only in BC Frame Auto-Repeat Mode.

FIGURE 3. BC MODE MEMORY MANAGEMENT

The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, mask Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The Loopback Word is an on-line self-test feature. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

AUTOMATIC RETRIES

The BU-65539 BC can be set to implement automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options, retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur, the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows for masking (“care/don't care”) for the individual RT Status Word bits.

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the BU-65539 represents DDC's fifth generation implementation of a 1553 RT. One of the salient features of the ACE's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-65539 RT response time is 2 to 5 µs dead time (4 to 7 µs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the BU-65539 include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real time by the BU-65539 protocol logic.

The BU-65539 RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B compliance. The ACE RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the BU-65539 RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

RT MEMORY ORGANIZATION

As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the ACE address space designated as fixed locations. All RT modes of operation require the Area A (and may use Area B) Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

RT MEMORY MANAGEMENT

One of the salient features of the ACE series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the BU-65539 provides an option to separate data received from broadcast messages from nonbroadcast received data.

Besides supporting a global double buffering scheme (as in BC mode), the ACE RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis. The 128-word tables include 32-word tables for transmit message pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary. For most applications, the subaddress tables provide more flexible buffering than the global scheme and current Area B tables are not used.

The fourth section of each of the RT Lookup Tables stores the 32 Subaddress Control Words. The individual Subaddress Control Words may be used to select the RT memory management

option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.

When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word. The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

SINGLE MESSAGE MODE

FIGURE 4 illustrates the RT Single Message memory management scheme. When operating the BU-65539 in its "AIM-HY" (default) mode, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). FIGURES 4, 5, and 6 delineate the "active" and "nonactive" areas by the non-shaded and shaded areas, respectively.

As shown, the ACE stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/$\overline{R}$ bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The BU-65539 RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

If a particular subaddress is set to the Single Message mode, there is a possibility that the contents of the receive data block may be overwritten or that the transmit block may be overread. In the Single Message mode it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective lookup table pointer. The Circular Buffering mode, on the other hand, makes use of a buffering structure which automatically updates.

To implement a data wraparound subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wraparound subaddress. Notice 2 recommends subaddress 30 as the wraparound subaddress.

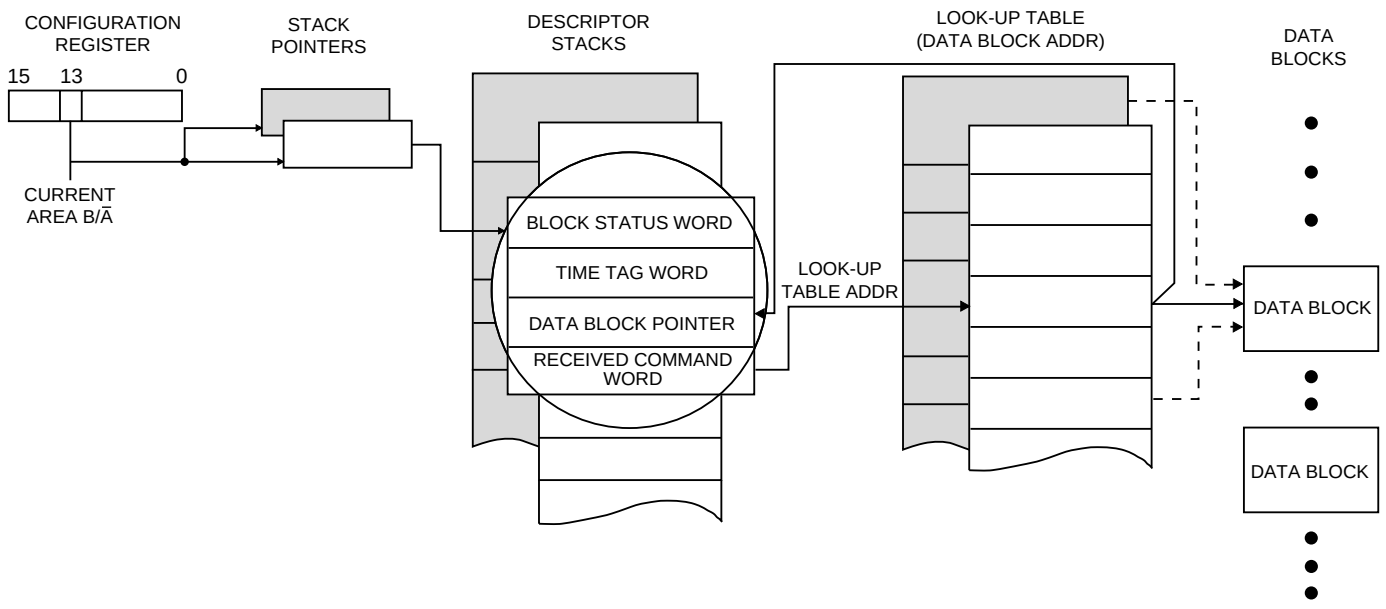


FIGURE 4. RT MEMORY MANAGEMENT: SINGLE MESSAGE MODE

CIRCULAR BUFFER MODE

FIGURE 5 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even powers of 2) by the respective Subaddress Control Word. As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the ACE stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The ACE transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/RX(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the BU-65539 address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 5 shows, **Implementing Bulk Data Transfers**.

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress. The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, **including errors and retries**, is transparent to the RT's host processor.

By strategically initializing the subaddresses Lookup Table pointer prior to the start of the bulk transfer, the BU-65539 may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

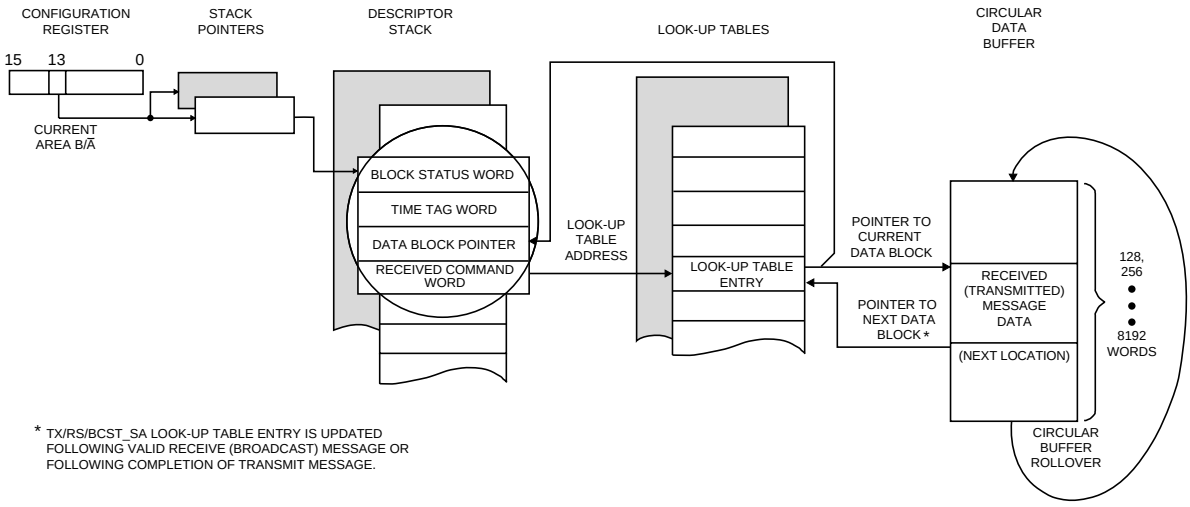


FIGURE 5. RT MEMORY MANAGEMENT: CIRCULAR BUFFER MODE

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the BU-65539 RT offers a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. FIGURE 6 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer modes, the Double Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.

At a given point in time, one of the two blocks will be designated as the “active” 1553 data block while the other will be designated as the “inactive” block. The Data Words from the next receive message to that subaddress will be stored in the “active” block. Upon completion of the message, provided that the message was valid and Subaddress Double Buffering is enabled, the BU-65539 will automatically switch the “active” and “inactive” blocks for the respective subaddress. The ACE accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress Lookup Table pointer. This points to the current “active” Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the “inactive” Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the “inactive” (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

RT INTERRUPTS

As in BC mode, the BU-65539 RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

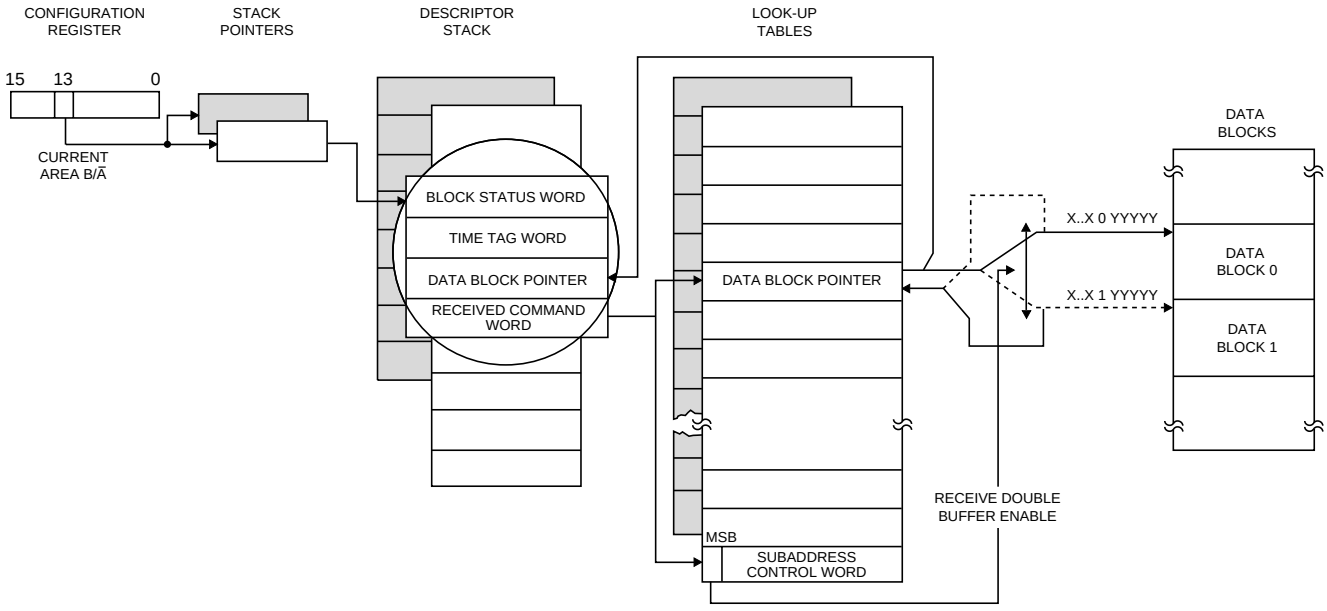


FIGURE 6. RT MEMORY MANAGEMENT: SUBADDRESS DOUBLE BUFFERING MODE

DESCRIPTOR STACK

At the beginning and end of each message, the BU-65539 RT stores a 4-word message descriptor in the active area stack. The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 4, 5, and 6 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions.

As in BC mode, the Time Tag Word stores the current contents of the BU-65539's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2, 4, 8, 16, 32, and 64 µs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The ACE stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks. The ACE stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the BU-65539 RT provides a software controllable means for setting the Busy Status Word bit as a function of subaddress. By a Busy Lookup Table in the BU-65539 address space, it is possible to set the Busy bit based on command broadcast/own address, T/$\overline{R}$ bit, and subaddress. Another programmable option, allows received Data Words to be either stored or not stored for messages, when the Busy bit is set.

OTHER RT FUNCTIONS

The BU-65539 allows the hardwired RT Address to be read by the host processor. Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test. Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The BU-65539 provides three bus monitor (MT) modes:

(1) The “AIM-HY” (default) or “AIM-HY'er” Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor. Besides providing monitor filtering based on RT Address, T/$\overline{R}$ bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software. The development of such software tends to be a tedious task. Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the BU-65539 monitors both 1553 buses. After initializing the Word Monitor and putting it on-line the BU-65539 stores all Command, Status, and Data Words received from both buses. For each word received from either bus, the BU-65539 stores a pair of words in RAM. The first word is the 16 bits of data from the received word. The second word is the Monitor Identification (ID), or “Tag” word. The ID Word contains information relating to bus channel, sync type, word validity, and inter-word time gaps. The BU-65539 stores data and ID words in a circular buffer in the shared RAM address space.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode. The BU-65539 stores the value of the 16-bit Trigger Word in the MT Trigger Word Register. The contents of this register represent the value of the Trigger Command Word. The BU-65539 has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The BU-65539 Selective Message Monitor provides features to greatly reduce the software and processing burden of the host CPU. The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/$\overline{R}$ bit, and Subaddress fields of received 1553 Command Words. The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words. The Selective Message Monitor maintains two stacks in the BU-65539 RAM: a Command Stack and a Data Stack.

SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor. The RT/Monitor mode provides complete Remote

Terminal (RT) operation for the BU-65539's strapped RT address and bus monitor capability for the other 30 nonbroadcast RT addresses. This allows the BU-65539 to simultaneously operate as a full function RT and “snoop” on all or a subset of the bus activity involving the other RTs on a bus. This type of operation is sometimes needed to implement a backup bus controller. The combined RT/Selective Monitor maintains three stack areas in the BU-65539 address space: an RT command stack, a Monitor command stack, and a Monitor Data Stack. The pointers for the various stacks have fixed locations on the BU-65539 address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

This mode of operation defines several fixed locations in the RAM. These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode. The fixed memory map consists of two Monitor Command Stack Pointers (location 102H and 106H), two Monitor Data Stack Pointers (locations 103H and 107H), and a Selective Message Monitor Lookup Table (0280-02FFH) based on RT Address, T/$\overline{R}$, and subaddress. Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 2K words.

Refer to FIGURE 7 for an illustration of the Selective Message Monitor operation. Upon receipt of a valid Command Word, the BU-65539 will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command. If disabled, the BU-65539 will ignore (and not store) the current message; if enabled, the BU-65539 will create an entry in the Monitor Command Stack at the address location referenced by the Monitor Command Stack Pointer.

Similar to RT mode, the ACE stores a Block Status Word, 16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word. The ACE writes the Block Status and Time Tag Words at both the start and end of the message. The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions. The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message. The BU-65539 will then proceed to store the subsequent words from the message (possible second

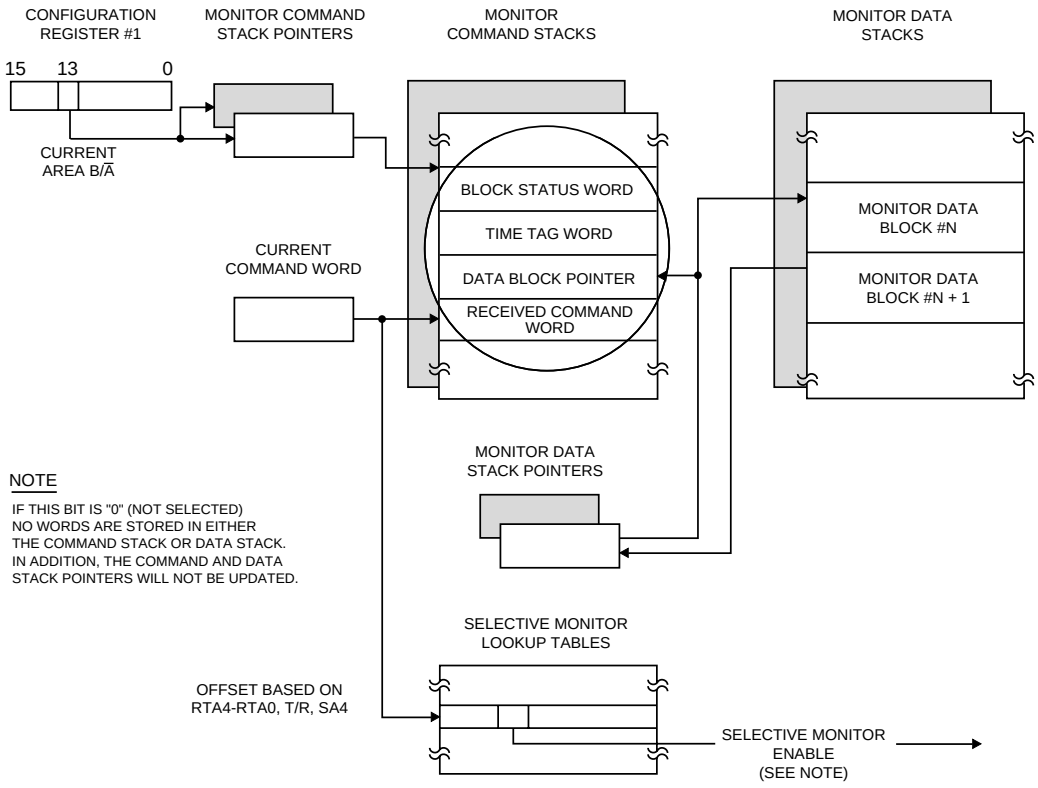


FIGURE 7. SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

Command Word, Data Word(s), Status Word(s)) into consecutive locations in the Monitor Data Stack.

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K words. The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions. In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

INTERFACE TO MIL-STD-1553 BUS

FIGURE 8 illustrates the interface from the BU-65539 to a 1553 bus for either transformer (long stub) or direct (short stub) coupling, plus the peak-to-peak voltage levels that appear at various points when transmitting.

Both coupling configurations require the use of an isolation transformer that interfaces directly to the PC Card. For the transformer (long stub) coupling configuration, a second transformer, referred to as a coupling transformer is required. In accordance with MIL-STD-1553B, the turns ratio of the coupling transformer is 1.0 to 1.4.

Both transformer and direct coupling configurations require an isolation resistor to be placed in series with each leg of the transformer connecting to the 1553 bus; this protects the bus against short circuit conditions in the transformers, stubs, or terminal components.

Jumpers allow for either transformer or direct coupling.

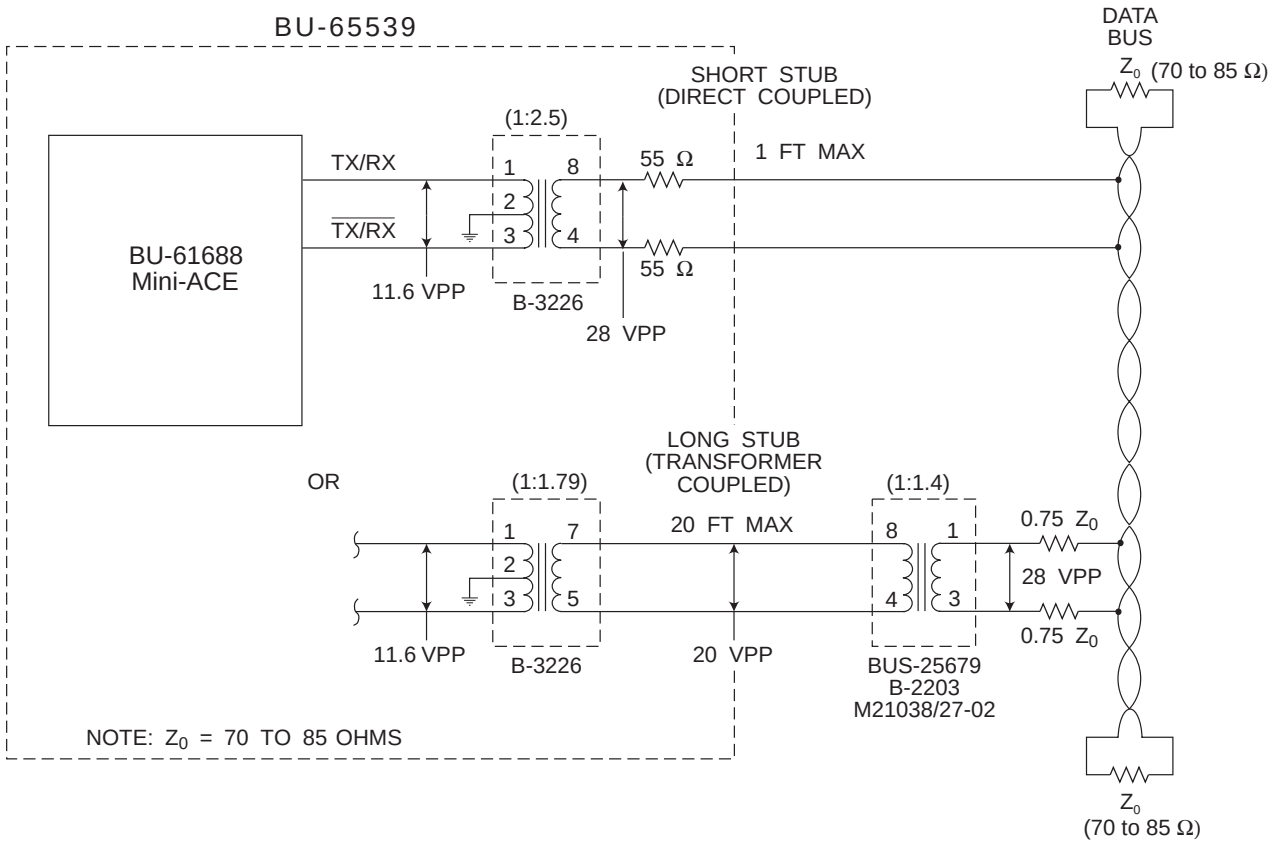


FIGURE 8. BU-65539 INTERFACE TO A MIL-STD-1553 BUS

I/O BASE ADDRESS

The BU-65539 contains a single jumper block “JP1” (see FIGURE 9) used to specify the I/O mapped base address of one 16-bit control register. The memory mapped base address of the 64K words of shared RAM and the hardware interrupt levels are software programmable via the BU-65539’s control register.

The I/O base address jumper block is used to specify the I/O mapped base address of one 16-bit register. The block contains nine individual jumpers, which are not numbered. The bottom is the edge closest to the ISA card edge connector. Each jumper can be placed on the pins, (ON selects ground “0”) or off the pins, (OFF selects 5 Volts “1”) to configure the card for the correct I/O base address. Jumper “JP1” is shown configured for 360 (hex), which is the default I/O base address for the BU-65539 card.

BUS COUPLING MODE

The BU-65539 can be interfaced to a MIL-STD-1553 bus in either Direct or Transformer coupled mode. The modes are configured via two jumper blocks labled JP2 and JP3 on the card (see FIGURE 11).

These jumpers are NOT numbered. The ground jumpers are located at the bottom of JP2 and JP3. The bottom is the edge closest to the ISA card edge connector. The diagram shows the jumpers configured for “Transformer Coupled” output/grounded TRIAX connector bodies and card edge frame.

The board edge bracket (and TRIAX connector bodies) can be directly connected to the DC return of the board if desired. This connection is exercised through placement of a jumper plug on either JP2 or JP3.

The bracket is “floating” from the board artwork and not exercising this option leaves the bracket making chassis ground connection through the PC card cage frame.

JP2: 1553 Channel B coupling option. Install jumpers on second and third sets of pins for transformer coupled connections or on first and forth sets of pins for direct (Series Resistors) coupled connections. The last set of jumpers is used to connect the shield on the 1553 cable (and the rear mounting bracket of the board) to the power supply ground on the card.

JP3: 1553 Channel A Coupling options. Same as JP2 but applies to Channel A.

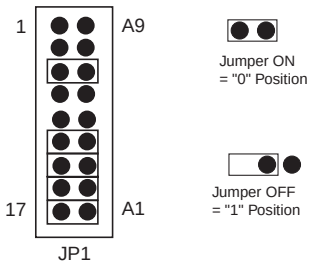


FIGURE 9. I/O BASE ADDRESS JUMPER BLOCK

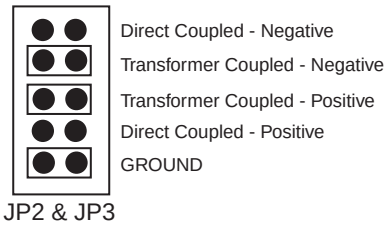
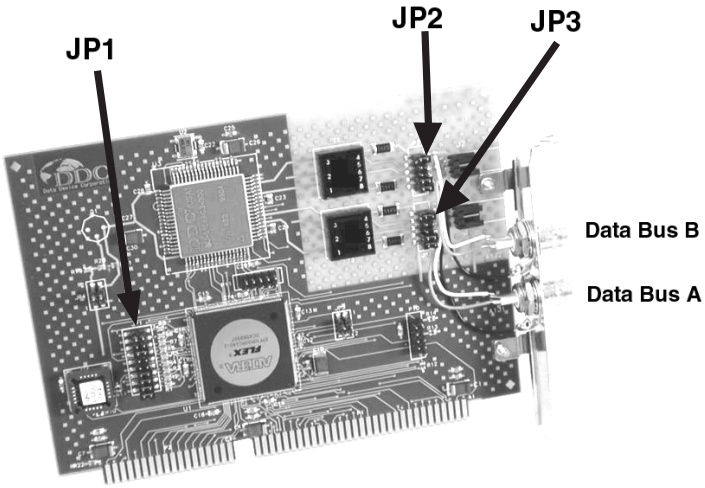


FIGURE 10. BUS COUPLING MODE



Note: All other jumper blocks on the card are for DDC use ONLY, and must not be altered.

FIGURE 11. BU-65539 JUMPER BLOCKS

ORDERING INFORMATION

BU-65539M2-300

└── Transceiver:
2 = Trapezoidal Transceiver (1553)

Note: The above product contains tin-lead solder.

Available Software:
BUS-69080S0 - 16-bit Runtime Library (DOS)
BUS-69081S0 - 16-Bit ACE Menu (Windows 3.x)
BUS-69082S0 - 32-Bit RTL and Drivers (Windows 95/98)
BUS-69083S0 - 32-Bit RTL and Drivers (Windows NT, Windows 2000)
BUS-69084S0 - 32-Bit ACE Menu (Windows 95/98)
BUS-69085S0 - 32-Bit ACE Menu (Windows NT, Windows 2000)

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