SC1176/SC1176A
Dual Synchronous Voltage Mode Controller with Current Sharing Circuitry

POWER MANAGEMENT

Description

The SC1176 is a versatile 2 phase, synchronous, voltage mode PWM controller that may be used in two distinct ways. First, the SC1176 is ideal for applications where point of use output power exceeds any single input power budget. Alternatively, the SC1176 can be used as a dual switcher. The SC1176 features a temperature compensated voltage reference, over current protection with 50% fold-back and internal level-shifted, high-side drive circuitry.

In current sharing configuration, the SC1176 can produce a single output voltage from two separate voltage sources (which can be different voltage levels) while maintaining current sharing between the channels. Current sharing is programmable to allow loading each input supply as required by the application.

In dual switcher configuration, two feedback paths are provided for independent control of the separate outputs. The device will provide a regulated output from flexibly configured inputs (3.3V, 5V, 12V), provided 5V is present for V_{CC}. The two switchers are 180° out of phase to minimize input and output ripple.

The SC1176A has the phases of the Master and the Slave inverted.

It offers a different pattern for ripple cancellation and prevents phase fold back during current limit.

The two chips are pin compatible.

Features

- 300kHz fixed frequency operation
- Soft Start and Enable function
- Power Good output provided
- Over current protection with 50% fold-back
- Phase-shifted switchers minimize ripple
- High efficiency operation, >90%
- Programmable output(s) as low as .9V
- Industrial temperature range
- SOIC-20 or TSSOP-20 pin Lead free package. This product is fully WEEE and RoHS compliant

Two Phase, Current Sharing Controller

- Flexible, same or separate V_{IN}
- Programmable current sharing
- Combined current limit with fold-back
- 2 phases operating opposed for ripple reduction
- Thermal distribution via multi-phase output

Two Independent PWM Controllers

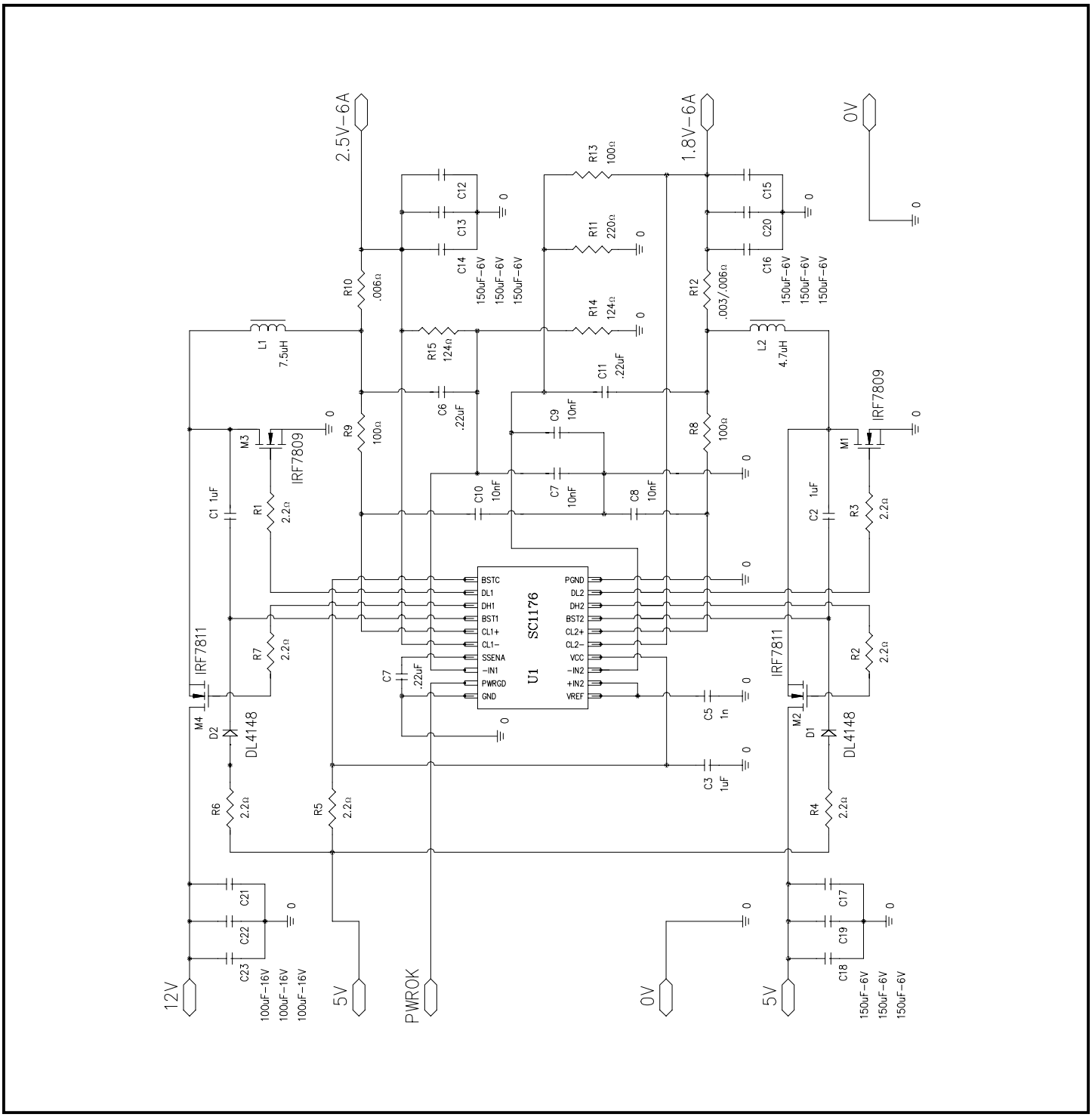
- Flexible, same or separate V_{IN}
- Independent control for each channel
- Independent and separate current limit
- 2 phases operating opposed for ripple reduction (if same V_{IN} used)

Applications

- Graphics cards
- DDR Memory
- Peripheral add-in card
- SSTL Termination
- Dual-Phase power supply
- Power supplies requiring two outputs

Typical Application Circuit

2 Channels with Current Sharing



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Limits	Units
V_{CC} to GND	V_{IN}	-0.3 to 15	V
PGND to GND		± 1	V
BST to GND		-0.3 to 26	V
Thermal Resistance Junction to Case SOIC TSSOP	θ_{JC}	 24 27	°C/W
Thermal Resistance Junction to Ambient SOIC TSSOP	θ_{JA}	 65 85	°C/W
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature Range	T_J	0 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, 0mV < (CS(+) - (CS(-)) < 60mV , T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	I_O = 2A(1), V_{OUT} set to 2.75V	2.65	2.75	2.85	V
Supply Voltage	V_{CC}	4.2		15	V
Supply Current	V_{CC} = 5.0		15		mA
Reference Voltage	I_{REF} = 0µA	0.89	0.9	0.91	V
Reference Voltage Line Regulation	5V < V_{CC} < 15V			0.5	%
Reference Voltage Load Regulation	I_{REF} = 0µA to 30µA			-12	mV
Output Line Regulation	5V < V_{IN} < 15V			0.5	%
Output Load Regulation	I_O = 0.3A to 15A (1)		1		%
Gain (A_{OL})	V_{OSENSE} to V_O		35		dB
Current Limit Voltage		60	70	80	mV
Oscillator Frequency		270	300	330	kHz
Oscillator Max Duty Cycle		90	95		%
DH Sink Current	DH - PGND = 3.0V	1.3			A
DH Sink Current	DH - PGND = 2.0V	0.85			A
DH Source Current	BSTH - DH = 3.5V	1.3			A
DH Source Current	BSTH - DH = 2.5V	0.85			A

Electrical Characteristics (Cont.)

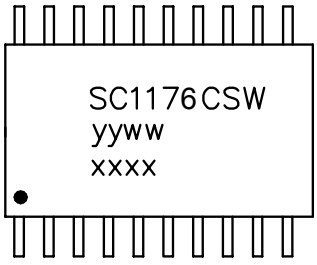
Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, 0mV < (CS(+) - (CS(-)) < 60mV , T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DL Sink Current	DL - PGNG = 3.0V	1.3			A
DL Sink Current	DL - PGND = 2.0V	0.85			A
DL Source Current	BSTL - DL = 3.5V	1.3			A
DL Source Current	BSTL - DL = 2.5V	0.85			A
Dead Time	Note 5	50	100	150	ns
Soft Start Charge Current (2)			25		µA
Soft Start Enable	0% duty cycle		1.4		V
Soft Start End	100% duty cycle		2.5		V
Soft Start Transition(2)	Synchronous mode		3.3		V
Power Good Window(3)			+10		$\%V_{OUT}$
Fold Back Current	V_{OUT} = 0V		50%		I_{LIM}
Fold Back Voltage Knee	$I = I_{LIM}$	0.9		V_{OUT}	V
Input Bias Current	-IN1, +IN2, -IN2			1	µA
BSTH to DH Leakage	BSTH - DH = 5V			10	µA
DH to PGND Leakage	DH - PGND = 5V			10	µA
BSTL to DL Leakage	BSTL - DL = 5V			10	µA
DL to PGND	DL - PGND = 5V			10	µA

Notes:
(1) Specification refers to application circuit.
(2) The soft start pin sources 25µA to an external capacitor. The converter operates in synchronous mode above the soft start transition threshold and in asynchronous mode below it.
(3) Power good is an open collector pulled low when the output voltage is outside the ±10% window.
(4) This device is ESD sensitive. Use of standard ESD handling precautions is required.
(5) 200ns maximum at 75°.

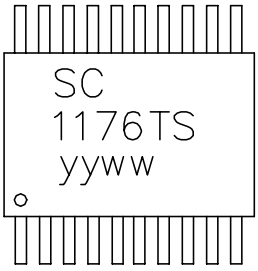
Marking Information

(SOIC-20)



TOP
yyww = Date Code (Example: 9908)
xxxx = Semtech Lot # (Example: 90101)

(TSSOP-20)



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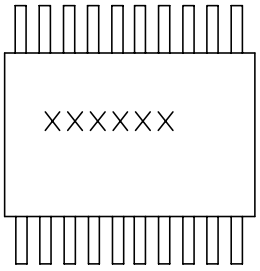
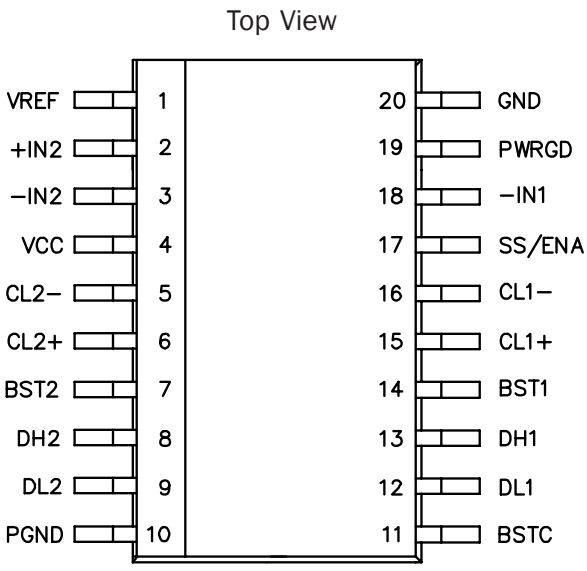


BOTTOM

nnnn = Part Number (Example: 1471)
yyww = Date Code (Example: 0012)
xxxxxx = Semtech Lot # (Example: P94A01)

Pin Configuration



(SOIC-20 and TSSOP-20 Pin)

Ordering Information

Device[1]	Package[2]
SC1176CSWTR	SOIC-20
SC1176CSWTRT	
SC1176ASWTR	
SC1176ASWTRT	
SC1176TSTR	TSSOP-20
SC1176TSTRT	
SC1176ATSTR	
SC1176EVB-1	Current Share Version Evaluation Board
SC1176-2EVB-2	Dual Channel Version Evaluation

Notes:
(1) Only available in tape and reel packaging. A reel contains 1000 (SOIC) or 2500 (TSSOP) devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

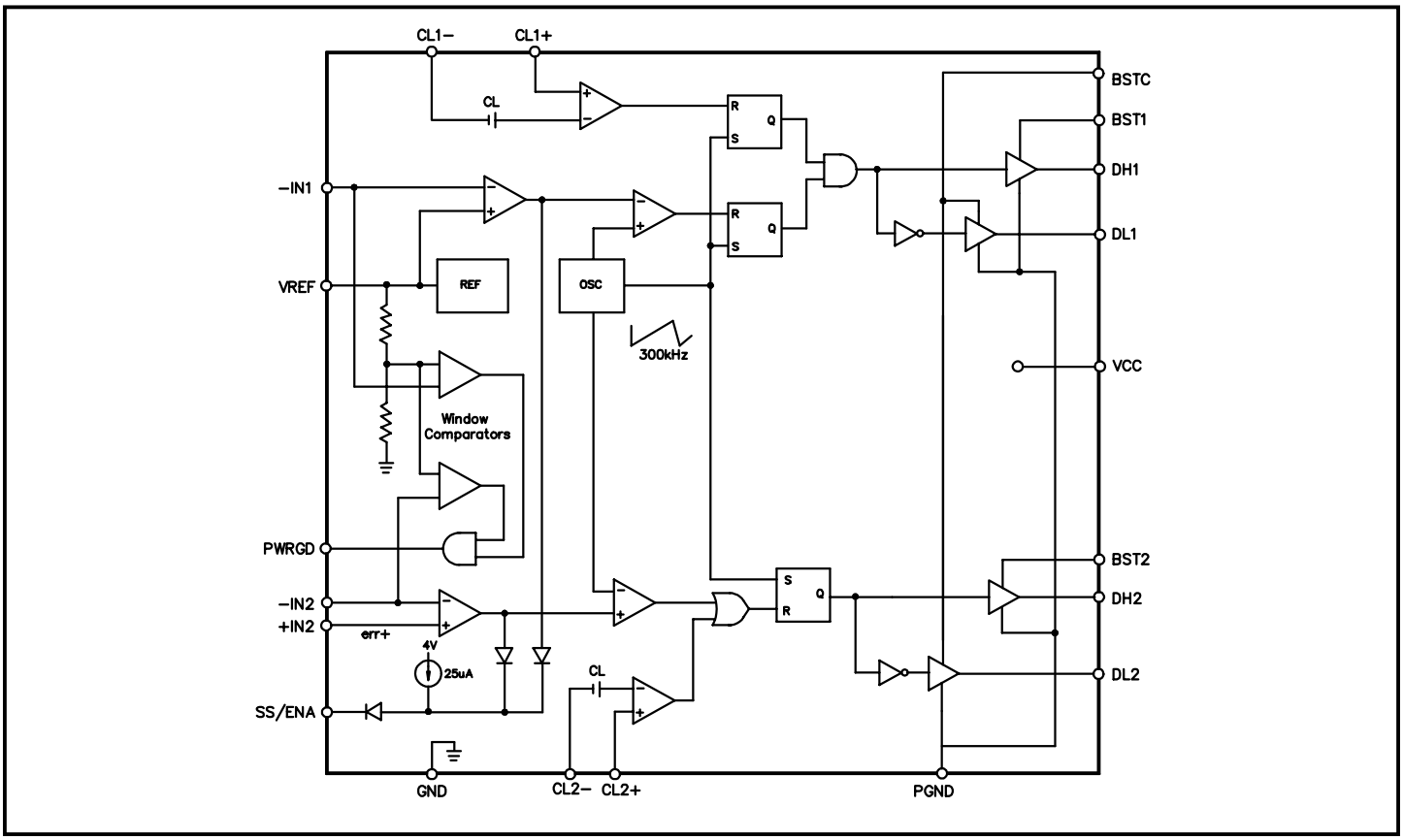
Pin Descriptions

EXPANDED PIN DESCRIPTION

Pin 1: (VREF)
Internal .9V reference
Connected to the + input of the master channel error amplifier.
Pin 2: (+IN2)
+ Input of slave channel error amplifier.
Connected to .9V reference (Pin 1) for
2 independent channel configuration.
Pin 3, 18: (-IN2, -IN1)
- Inputs of close loop error amplifiers.
Works as a feedback inputs (For both modes).
Pin 4: (VCC)
VCC chip supply voltage.
15V maximum, 15mA typical.
Needs a 1µF ceramic multilayer decoupling capacitor to GND (Pin 20).
Pin 5, 6,15, 16: (CL2-, CL2+, CL1+, CL1-)
Pins (-) and (+) of the current limit amplifiers for both channels.
Connected to output current sense resistors. Compares that sense voltage to internal 75mV reference.
Needs RC filter for noise rejection.
Pin 7, 14: (BST2, BST1)
BST signal. Supply for high side driver.
Can be connected to a high enough voltage source.
Usually connected to bootstrap circuit.

Pin 8, 13: (DH2, DH1)
DH signal (Drive High).
Gate drive for top MOSFETs.
Requires a small serie resistor.
Pin 9, 12: (DL2, DL1)
DL signal (Drive Low).
Gate drive for bottom MOSFETs.
Requires a small serie resistor.
Pin 10: (PGND)
Power GND. Return of gate drive currents.
Pin 11: (BSTC)
Supply for bottom MOSFETs gate drive.
Pin 17: (SS/ENA)
Soft start pin. Internal current source connected to external capacitor.
Inhibits he chip if pulled down.
Pin 19: (PWRGD)
Power good signal.
Open collector signal .
Turns to 0 if output voltage is outside the power good window.
Pin 20: (GND)
Analog GND.
Return of analog signals and bias of chip.

Block Diagram



NOTES

(1) Block 1 (top) is the Master and Block 2 (bottom) is the Slave in current sharing configuration.

(2) For independent operation there is no Master or Slave.

Applications Information - Theory of Operation

Main Loop(s)

The SC1176 is a dual, voltage mode synchronous Buck controller, the two separate channels are identical and share only IC supply pins (Vcc and GND), output driver ground (PGND) and pre-driver supply voltage (BSTC). They also share a common oscillator generating a sawtooth waveform for channel 1 and an inverted sawtooth for channel 2. Each channel has its own current limit comparator. Channel 1 has the positive input of the error amplifier internally connected to Vref. Channel 2 has both inputs of the error amplifier uncommitted and available externally. This allows the SC1176 to operate in two distinct modes.

a) Two independent channels with either common or different input voltages and different output voltages. The two channels each have their own voltage feedback path from their own output. In this mode, the positive input of error amplifier 2 is connected externally to Vref. If the application uses a common input voltage, the sawtooth phase shift between the channels provides some measure of input ripple current cancellation.

b) Two channels operating in current sharing mode with common output voltage and either common input voltage or different input voltages. In this mode, channel 1 operates as a voltage mode Buck controller, as before, but error amp 2 monitors and amplifies the difference in voltage across the output current sense resistors of channel 1 and channel 2 (Master and Slave) and adjusts the Slave duty cycle to match output currents. Because of finite gain and offsets in the loop, the resistor ratio for perfect current match-

ing is not 1:1. The Master and Slave channels still have their own current limits, identical to the independent channel case.

Power Good

The controller provides a power good signal. This is an open collector output, which is pulled low if the output voltage is outside of the power good window.

Soft Start/Enable

The Soft Start/Enable (SS/ENA) pin serves several functions. If held below the Soft Start Enable threshold, both channels are inhibited. DH1 and DH2 will be low, turning off the top FETs. Between the Soft Start Enable threshold and the Soft Start End threshold, the duty cycle is allowed to increase. At the Soft Start End threshold, maximum duty cycle is reached. In practical applications the error amplifier will be controlling the duty cycle before the Soft Start End threshold is reached. To avoid boost problems during startup in current share mode, both channels start up in asynchronous mode, and the bottom FET body diode is used for recirculating current during the FET off time. When the SS/ENA pin reaches the Soft Start Transition threshold, the channels begin operating in synchronous mode for improved efficiency. The soft start pin sources approximately 25uA and soft start timing can be set by selection of an appropriate soft start capacitor value.

SENSE RESISTOR SELECTION

Current Sharing Mode

Calculation of the three programming resistors to achieve sharing.
Three resistors will determine the current sharing load line.
First the offset resistor will ensure that the load line crosses the origin (0 Amp on each channel) for sharing at light current. A pull up resistor from the 5V bias (V_{CC} of the chip) will be used. For low duty cycle on the slave channel (below 50%), the pull up will be on pin 3. For high duty cycle on the slave channel (above 50%), the pull up will be on pin 2.

The formula is:

$$R_{pull-up}\ (K\Omega) = 2.1\ X\ \frac{5 - V_{OUT}}{.5 - \frac{V_{OUT} + .1}{V_{SLAVE}}}$$

100Ω being the value of the resistors connecting the pins 2 and 3 to the two output sense resistors.

.1 V is an estimated voltage drop across the MOSFETs.

Positive values go to pin 3, negative to pin 2.

A +20K will be a 20K on pin 3.
A -20K will be a 20K on pin 2.

Now that the offset resistor has been fixed, we need to set up the maximum current for each channel.

Selection of R_{SENSE} 1 for the master channel: (in m ohm)

R_{SENSE} 1 = 72mV / I max master

Selection of R_{SENSE} 2 for the slave channel: (in m ohm)

R_{SENSE} 2 = 72mV / I max slave

The errors will be minimized if the power components have been sized proportionately to the maximum currents.

Independent Channels

Calculation of the two current limiting resistors.
There is no need for an offset resistor in the independent channels mode, only the two sense resistors are used:

Selection of R_{SENSE} 1 for the channel 1: (in m ohm)

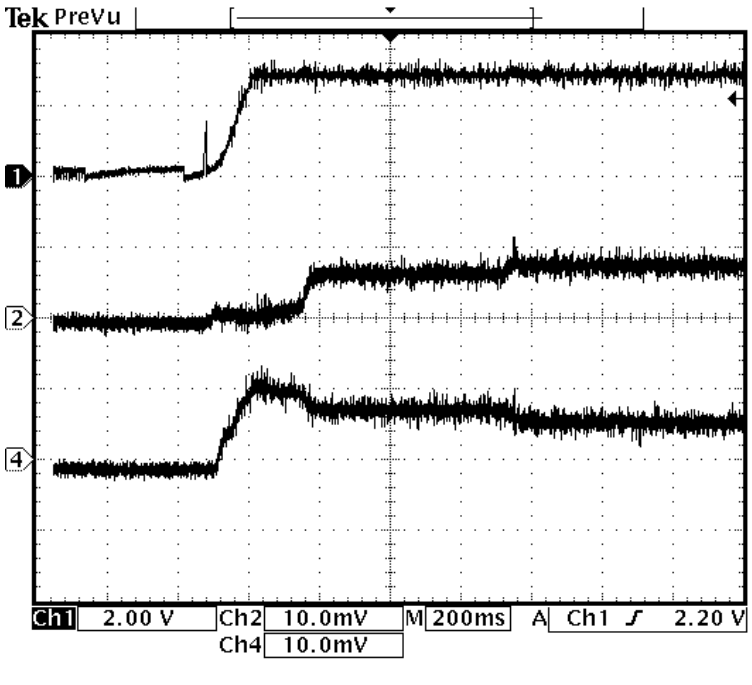
R_{SENSE} 1 = 72mV / I max ch 1

Selection of R_{SENSE} 2 for the channel 2: (in m ohm)

R_{SENSE} 1 = 72mV / I max ch 2

Typical Characteristics - 2 Channels with Current Sharing

Figure 1: V_{OUT} vs $I_{IN(5V)}$ and $I_{IN(12V)}$ with V_{CC} applied and 4A load. Soft start capacitor = 10nF.



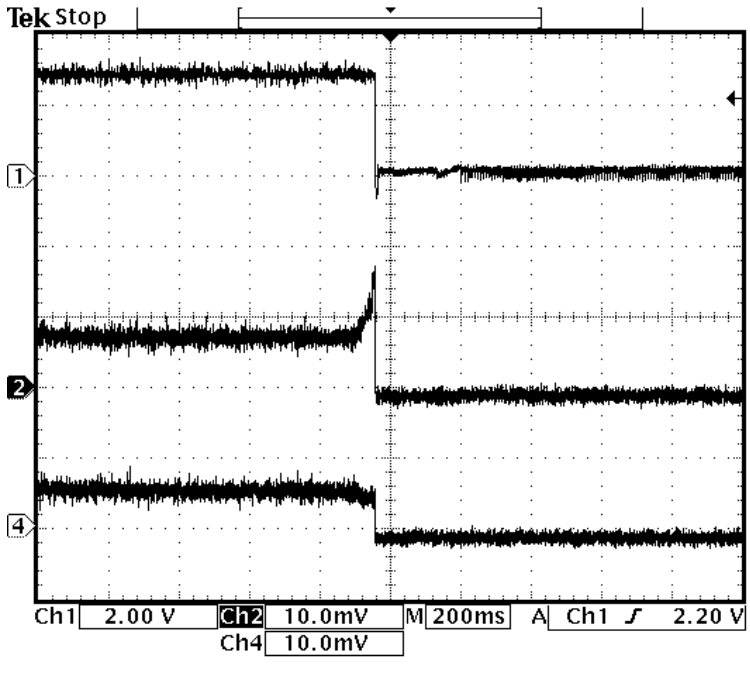
Ch1: V_{OUT}

Ch2: $I_{IN(5V)}$ (1A/Div)

Ch4: $I_{IN(12V)}$ (1A/Div)

I_{OUT}: 4.004 Amps

Figure 2: V_{OUT} vs $I_{IN(5V)}$ and $I_{IN(12V)}$ with V_{CC} removed and 4A load. Soft start capacitor = 10nF.



Ch1: V_{OUT}

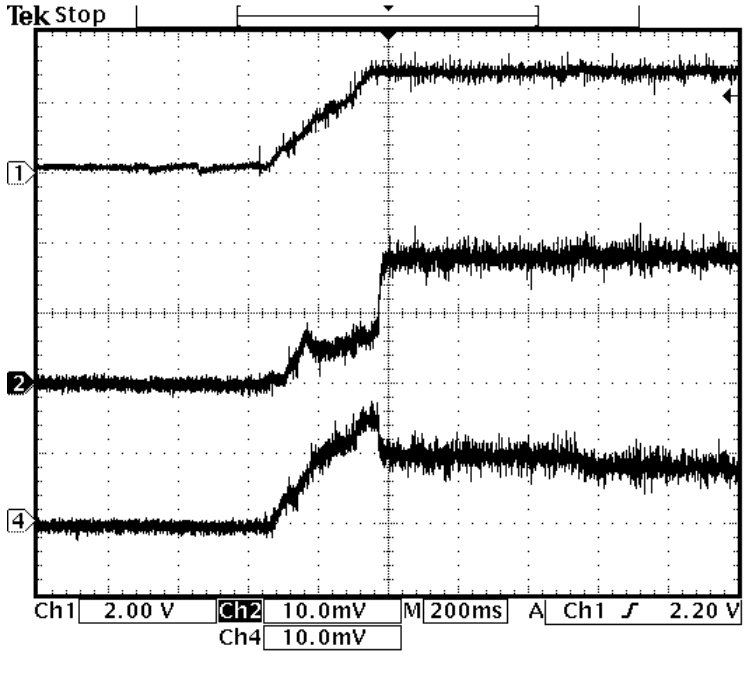
Ch2: $I_{IN(5V)}$ (1A/Div)

Ch4: $I_{IN(12V)}$ (1A/Div)

I_{OUT}: 4.004 Amps

Typical Characteristics - 2 Channels with Current Sharing (Cont.)

Figure 3: V_{OUT} vs $I_{IN(5V)}$ and $I_{IN(12V)}$ with V_{CC} applied and 12A load. Soft start capacitor = 10nF.



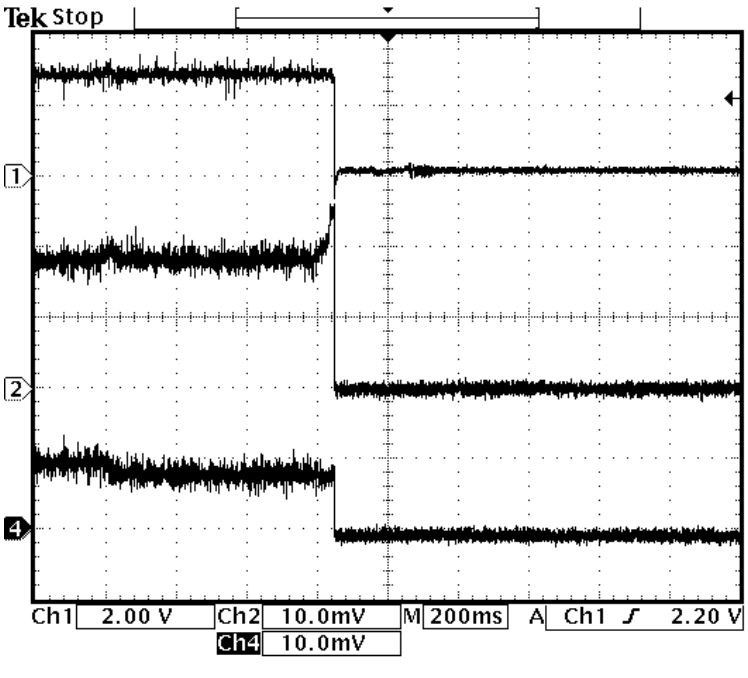
Ch1: V_{OUT}

Ch2: $I_{IN(5V)}$ (2A/Div)

Ch4: $I_{IN(12V)}$ (2A/Div)

I_{OUT}: 12 Amps

Figure 4: V_{OUT} vs $I_{IN(5V)}$ and $I_{IN(12V)}$ with V_{CC} removed and 12A load. Soft start capacitor = 10nF.



Ch1: V_{OUT}

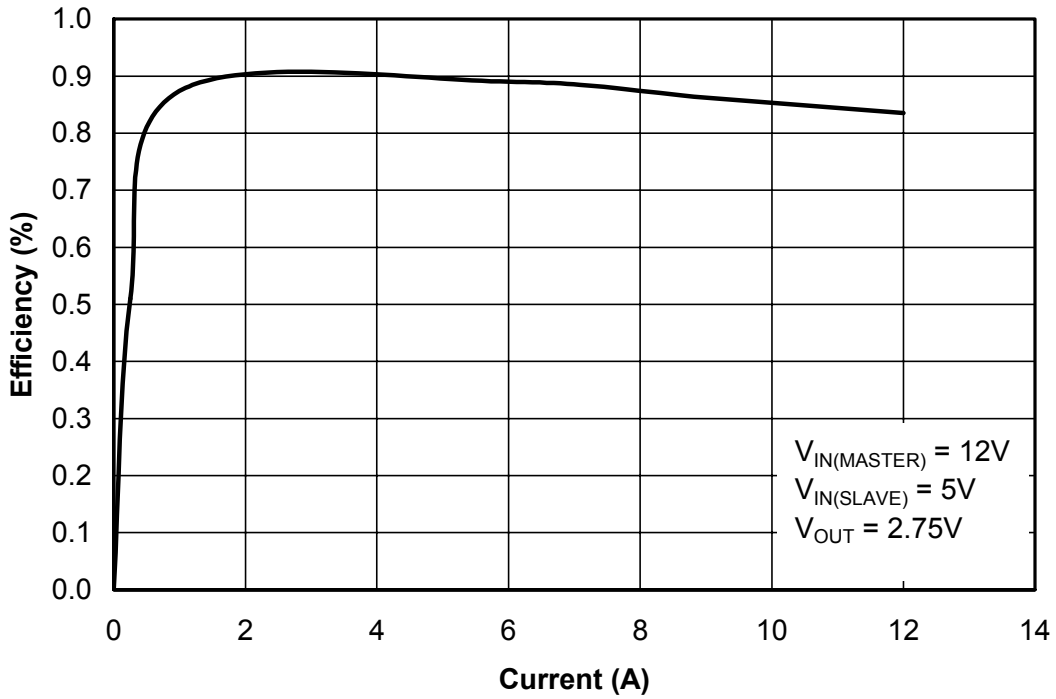
Ch2: $I_{IN(5V)}$ (2A/Div)

Ch4: $I_{IN(12V)}$ (2A/Div)

I_{OUT}: 12 Amps

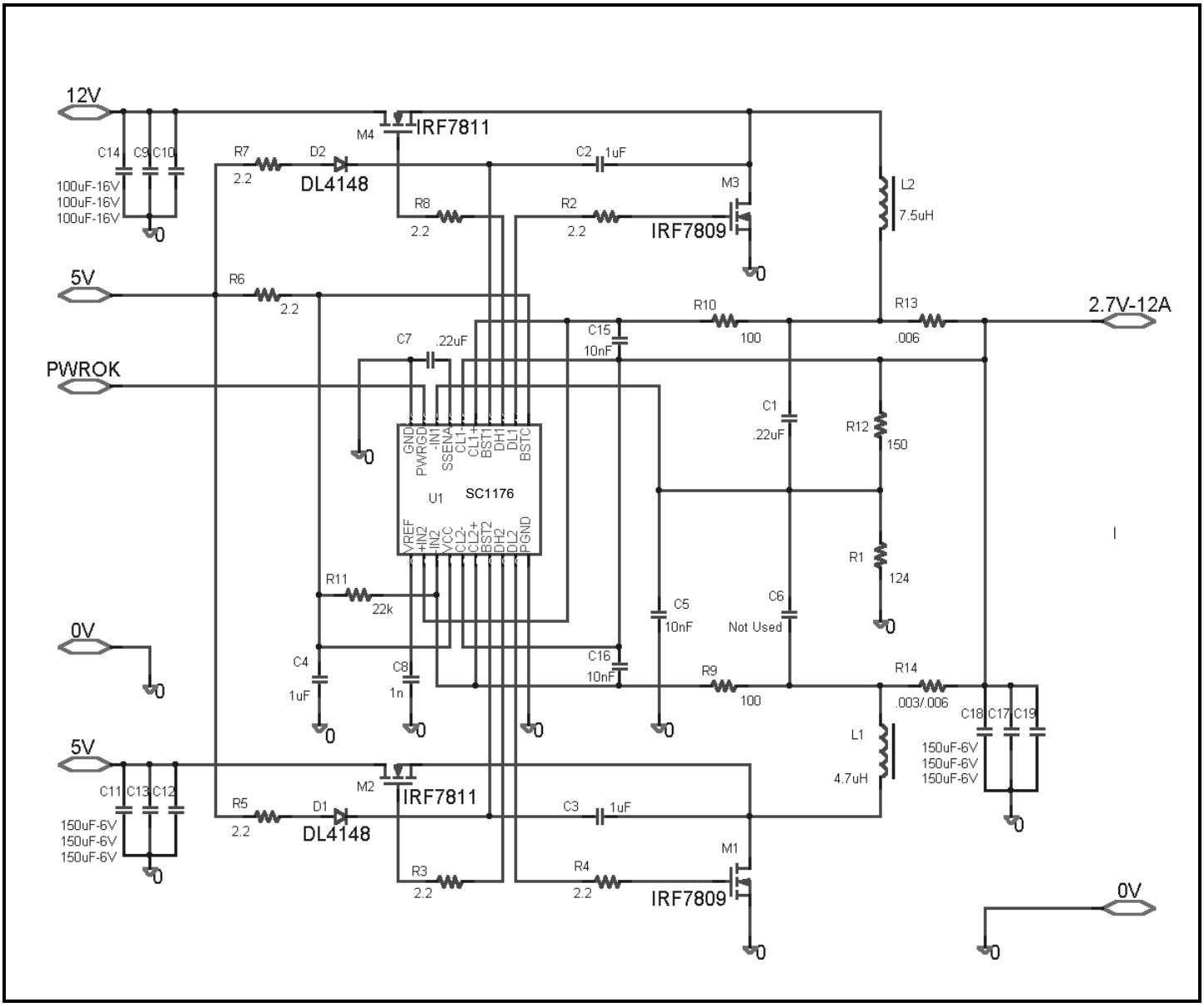
Typical Characteristics - 2 Channels with Current Sharing (Cont.)

Figure 5: Efficiency data - current sharing mode.



The Current Sharing Evaluation Board is not intended for a specific application. The power components are not optimized for minimum cost and size. This evaluation board should be used to understand the operation of the SC1176. To design with SC1176 for specific current sharing applications. Please refer to: Application note AN00-3.

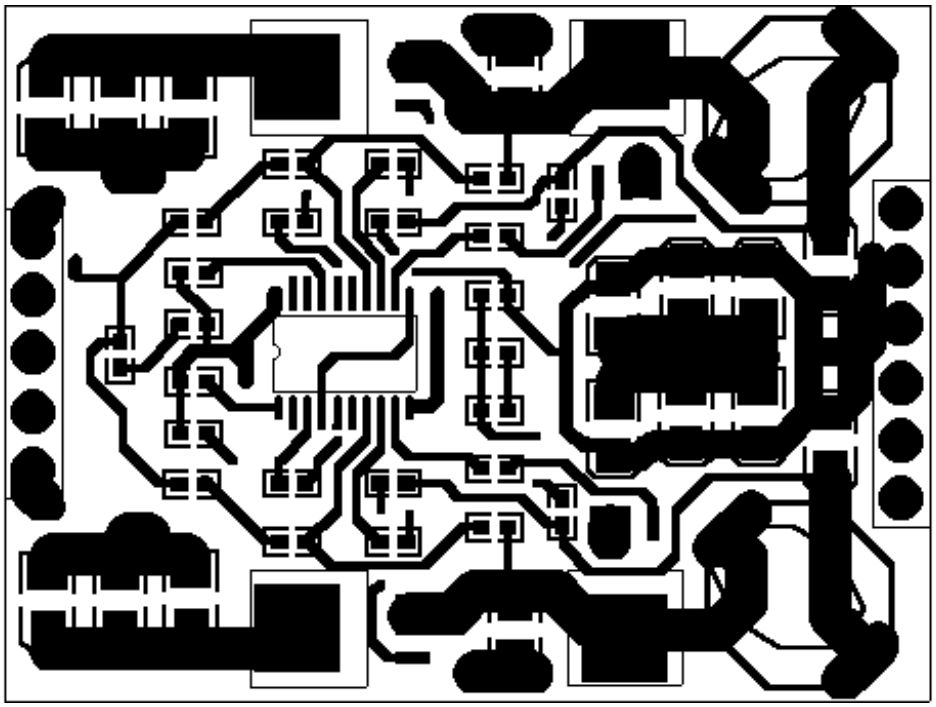
Evaluation Board Schematic - 2 Channel with Current Sharing



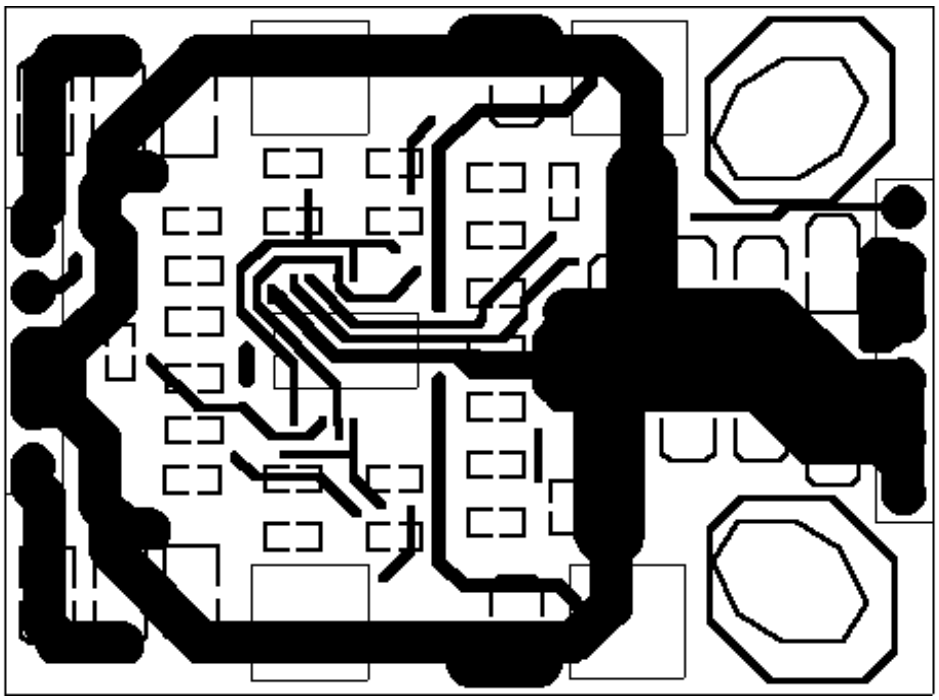
Evaluation Board Bill of Materials - 2 Channels with Current Sharing

Item	Quantity	Reference	Part
1	2	C1,C7	.22uF, 50V
2	3	C2,C3,C4	1uF, 50V
3	3	C5,C15,C16	10nF, 50V
4	1	C8	1nF, 50V
5	3	C9,C10,C14	100uF, 6V
6	6	C11,C12,C13,C17,C18,C19	150uF, 16V
7	2	D1,D2	DL4148
8	1	L1	7.5uH, 8A
9	1	L2	4.7uH, 8A
10	2	M1,M3	IRF7809 or FDB7030
11	2	M2,M4	IRF7811 or FDB7030
12	1	R1	124
13	7	R2,R3,R4,R5,R6,R7,R8	2.2
14	2	R9,R10	100
15	1	R12	150
16	1	R13	.006
17	1	R14	.003
18	1	U1	SC1176

Evaluation Board Gerber Plots - 2 Channels with Current Sharing

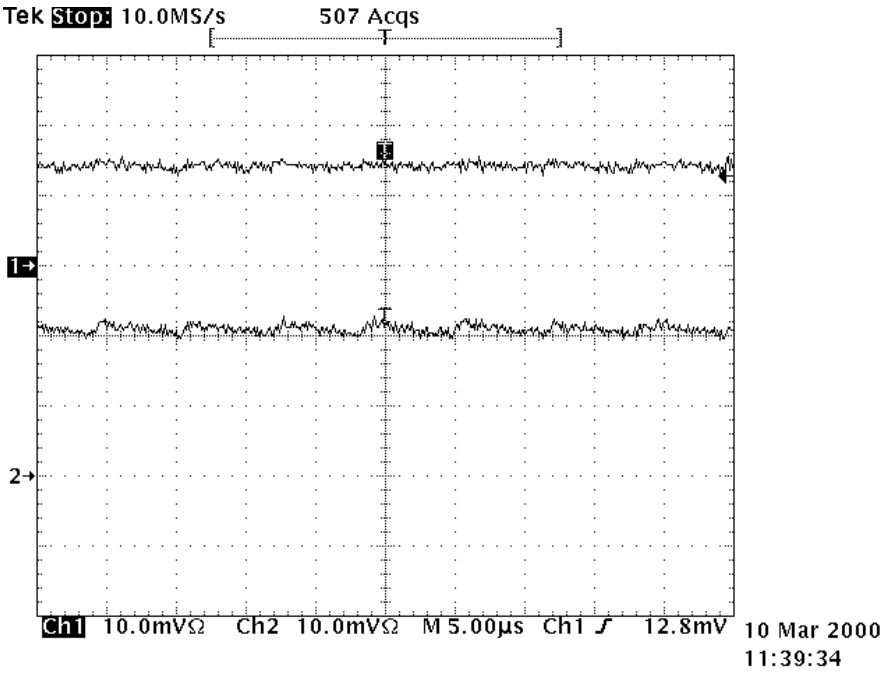


Top Side Traces

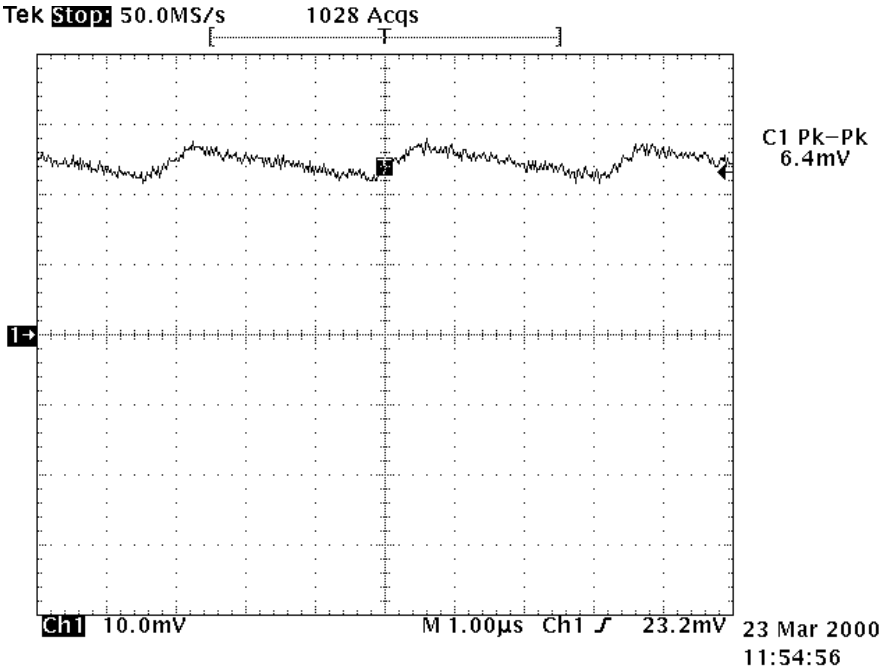


Bottom Side Traces

Typical Characteristics - 2 Independent Channels



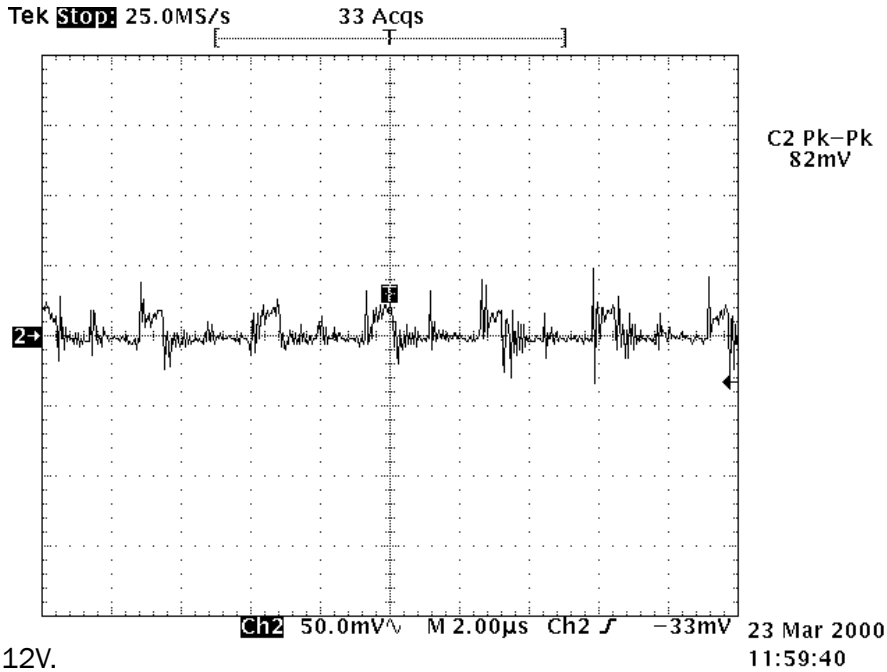
Output Current



Input Voltage = 12V @ 5Amps. 2A/DIV.

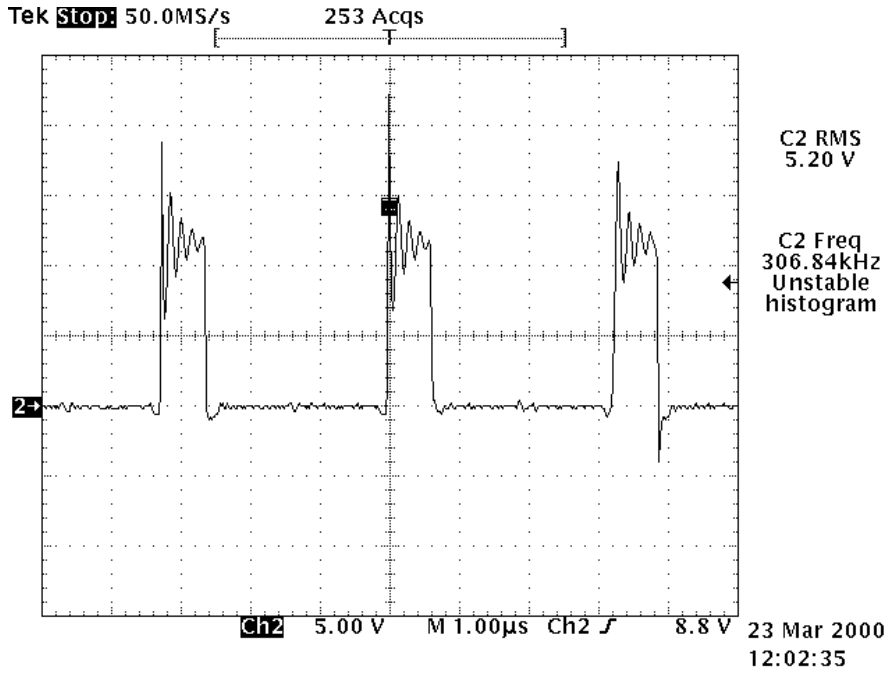
Typical Characteristics - 2 Independent Channels (Cont.)

Peak - Peak Output Ripple @ 5A



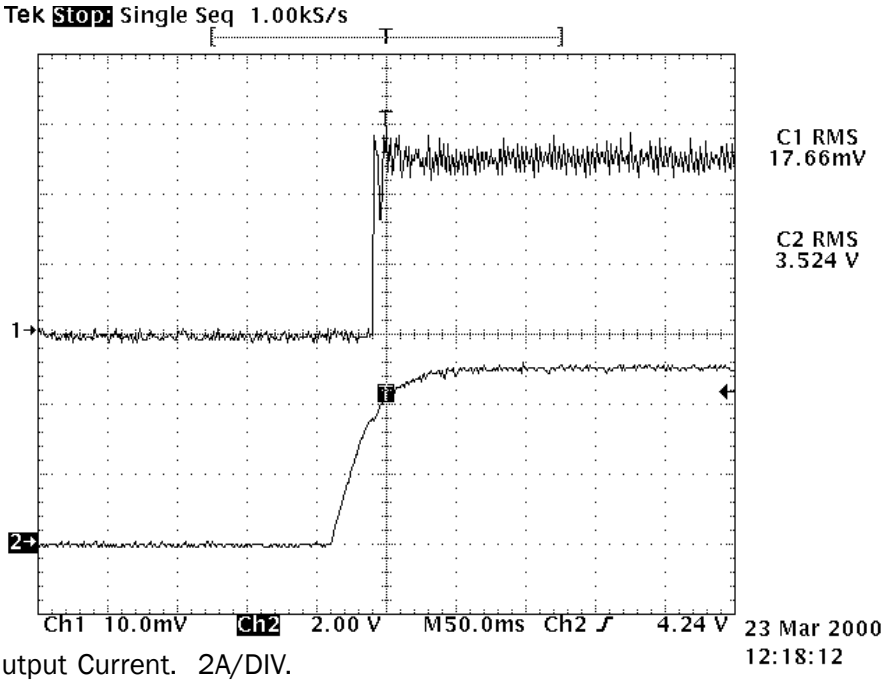
Input Voltage = 12V.
Output Voltage = 2.0V

Phase Node 12V Input @ 5A (without snubber and RC network.



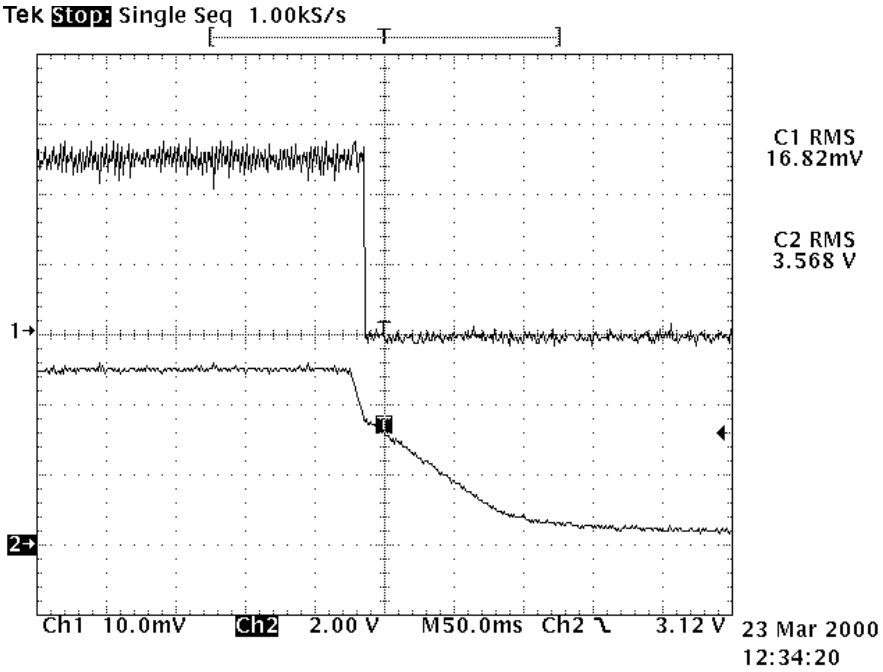
Typical Characteristics - 2 Independent Channels (Cont.)

Start-up Power On



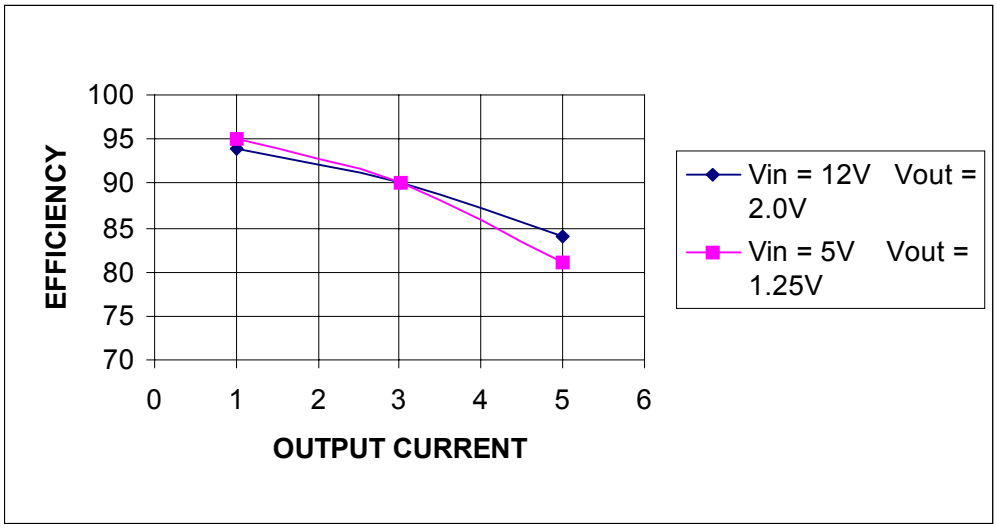
Chan. 1 = Output Current. 2A/DIV.
Chan. 2 = 5V Bias Voltage

Power Off



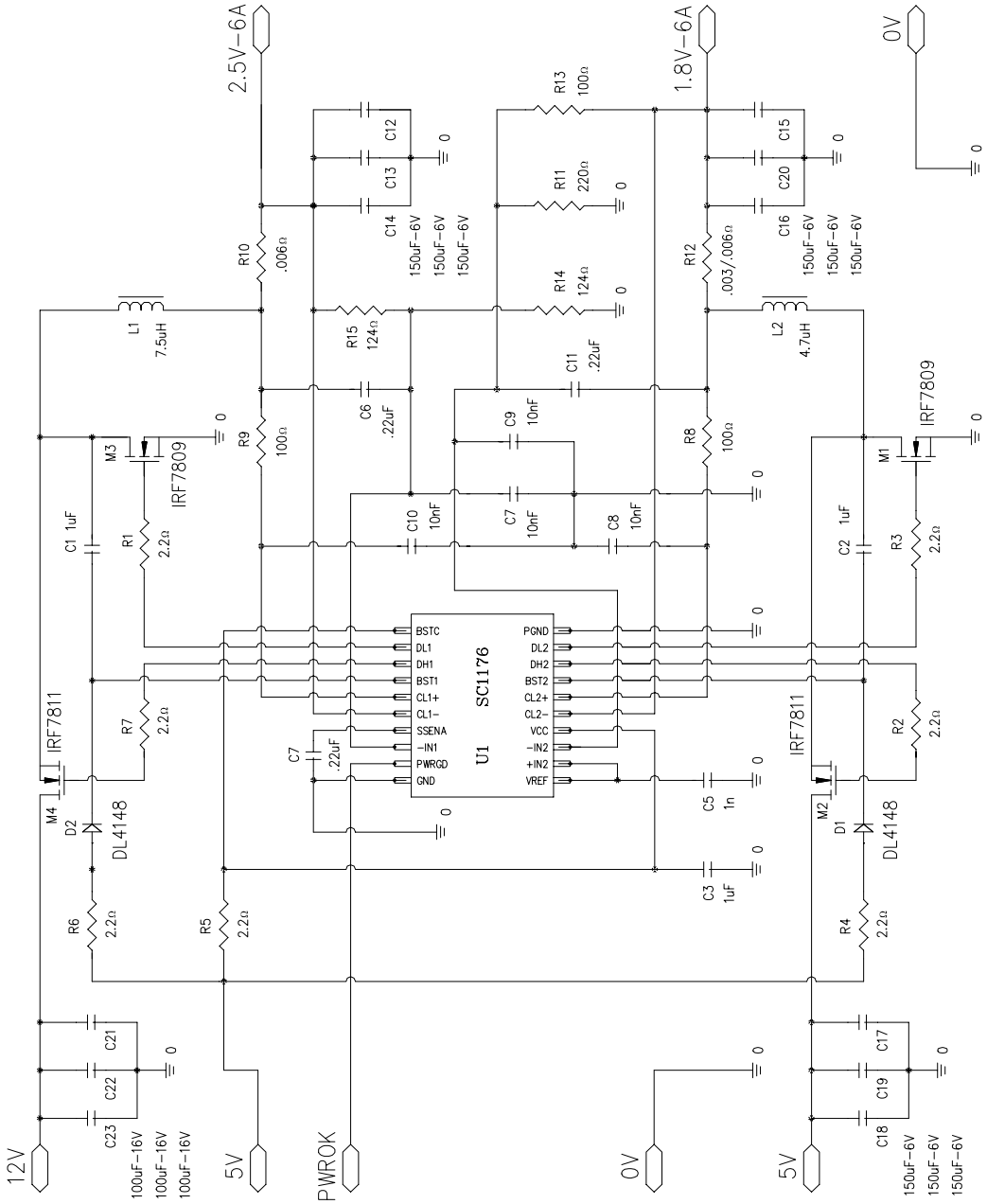
Chan. 1 = Output Current. 2A/DIV.
Chan. 2 = 5V Bias Voltage

Typical Characteristics - 2 Independent Channels Efficiency Test



The Independent Channels Evaluation Board is not intended for a specific application. The power components are not optimized for minimum cost and size. This evaluation board should be used to understand the operation of the SC1176. To design with the SC1176 for specific independent channels applications. Please refer to: Application note AN00-4.

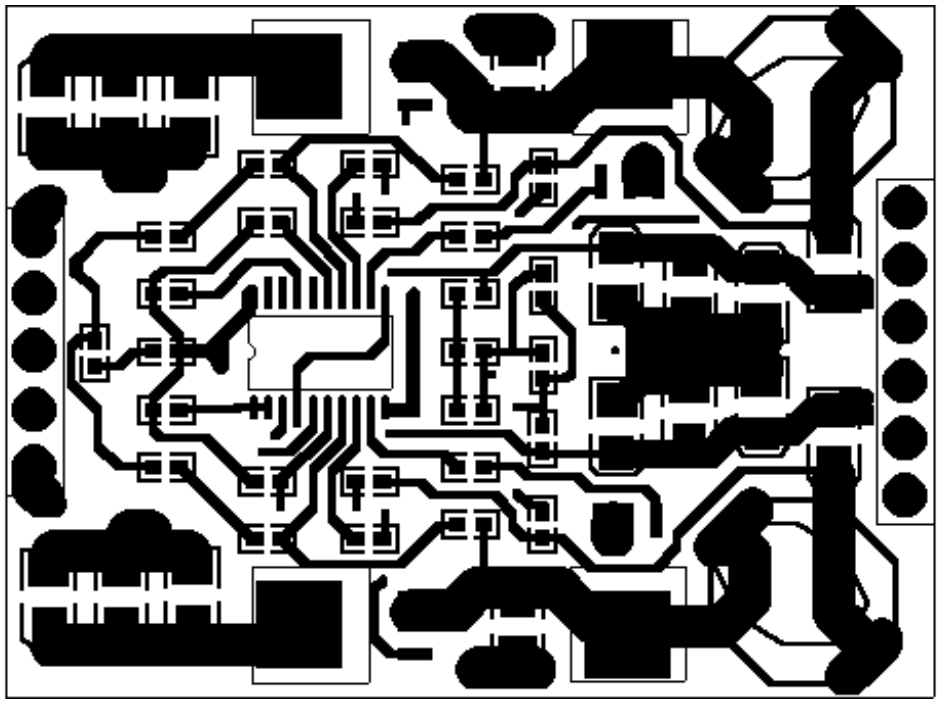
Evaluation Board Schematic - 2 Independent Channels



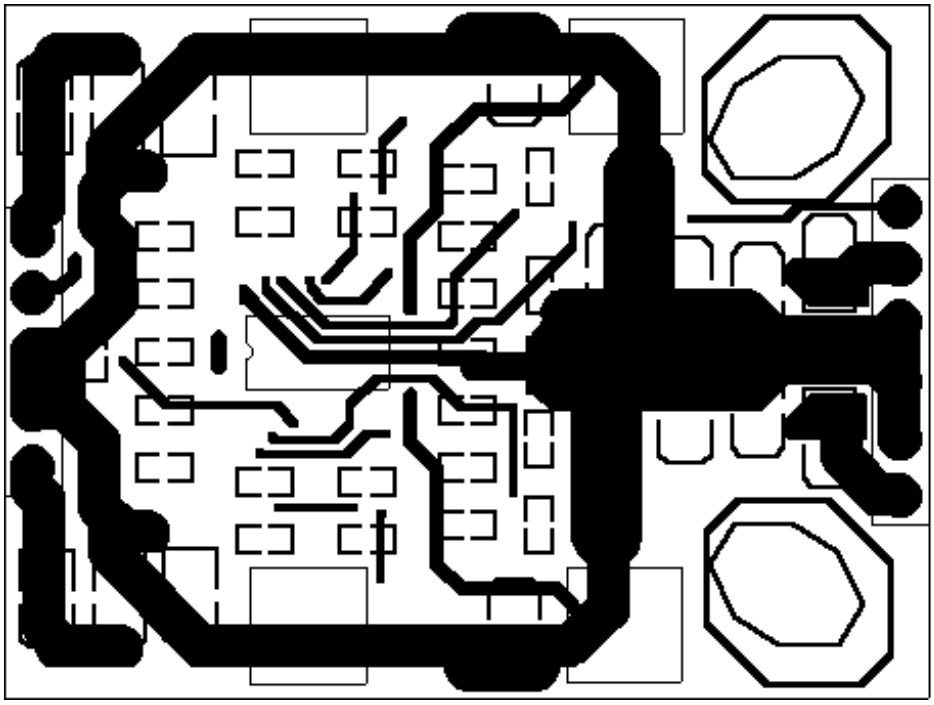
Evaluation Board Bill of Materials - 2 Independent Channels

Item	Quantity	Reference	Part
1	3	C1,C2,C3	1uF, 50V
2	3	C4,C6,C11	.22uF, 50V
3	1	C5	1nF, 50V
4	4	C7,C8,C9,C10	10nF, 50V
5	9	C12,C13,C14,C15,C16,C17,C18,C19,C20	150uF, 6V
6	3	C21,C22,C23	100uF, 16V
7	2	D1,D2	DL4148
8	1	L1	7.5uH, 8A
9	1	L2	4.7uH, 8A
10	2	M1,M3	IRF7809 or FDB7030
11	2	M2,M4	IRF7811 or FDB7030
12	7	R1,R2,R3,R4,R5,R6,R7	2.2
13	3	R8,R9,R13	100
14	1	R10	.006
15	1	R11	220
16	1	R12	.003
17	2	R14,R15	124
18	1	U1	SC1176

Evaluation Board Gerber Plots - 2 Independent Channels



Top Side Traces



Bottom Side Traces

Layout Guidelines

Power and signal traces must be kept separated for noise considerations. Feedback, current sense traces and analog ground should not cross any traces or planes carrying high switching currents, such as the input loop or the phase node.

The input loop, consisting of the input capacitors and both MOSFETs must be kept as small as possible. All of the high switching currents occur in this loop. The enclosed loop area must be kept small to minimize inductance and radiated and conducted emissions. Designing for minimum trace length is not always the best approach, often a more optimum layout can be achieved by keeping loop area constraints in mind.

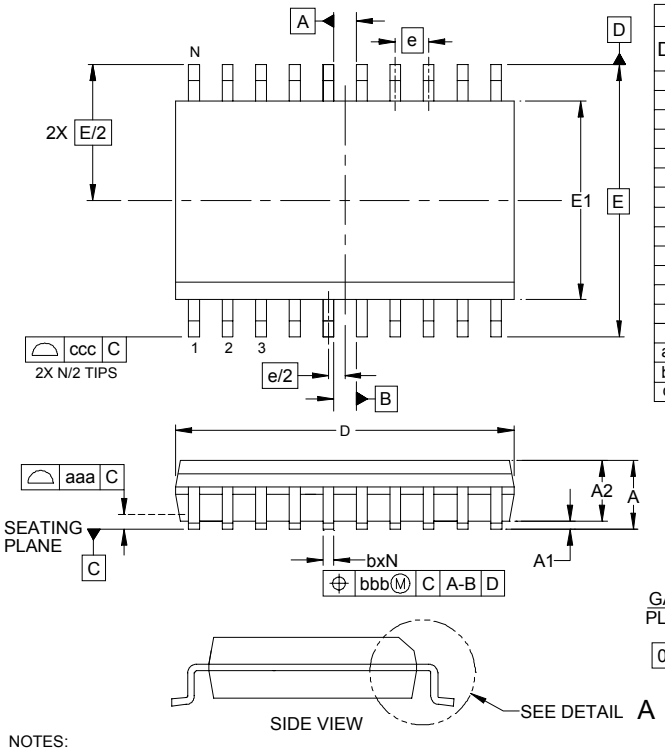
It is important to keep gate lengths short, the IC must be close to the power switches. This is more difficult in a dual channel device than a single and requires that the two power paths run on either side of a centrally located controller.

Grounding requirements are always conflicting in a buck converter, especially at high power, and the trick is to achieve the best compromise. Power ground (PGND) should be returned to the bottom MOSFET source to provide the best gate current return path. Analog ground (GND) should be returned to the ground side of the output capacitors so that the analog circuitry in the controller has an electrically quiet reference and to provide the greatest feedback accuracy. The problem is that the differential voltage capability of the two IC grounds is limited to about 1V for proper operation and so the physical separation between the two grounds must also be minimized. If the grounds are too far apart, fast current transitions in the connection can generate voltage spikes exceeding the 1V capability, resulting in unstable and erratic behavior.

The feedback divider must be close to the IC and be returned to analog ground. Current sense traces must be run parallel and close to each other and to analog ground.

The IC must have a ceramic decoupling capacitor across its supply pins, mounted as close to the device as possible. The small ceramic, noise-filtering capacitors on the current sense lines should also be placed as close to the IC as possible.

Outline Drawing - SOIC-20

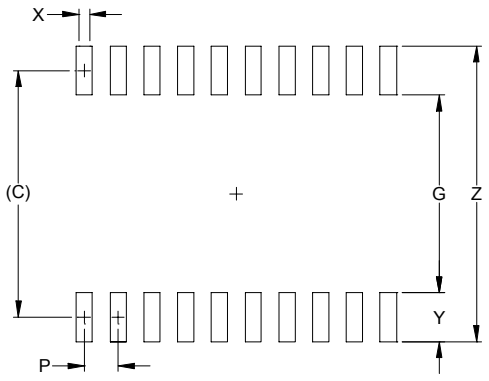


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.093	-	.104	2.35	-	2.65
A1	.004	-	.012	0.10	-	0.30
A2	.081	-	.100	2.05	-	2.55
b	.012	-	.020	0.31	-	0.51
c	.008	-	.013	0.20	-	0.33
D	.500	.504	.508	12.70	12.80	12.90
E1	.291	.295	.299	7.40	7.50	7.60
E	.406 BSC			10.30 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.030	0.25	-	0.75
L	.016	-	.041	0.40	-	1.04
L1	(.041)			(1.04)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.013			0.33		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-013, VARIATION AC.

Land Pattern - SOIC-20

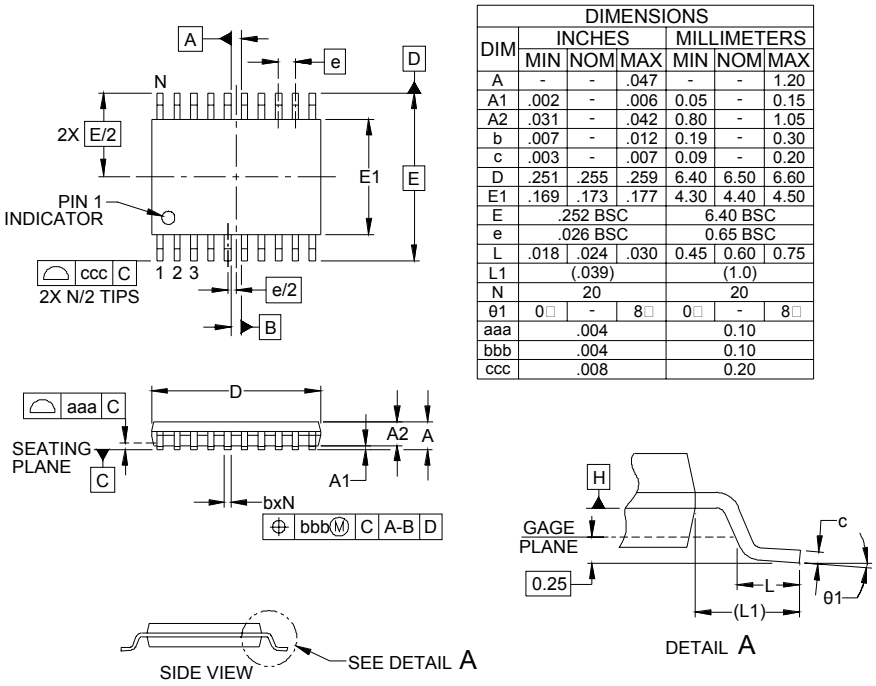


DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.362)	(9.20)
G	.276	7.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.449	11.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 307A.

Outline Drawing - TSSOP-20

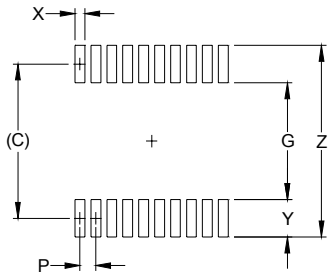


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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