

# CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

**ICS840S05I**

## GENERAL DESCRIPTION

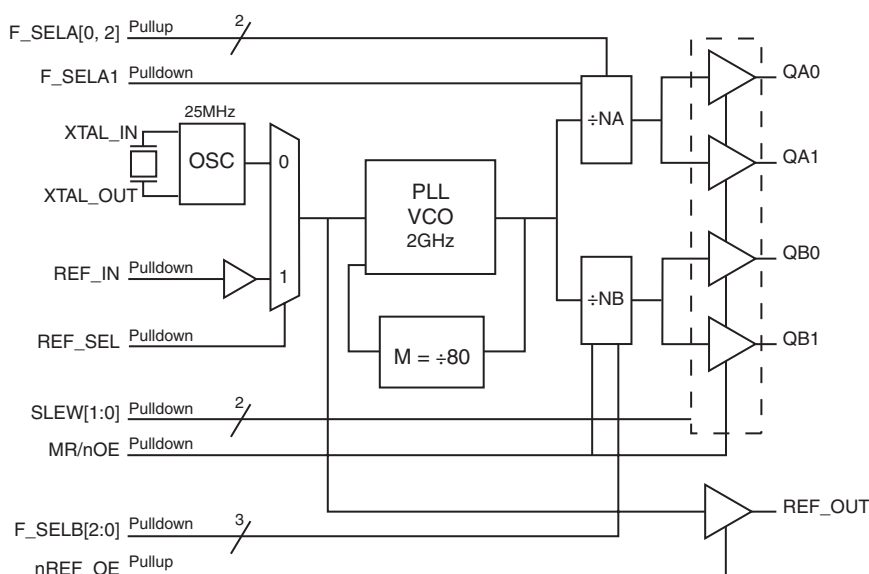
The ICS840S05I is a four output, Crystal or single ended-to-LVCMOS/LVTTL Frequency Synthesizer and a member of HiperClocks™ family of high performance clock solutions from IDT. The ICS840S05I uses a 25MHz parallel resonant crystal to generate 33.33MHz – 166.67MHz clock signals, replacing solutions requiring multiple oscillator and fan-out buffer solution. The device supports output slew rate control with two slew select pins (SLEW[1:0]). The VCO operates at a frequency of 2GHz. The device has 2 output banks, Bank A with two 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs and Bank B with two 33.33MHz – 166.67MHz LVCMOS/LVTTL outputs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The low phase noise characteristic of the ICS840S05I makes it an ideal clock source for Gigabit Ethernet application. Designed for networking and industrial applications, the ICS840S05I can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

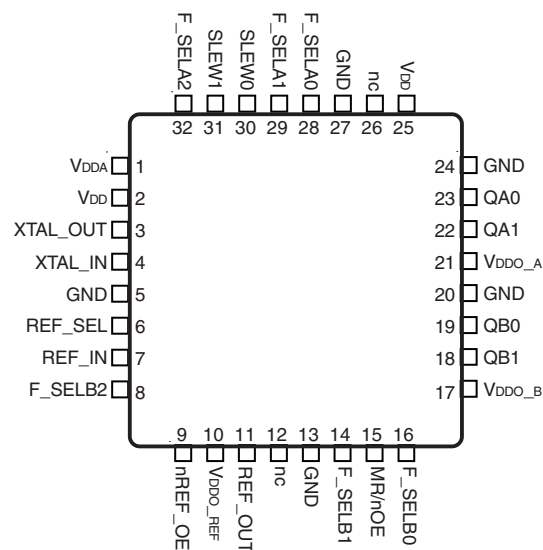
## FEATURES

- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- One REF\_OUT LVCMOS/LVTTL clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference input
- Supports the following output frequencies:  
Bank A/Bank B: 33.33MHz, 50MHz, 66.67MHz, 83.33MHz, 100MHz, 125MHz, 133.33MHz, and 166.67MHz
- VCO: 2GHz
- Slew rate control
- RMS period jitter: 10ps (typical)
- Output supply modes:  
Core/Output  
3.3V/3.3V  
3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS840S05I**  
**32-Lead TQFP, E-Pad**  
 7mm x 7mm x 1.0mm package body  
**Y package**  
 Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

| Number               | Name                            | Type   |          | Description                                                                                                                                                                                                                                          |
|----------------------|---------------------------------|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                    | V <sub>DDA</sub>                | Power  |          | Analog supply pin.                                                                                                                                                                                                                                   |
| 2, 25                | V <sub>DD</sub>                 | Power  |          | Core supply pin.                                                                                                                                                                                                                                     |
| 3,<br>4              | XTAL_OUT,<br>XTAL_IN            | Input  |          | Crystal oscillator interface. XTAL_OUT is the output.<br>XTAL_IN is the input.                                                                                                                                                                       |
| 5, 13, 20,<br>24, 27 | GND                             | Power  |          | Power supply ground.                                                                                                                                                                                                                                 |
| 6                    | REF_SEL                         | Input  | Pulldown | Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. LVCMOS/LVTTL interface levels.                                                                                                                                            |
| 7                    | REF_IN                          | Input  | Pulldown | Single-ended LVCMOS/LVTTL reference clock input.                                                                                                                                                                                                     |
| 8,<br>14,<br>16      | F_SELB2,<br>F_SELB1,<br>F_SELB0 | Input  | Pulldown | Frequency select pins for Bank B outputs.<br>See Table 3A. LVCMOS/LVTTL interface levels.                                                                                                                                                            |
| 9                    | nREF_OE                         | Input  | Pullup   | Active low REF_OUT enable/disable pin.<br>LVCMOS/LVTTL interface levels.                                                                                                                                                                             |
| 10                   | V <sub>DDO_REF</sub>            | Power  |          | Output supply pin for REF_OUT clock output.<br>LVCMOS/LVTTL interface levels.                                                                                                                                                                        |
| 11                   | REF_OUT                         | Output |          | Single-ended LVCMOS/LVTTL reference clock output.                                                                                                                                                                                                    |
| 12, 26               | nc                              | Unused |          | No connect.                                                                                                                                                                                                                                          |
| 15                   | MR/nOE                          | Input  | Pulldown | Active HIGH Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (HI-Z). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 17                   | V <sub>DDO_B</sub>              | Power  |          | Output supply pin for QBx outputs.                                                                                                                                                                                                                   |
| 18, 19               | QB1, QB0                        | Output |          | Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels.<br>15Ω typical output impedance.                                                                                                                                                   |
| 21                   | V <sub>DDO_A</sub>              | Power  |          | Output supply pin for QAx outputs.                                                                                                                                                                                                                   |
| 22, 23               | QA1, QA0                        | Output |          | Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels.<br>15Ω typical output impedance.                                                                                                                                                   |
| 28,<br>32            | F_SEL_A0,<br>F_SELA2            | Input  | Pullup   | Frequency select pins for Bank A outputs.<br>See Table 3A. LVCMOS/LVTTL interface levels.                                                                                                                                                            |
| 29                   | F_SELA1                         | Input  | Pulldown | Frequency select pin for Bank A outputs.<br>See Table 3A. LVCMOS/LVTTL interface levels.                                                                                                                                                             |
| 30,<br>31            | SLEW0,<br>SLEW1                 | Input  | Pulldown | Slew rate select pins for LVCMOS/LVTTL clock output. See Table 3B.<br>LVCMOS/LVTTL interface levels.                                                                                                                                                 |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol         | Parameter                     | Test Conditions                                                                                   | Minimum | Typical | Maximum | Units      |
|----------------|-------------------------------|---------------------------------------------------------------------------------------------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance             |                                                                                                   |         | 4       |         | pF         |
| $C_{PD}$       | Power Dissipation Capacitance | Slew Rate = 2.75V/ns<br>$V_{DD}, V_{DDA}, V_{DDO\_REF}, V_{DDO\_A}, V_{DDO\_B} = 3.465V$          |         | TBD     |         | pF         |
|                |                               | Slew Rate = 1ns<br>$V_{DD}, V_{DDA}, V_{DDO\_REF}, V_{DDO\_A}, V_{DDO\_B} = 3.465V$               |         | TBD     |         | pF         |
|                |                               | Slew Rate = 2.75V/ns<br>$V_{DD}, V_{DDA} = 3.465V, V_{DDO\_REF}, V_{DDO\_A}, V_{DDO\_B} = 2.625V$ |         | TBD     |         | pF         |
|                |                               | Slew Rate = 1ns<br>$V_{DD}, V_{DDA} = 3.465V, V_{DDO\_REF}, V_{DDO\_A}, V_{DDO\_B} = 2.625V$      |         | TBD     |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor         |                                                                                                   |         | 51      |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor       |                                                                                                   |         | 51      |         | k $\Omega$ |
| $R_{OUT}$      | Output Impedance              |                                                                                                   |         | 15      |         | $\Omega$   |

TABLE 3A. FREQUENCY SELECT FUNCTION TABLE

|                     |                     | Inputs              |                 |                         | Output Frequency<br>(25MHz Reference) |               |
|---------------------|---------------------|---------------------|-----------------|-------------------------|---------------------------------------|---------------|
| F_SELA2,<br>F_SELB2 | F_SELA1,<br>F_SELB1 | F_SELA0,<br>F_SELB0 | M Divider Value | NA, NB<br>Divider Value | QA[2:0] (MHz)                         | QB[2:0] (MHz) |
| L                   | L                   | L                   | 80              | 60                      | 33.33                                 | 33.33         |
| L                   | L                   | H                   | 80              | 40                      | 50                                    | 50            |
| L                   | H                   | L                   | 80              | 30                      | 66.67                                 | 66.67         |
| L                   | H                   | H                   | 80              | 24                      | 83.33                                 | 83.33         |
| H                   | L                   | L                   | 80              | 20                      | 100                                   | 100           |
| H                   | L                   | H                   | 80              | 16                      | 125                                   | 125           |
| H                   | H                   | L                   | 80              | 15                      | 133.33                                | 133.33        |
| H                   | H                   | H                   | 80              | 12                      | 166.67                                | 166.67        |

TABLE 3B. SLEW RATE FUNCTION TABLE

| Setting |       | Slew Rate |
|---------|-------|-----------|
| SLEW1   | SLEW0 | (V/ns)    |
| 0       | 0     | 2.95      |
| 0       | 1     | 2.25      |
| 1       | 0     | 1.5       |
| 1       | 1     | 0.8       |

NOTE: Please refer to the AC Characteristics Table for slew rate test condition.

#### ABSOLUTE MAXIMUM RATINGS

|                                          |                               |
|------------------------------------------|-------------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                          |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5$ V     |
| Outputs, $V_O$                           | -0.5V to $V_{DDO\_X} + 0.5$ V |
| Package Thermal Impedance, $\theta_{JA}$ | 36.2°C/W (0 mps)              |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C                |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol                                 | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|----------------------------------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$                               | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$                              | Analog Supply Voltage |                 | $V_{DD} - 0.20$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_A}, V_{DDO\_B}, V_{DDO\_REF}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{DD}$                               | Power Supply Current  |                 |                 | 135     |          | mA    |
| $I_{DDA}$                              | Analog Supply Current |                 |                 | 20      |          | mA    |
| $I_{DDO\_A}, I_{DDO\_B}, I_{DDO\_REF}$ | Output Supply Current |                 |                 | 1       |          | mA    |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

| Symbol                                 | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|----------------------------------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$                               | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$                              | Analog Supply Voltage |                 | $V_{DD} - 0.20$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_A}, V_{DDO\_B}, V_{DDO\_REF}$ | Output Supply Voltage |                 | 2.375           | 2.5     | 2.625    | V     |
| $I_{DD}$                               | Power Supply Current  |                 |                 | 135     |          | mA    |
| $I_{DDA}$                              | Analog Supply Current |                 |                 | 20      |          | mA    |
| $I_{DDO\_A}, I_{DDO\_B}, I_{DDO\_REF}$ | Output Supply Current |                 |                 | 1       |          | mA    |

**TABLE 4C. LVCMOS DC CHARACTERISTICS,  $V_{DD} = V_{DDO\_REF} = 3.3V \pm 5\%$ ,  $V_{DDO\_A} = V_{DDO\_B} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol   | Parameter                   | Test Conditions                                                                                         | Minimum | Typical | Maximum        | Units   |
|----------|-----------------------------|---------------------------------------------------------------------------------------------------------|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          | $V_{DD} = 3.465V$                                                                                       | 2       |         | $V_{DD} + 0.3$ | V       |
|          |                             | $V_{DD} = 3.465V$                                                                                       | 1.7     |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           | $V_{DD} = 2.625V$                                                                                       | -0.3    |         | 0.8            | V       |
|          |                             | $V_{DD} = 2.625V$                                                                                       | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current          | nREF_OE, F_SELA0, F_SELA2<br>$V_{DD} = V_{IN} = 3.465V$ or $2.625V$                                     |         |         | 5              | $\mu A$ |
|          |                             | F_SELB[0:2], SLEW0, SLEW1<br>F_SELA1, MR/nOE, REF_IN, REF_SEL<br>$V_{DD} = V_{IN} = 3.465V$ or $2.625V$ |         |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current           | nREF_OE, F_SELA0, F_SELA2<br>$V_{DD} = V_{IN} = 3.465V$ or $2.625V$                                     | -150    |         |                | $\mu A$ |
|          |                             | F_SELB[0:2], SLEW0, SLEW1<br>F_SELA1, MR/nOE, REF_IN, REF_SEL<br>$V_{DD} = V_{IN} = 3.465V$ or $2.625V$ | -5      |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 | $V_{DDO\_A\_B\_REF} = 3.3V \pm 5\%$                                                                     | 2.6     |         |                | V       |
|          |                             | $V_{DDO\_A\_B\_REF} = 2.5V \pm 5\%$                                                                     | 1.8     |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  | $V_{DDO\_A\_B\_REF} = 3.3V$ or $2.5V \pm 5\%$                                                           |         |         | 0.5            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO\_A\_B\_REF}/2$ . See Parameter Measurement Information, Output Load Test Circuit diagram.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 6A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol         | Parameter              |            | Test Conditions                                                 | Minimum | Typical | Maximum | Units |
|----------------|------------------------|------------|-----------------------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$      | Output Frequency       | QAx        |                                                                 |         | 125     |         | MHz   |
|                |                        | QBx        |                                                                 | 33.33   |         | 200     | MHz   |
| $tsk(o)$       | Output Skew; NOTE 1, 2 |            |                                                                 |         | 40      |         | ps    |
| $tsk(b)$       | Bank Skew; NOTE 2, 3   |            |                                                                 |         | 25      |         | ps    |
| $t_{jit(per)}$ | RMS Period Jitter      |            |                                                                 |         | 10      |         | ps    |
| $t_{SLEW}$     | Slew Rate; NOTE 4      | SLEWx = 00 | Single-ended Output Clock Rise/Fall Time, 20% to 80%; 15pF Load |         | 2.95    |         | V/ns  |
|                |                        | SLEWx = 01 |                                                                 |         | 2.25    |         | V/ns  |
|                |                        | SLEWx = 10 |                                                                 |         | 1.5     |         | V/ns  |
|                |                        | SLEWx = 11 |                                                                 |         | 0.8     |         | V/ns  |
| $t_L$          | PLL Lock Time          |            |                                                                 |         | TBD     |         | ms    |
| odc            | Output Duty Cycle      |            |                                                                 |         | 50      |         | %     |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at  $V_{DDO\_A\_B\_REF}/2$ .

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

**TABLE 6B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO\_REF} = V_{DDO\_A} = V_{DDO\_B} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

| Symbol         | Parameter              |            | Test Conditions                                                 | Minimum | Typical | Maximum | Units |
|----------------|------------------------|------------|-----------------------------------------------------------------|---------|---------|---------|-------|
| $f_{OUT}$      | Output Frequency       | QAx        |                                                                 |         | 125     |         | MHz   |
|                |                        | QBx        |                                                                 | 33.33   |         | 200     | MHz   |
| $tsk(o)$       | Output Skew; NOTE 1, 2 |            |                                                                 |         | 40      |         | ps    |
| $tsk(b)$       | Bank Skew; NOTE 2, 3   |            |                                                                 |         | 25      |         | ps    |
| $t_{jit(per)}$ | RMS Period Jitter      |            |                                                                 |         | 10      |         | ps    |
| $t_{SLEW}$     | Slew Rate; NOTE 4      | SLEWx = 00 | Single-ended Output Clock Rise/Fall Time, 20% to 80%; 15pF Load |         | 2.95    |         | V/ns  |
|                |                        | SLEWx = 01 |                                                                 |         | 2.25    |         | V/ns  |
|                |                        | SLEWx = 10 |                                                                 |         | 1.5     |         | V/ns  |
|                |                        | SLEWx = 11 |                                                                 |         | 0.8     |         | V/ns  |
| $t_L$          | PLL Lock Time          |            |                                                                 |         | TBD     |         | ms    |
| odc            | Output Duty Cycle      |            |                                                                 |         | 50      |         | %     |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

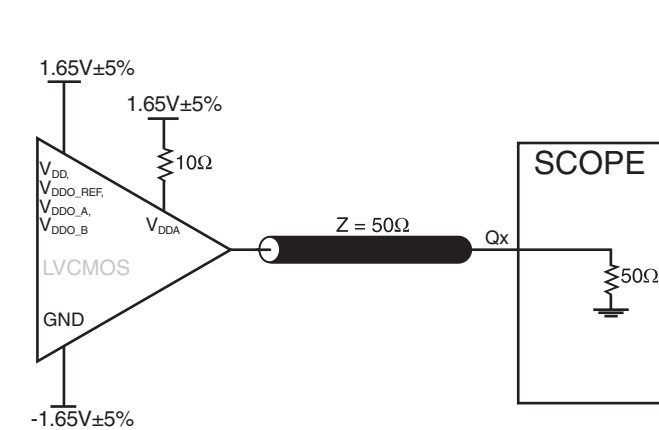
Measured at  $V_{DDO\_A\_B\_REF}/2$ .

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

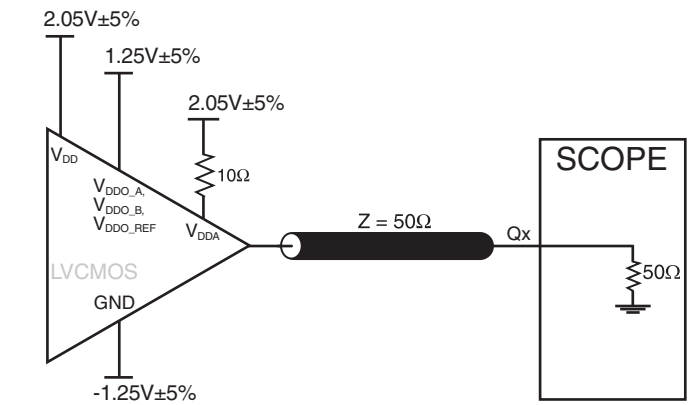
NOTE 3: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 4: A slew rate of 2V/ns or greater should be selected for output frequencies of 100MHz and higher.

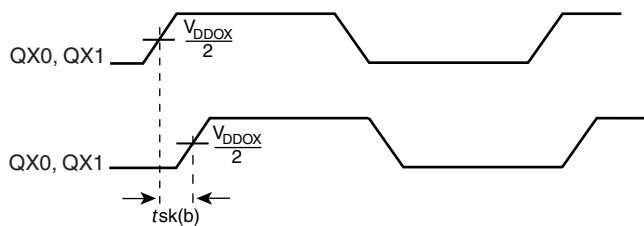
## PARAMETER MEASUREMENT INFORMATION



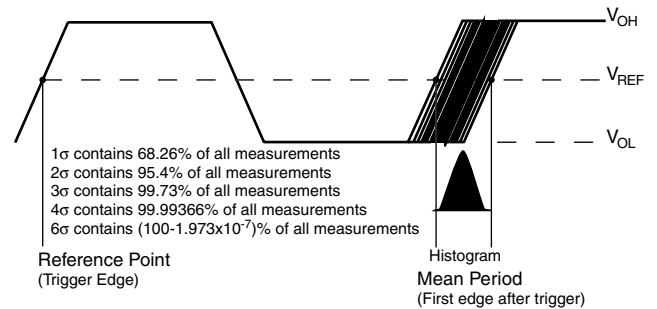
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



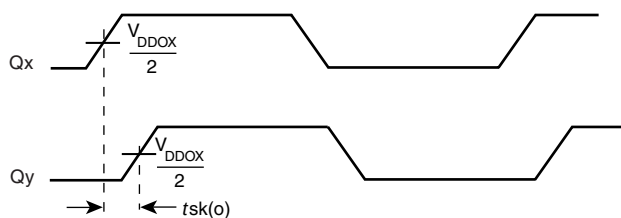
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



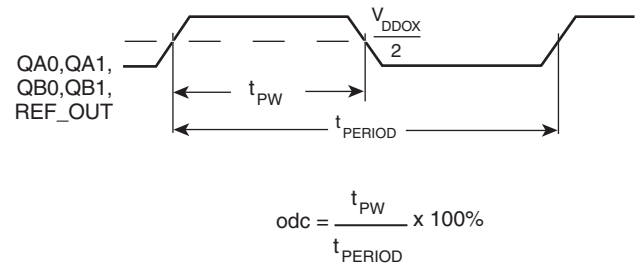
BANK SKEW (where X denotes outputs in the same bank)



RMS PERIOD JITTER



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT SLEW RATE

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840S05I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$  and  $V_{DDO\_REF}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10μF and a .01μF bypass capacitor should be connected to each  $V_{DDA}$ . The 10Ω resistor can also be replaced by a ferrite bead.

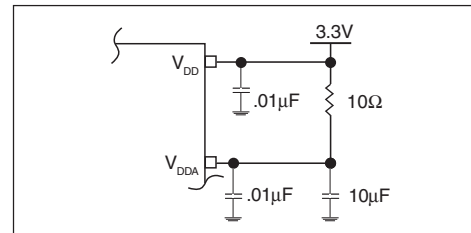


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS840S05I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below

were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

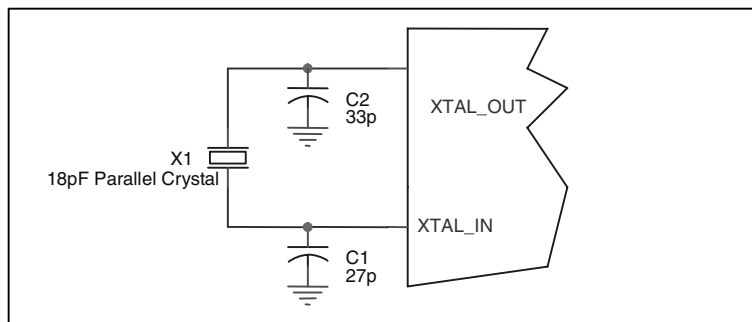


FIGURE 2. CRYSTAL INPUT INTERFACE

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_IN to ground.

##### REF\_IN INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF\_IN to ground.

##### LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.



## LVCMOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 3. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ .

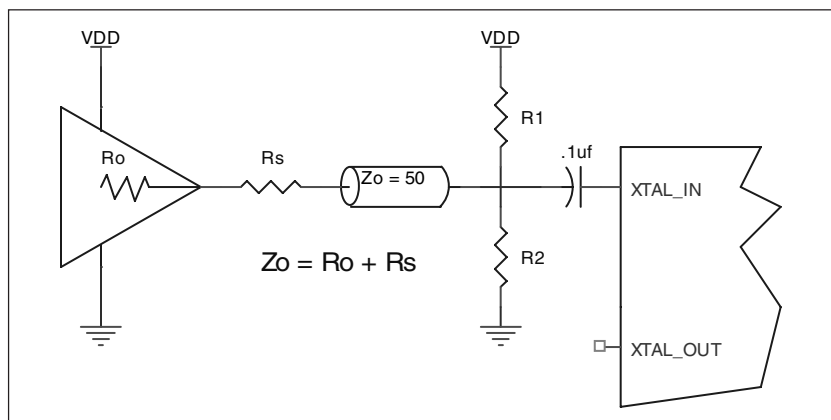


FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

## THERMAL RELEASE PATH

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through

solder as shown in Figure 4. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

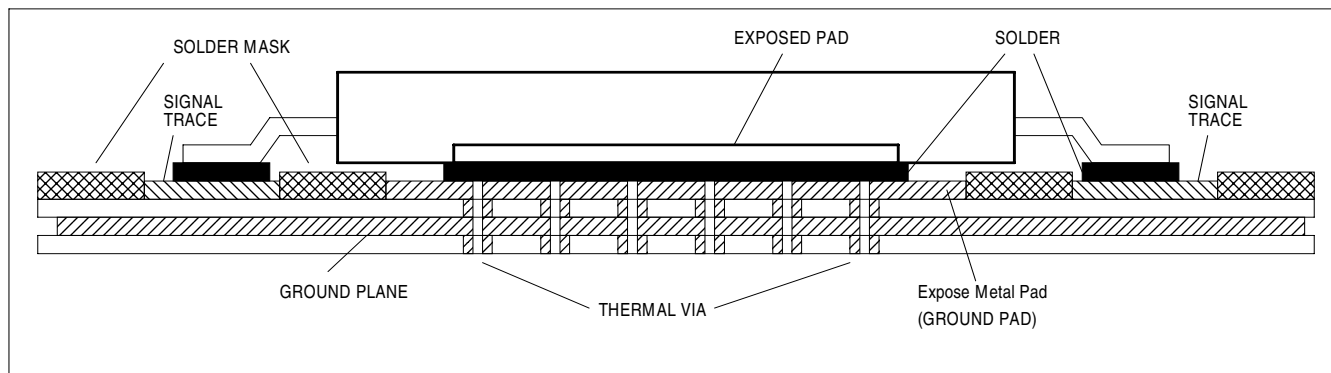


FIGURE 4. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 32 LEAD TQFP, E-PAD

| $\theta_{JA}$ by Velocity (Meters per Second) |          |          |          |
|-----------------------------------------------|----------|----------|----------|
|                                               | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards   | 36.2°C/W | 30.6°C/W | 29.2°C/W |

### TRANSISTOR COUNT

The transistor count for ICS840S05I is: 2349

TQFP PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD TQFP, E-PAD

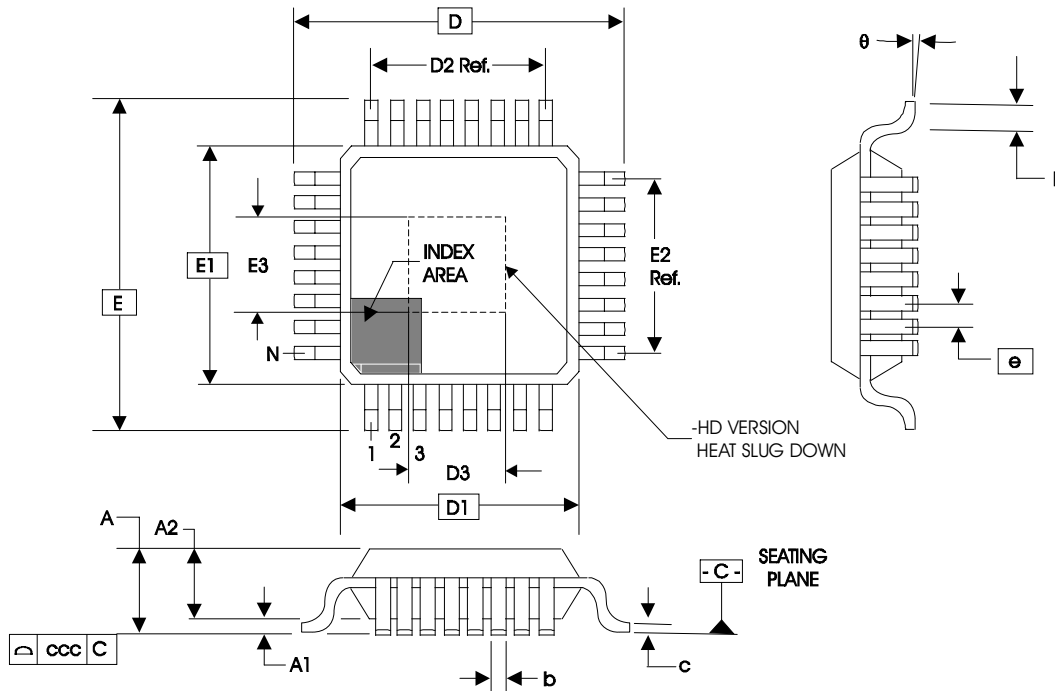


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |            |         |         |
|--------------------------------------------------|------------|---------|---------|
| SYMBOL                                           | ABA-HD     |         |         |
|                                                  | MINIMUM    | NOMINAL | MAXIMUM |
| N                                                | 32         |         |         |
| A                                                | --         | --      | 1.20    |
| A1                                               | 0.05       | 0.10    | 0.15    |
| A2                                               | 0.95       | 1.0     | 1.05    |
| b                                                | 0.30       | 0.35    | 0.40    |
| c                                                | 0.09       | --      | 0.20    |
| D, E                                             | 9.00 BASIC |         |         |
| D1, E1                                           | 7.00 BASIC |         |         |
| D2, E2                                           | 5.60 Ref.  |         |         |
| e                                                | 0.80 BASIC |         |         |
| L                                                | 0.45       | --      | 0.75    |
| $\theta$                                         | 0°         | --      | 7°      |
| ccc                                              | --         | --      | 0.10    |
| D3 & D3                                          | 3.0        | 3.5     | 4.0     |

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking      | Package                         | Shipping Packaging | Temperature   |
|-------------------|--------------|---------------------------------|--------------------|---------------|
| ICS840S05AYI      | ICS840S05AYI | 32 lead TQFP, E-Pad             | tube               | -40°C to 85°C |
| ICS840S05AYIT     | ICS840S05AYI | 32 lead TQFP, E-Pad             | 2500 tape & reel   | -40°C to 85°C |
| ICS840S05AYILF    | ICS840S05AIL | 32 lead "Lead-Free" TQFP, E-Pad | tube               | -40°C to 85°C |
| ICS840S05AYILFT   | ICS840S05AIL | 32 lead "Lead-Free" TQFP, E-Pad | 2500 tape & reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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