SPI Bus Compatibility
*FM25160 16Kb SPI FRAM*

RAMTRON

Overview

The FM25160 uses an industry standard SPI interface. When comparing the FM25160 with 16Kb SPI EEPROMs, users may notice two minor operating differences. First, the SPI bus protocol includes 4 modes which may be selected by the controller. The FM25160 operates in mode 0 only. Some EEPROMs operate in both mode 0 and mode 3. Attempting to communicate in modes other than 0 will cause the FM25160 to behave unpredictably.

Second, there is a minor improvement in overhead by including the upper address bits within the command word rather than as an extra byte. A complete explanation of the SPI modes and the differences in memory addressing follows the troubleshooting section below.

Troubleshooting

The most common difficulty experienced by developers using the FM25160 for the first time relates to the SPI mode. In many cases, this selection is not a conscious decision; rather it is a default condition. The relationship shown in Figure 1 must be satisfied in order to begin communication with the FM25160. As shown, the SCK signal must begin in a low state prior to the falling edge of the /CS signal. If SCK begins in a high state, this effectively selects a different SPI mode that is not compatible with the FM25160.

Figure 1. Expected Timing Relationship
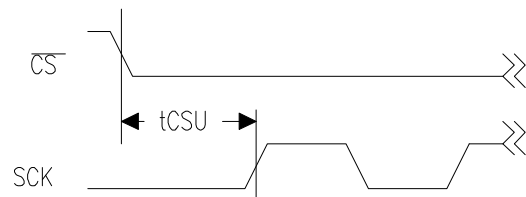
In the current data sheet, the timing parameter tCSU has a minimum value of 240 nS. This indicates that the chip select signal must fall at least 240 nS prior to the first rising edge. However the polarity relationship indicated by the figure must be satisfied

as well. As shown, the SCK must be low when the chip select falls and remain low for the tCSU period. After the falling edge of /CS, the SCK cannot start high, then go low and back high in order to produce the first rising edge. While this might satisfy the tCSU parameter it will cause improper operation. An example that will <u>not work</u> is shown in Figure 2.

Figure 2. Invalid Timing Relationship
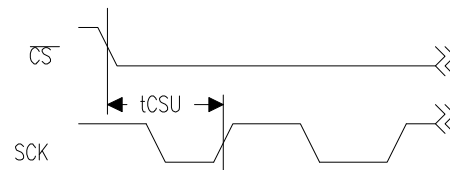
SPI Modes

The SPI bus protocol includes 4 modes. These modes determine the relationship between the serial clock and the data bits. Many common microcontrollers contain built-in hardware SPI ports. Some of these controllers make the SPI mode fully programmable, others allow a more limited selection. In order to have direct compatibility with the FM25160, the user should select mode 0. In the SPI configuration register (if any) for the controller, this requires setting the CPOL bit to 0 and the CPHA bit to 0. The four modes are illustrated below.

In some cases, users will be emulating the SPI protocol in software using general-purpose port pins. In this case, the software can be written to manipulate the port pins to achieve the correct relationship. The correct relationship is shown in the figure for Mode 0 below.

Note: in the case of a microcontroller host that has port pins with a default high state, it will be necessary to set the SCK pin to a low state manually prior to beginning a transaction.
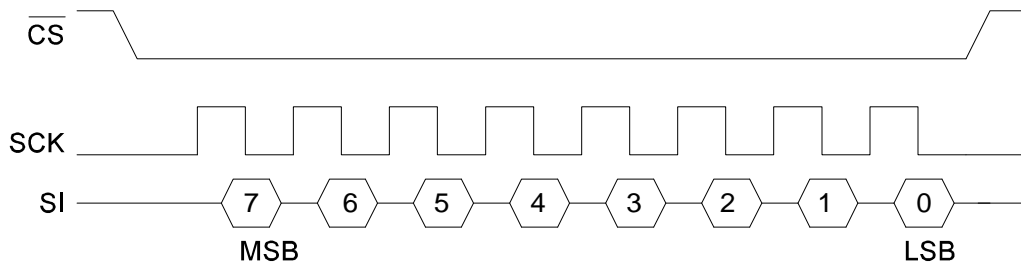
The desired relationship for mode 0 is illustrated below. In order to highlight the differences, modes 1-3 are also shown.
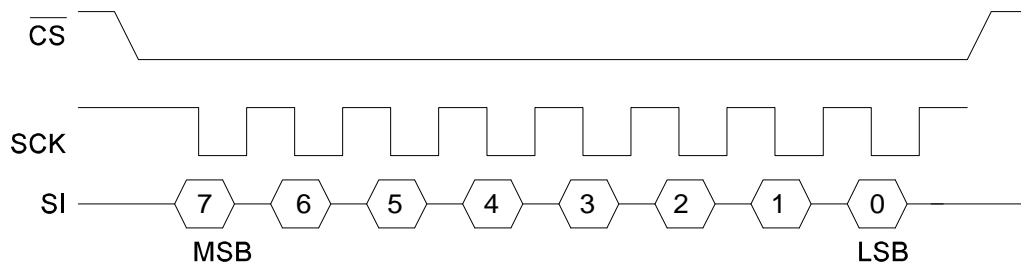
Figure 2. SPI Modes
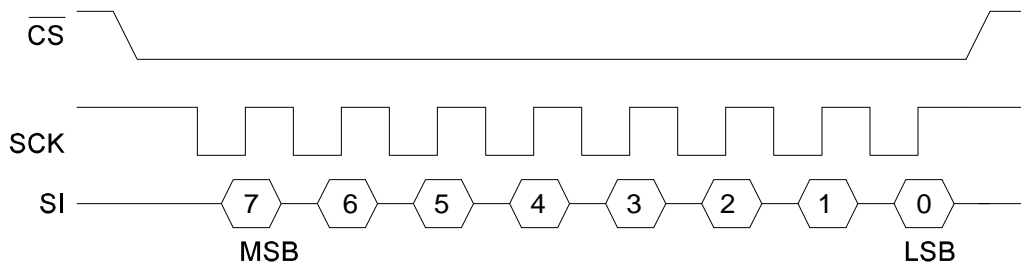
SPI Mode 0 : CPOL=0, CPHA=0
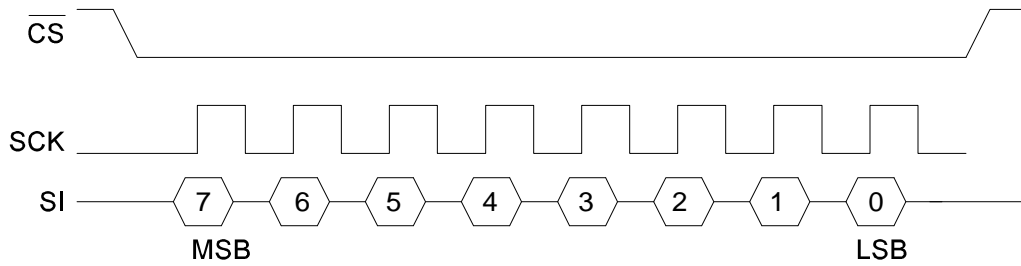
SPI Mode 1: CPOL=0, CPHA=1

SPI Mode 2 : CPOL=1, CPHA=0

SPI Mode 3 : CPOL=1, CPHA=1

Note: For all modes, SO is driven on the opposite edge. For example, if data input is latched on the rising edge, data output is driven on the falling edge.

Addressing

The address field for a 2Kx8 memory requires 11-bits. Address bits are shifted into the part MSB first. However the relative position of address bits for the FM25160 is different than certain other EEPROM-based serial memories. The FM25160 places the 3 upper address bits in the unused locations within the op-code word. The remaining 8-bits are grouped in an address byte that follows the op-code. By contrast, certain other memory devices leave the op-code bits as unassigned and include an additional address byte into the protocol. The result is that the FM25160 requires two bytes of overhead per new address, while other parts require three bytes per address. The addressing scheme of the FM25160 and a representative 16Kb SPI EEPROM are shown below.

Summary

When replacing a 2Kx8 SPI EEPROM with the FM25160, the designer should examine two issues. First is the SPI mode. If the old design used mode 0, then no change is needed. If the old design used mode 3, then the configuration should be altered accordingly.

For microcontrollers equipped with a hardware SPI port, the SPI configuration register should be set to CPOL=0, CPHA=0. For software implementations, the serial clock should idle in a low state and data should be clocked on the rising edge.

The relative location of the address MSB is the second issue. The FM25160 expects A10 to A8 in the op-code at bit locations 5 to 3 respectively. Existing implementations using 16Kb SPI EEPROMs most likely place these address bits within an address byte and program the op-code bits to 0. A minor code change will allow the upper 3 address bits to be included within the op-code and eliminate the upper address byte.

Note: The FM25040 4Kb SPI FRAM requires the same consideration for SPI mode but uses the same addressing scheme as other serial memories. In this case, all parts place the most significant address bit in the op-code.
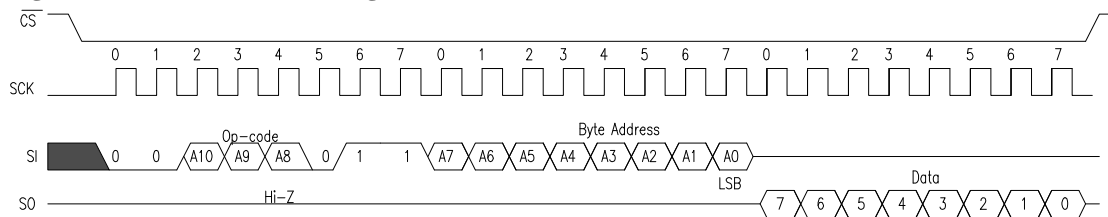
Figure 3A. FM25160 Addressing

Figure 3B. 16-bit EEPROM Addressing