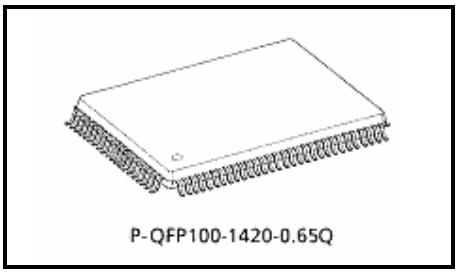
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC9325FG

Single-Chip DTS Microcontroller (DTS-20)

The TC9325FG is a single-chip digital tuning system (DTS) microcontroller incorporating a 230 MHz prescaler, PLL, and LCD driver. In addition to a 20-bit IF counter, an 8-channel, 8-bit AD converter, two types of serial interface, and buzzer function, the TC9325FG offers a range of functions required for DTS, including an interrupt function, an 8-bit timer-counter, and an 8-bit pulse counter. In addition, the LCD driver features six modes combining 1/4, 1/3, and 1/2 duty and 1/2 and 1/3 bias. This product is suitable for use in a wide variety of DTS systems, from automobile to home audio, including compact stereo systems.

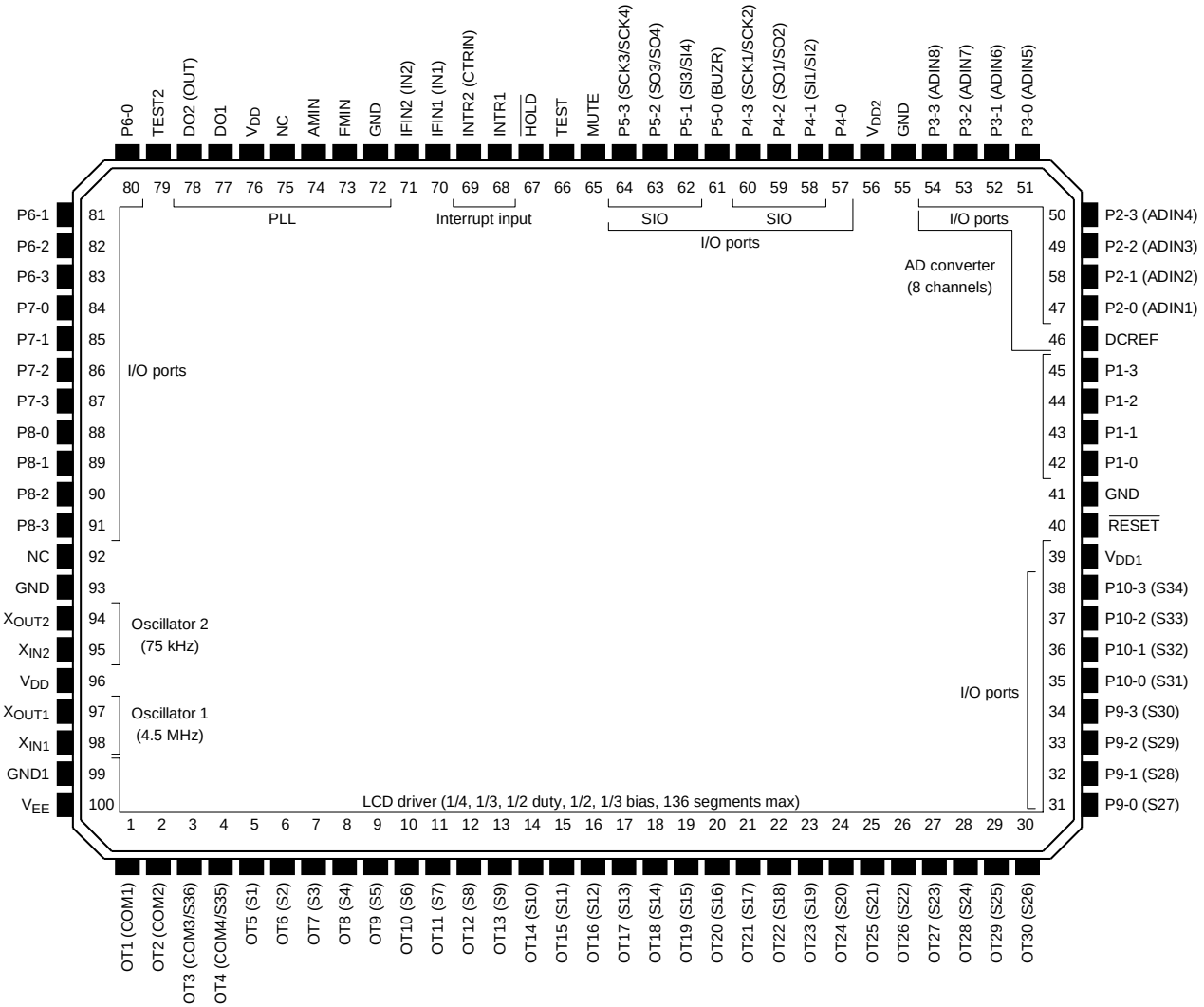


Weight: 1.6 g (typ.)

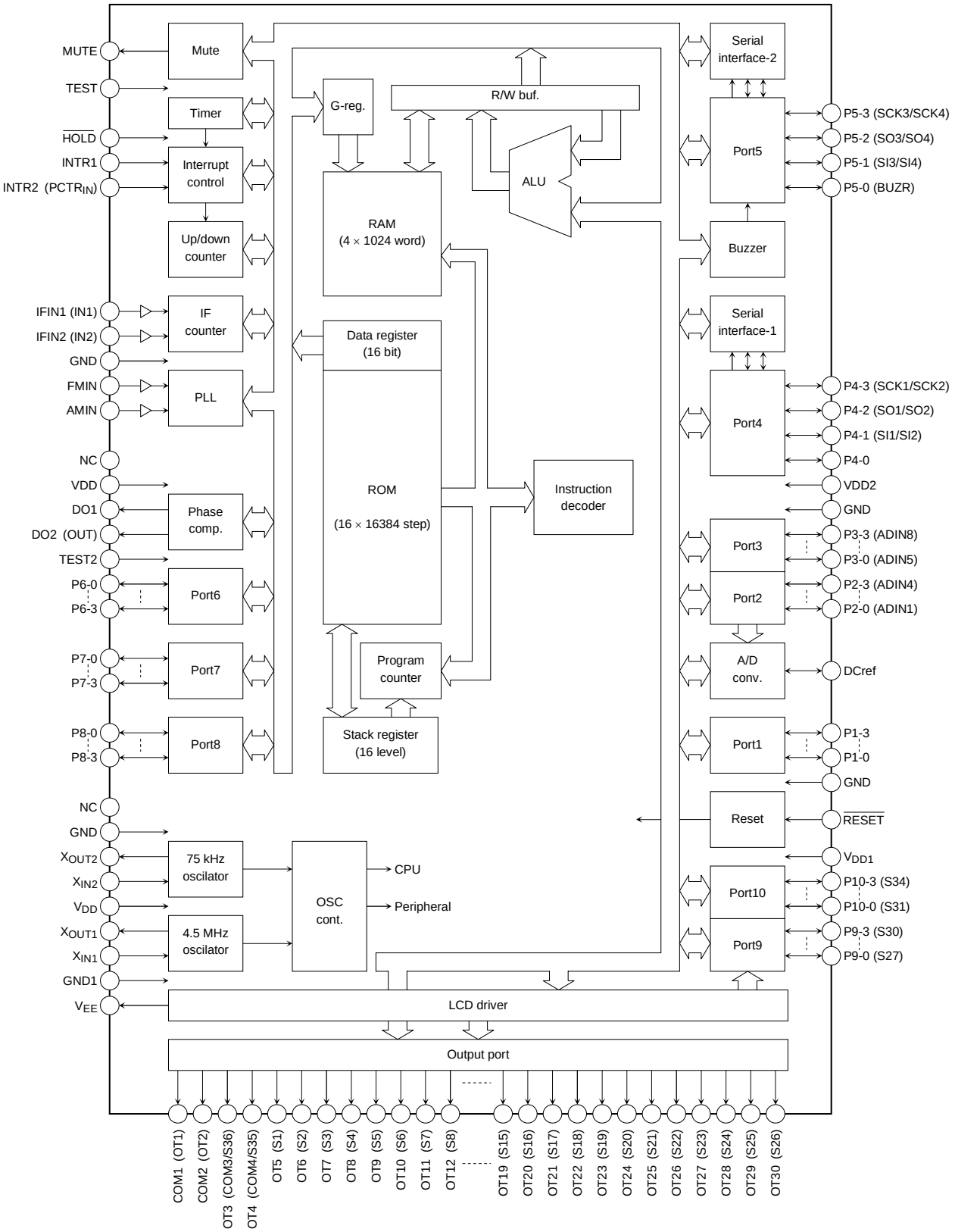
Features

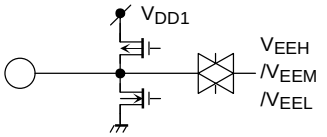
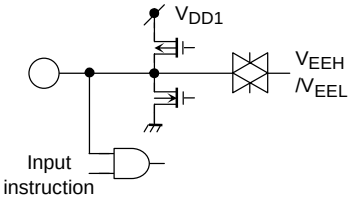
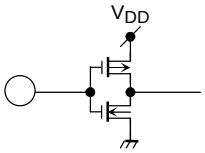
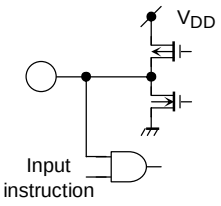
- CMOS DTS microcontroller LSI with built-in 230 MHz prescaler, PLL, and LCD driver
- Operating voltage: PLL operating: V_{DD} = 3.0 to 3.6 V (typ. 3.3 V)
  PLL off: V_{DD} = 3.0 to 3.6 V (when CPU only operating)
- Crystal oscillator frequency: 4.5 MHz, 75 kHz
- Current dissipation: PLL operating: I_{DD} = 3.5 mA (typ.) (crystal oscillator frequency 4.5 MHz, VHF mode)
  PLL off: I_{DD} = 1 mA (typ.) (crystal oscillator frequency 4.5 MHz, CPU only operating)
  PLL off: I_{DD} = 0.25 mA (typ.) (crystal oscillator frequency 75 kHz, CPU only operating)
- Operating temperature range: Ta = −40 to 85°C
- Program memory (ROM): 16 bits × 16,384 steps
- Data memory (RAM): 4 bits × 1,024 words
- Instruction execution time: 1.78 µs (crystal oscillator frequency 4.5 MHz)
  40 µs (crystal oscillator frequency 75 kHz)
- Stack levels: 16
- General-purpose IF counter: 20-bit (CMOS input supported)
- AD converter: 8 bits × 8 channels
- LCD driver: 1/4, 1/3, 1/2 duty, 1/2, 1/3 bias modes selectable, 136 segments maximum
- I/O ports: CMOS I/O ports: 40
  Output-only ports: Up to 31, input-only ports: Up to 5
- Timer-counter: 8-bit (as timer clock: INTR1, INTR2, instruction cycle, or 1 kHz selectable)
- Pulse counter: 8-bit up/down counter (input from INTR2 pin)
- Buzzer: 0.625 to 3 kHz (8 settings)
  Four modes: Continuous, Single-Shot, 10-Hz Intermittent, 10-Hz Intermittent at 1-Hz Intervals
- Interrupts: 2 external, 4 internal (three types of serial interface, 8-bit timer)
- Package: QFP-100 (0.65-mm pitch)

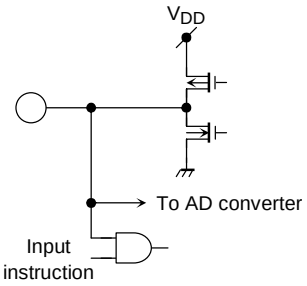
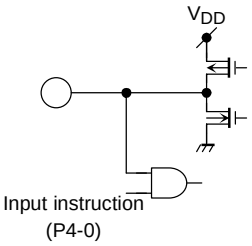
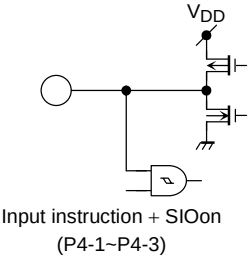
Pin Assignment

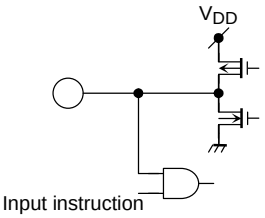
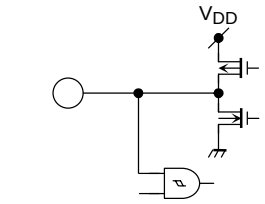
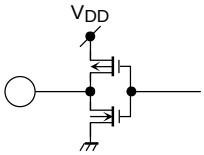
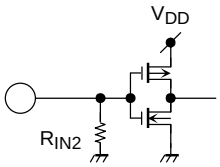


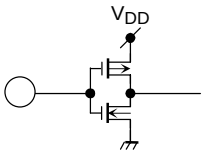
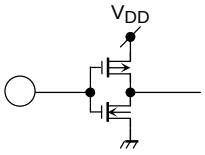
Block Diagram

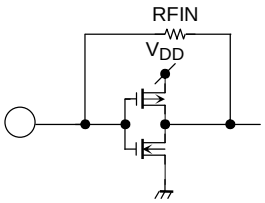
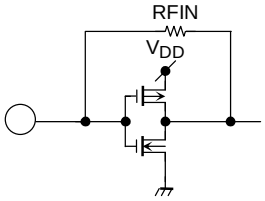
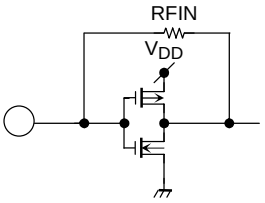


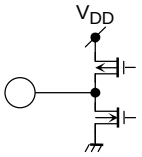
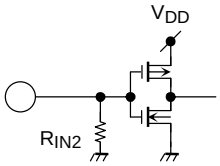
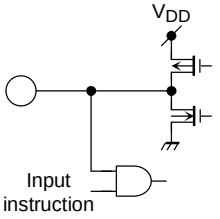
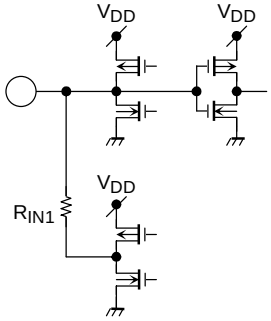
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
1	OT1/COM1	Output port /LCD common output	Output ports. Pins OT1 to OT20 can be incremented by software, allowing easy data access to external RAM/ROM. Can be set to LCD driver output by software. At 1/4 duty, controller can display up to 136 segments using a matrix consisting of COM1 to 4 and SEG1 to 34. At 1/3 duty, can display up to 105 segments using a matrix consisting of COM1 to 3 and SEG1 to 35. At 1/2 duty, can display up to 72 segments using a matrix consisting of COM1 to 2 and SEG1 to 36. Set to output ports after a system reset or clock stop.	
2	OT2/COM2			
3	OT3/COM3 /S36	Output port /LCD common output /LCD segment output		
4	OT4/COM4 /S35			
5~30	OT5/S1 ~ OT30/S26	Output port /LCD segment output		
31~34	P9-0/S27 ~ P9-3/S30	I/O port 9 /LCD segment output	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. These can be set bit by bit to LCD driver output by software. After a system reset, set to I/O port input. When a clock stop is executed, the pins used as the LCD driver must be set to output Low level (function as an I/O port).	
35~38	P10-0/S31 ~ P10-3/S34	I/O port 10 /LCD segment output		
40	$\overline{\text{RESET}}$	Reset input	Device's system reset signal input pin. Setting $\overline{\text{RESET}}$ to Low level triggers a reset. When the pin is set to High, the program starts from address 0. Since system reset will start if a voltage beyond 0 V to 3.5 V is supplied to V_{DD} pin, this pin is used fixed at High level.	
42~45	P1-0 ~ P1-3	I/O port 1	4-bit CMOS I/O port. Input and output can be programmed in 1-bit units.	

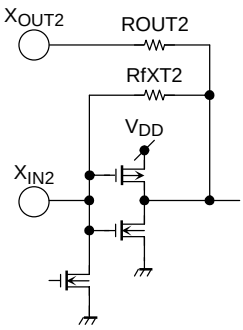
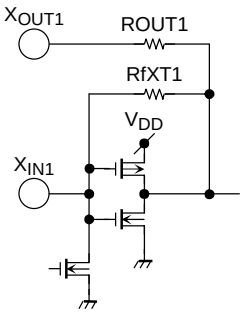
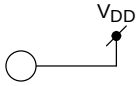
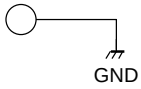
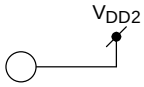
Pin No.	Symbol	Pin Name	Function and Operation	Remarks
46	DCREF	AD converter reference voltage input	AD converter reference voltage input pin. Normally apply V_{DD}.	
47~50	P2-0 /ADIN1 ~ P2-3 /ADIN4	I/O port 2 /A/D analog voltage input	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. Pins P2-0 to P3-3 are also used for the built-in 8-bit, 8-channel AD converter analog input. The built-in AD converter is a successive comparison system. When using a 4.5 MHz oscillator, the conversion clock can be selected from among 900 kHz, 100 kHz, and 50 kHz. When using a 75 kHz oscillator, the conversion clock is set to 75 kHz. The conversion times are respectively 23, 192, 382, and 294 μs. The necessary pins can be programmed to A/D analog input in 1-bit units. Voltage up to the V_{DD} can be input as the AD converter analog input voltage. Settings for the AD converter and its associated control can be performed by software.	
51~54	P3-0 /ADIN5 ~ P3-3 /ADIN8	I/O port 3 /A/D analog voltage input		
57	P4-0	I/O port 4	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. Pins P4-1 to P4-3 also input/output the two serial interface circuits (SIO1, SIO2). On the clock edge of the SCK1 pin, SIO1 can input 4-bit or 8-bit serial data to pin SI1 or input/output data to pin SO1. As the serial operating clock (SCK1), an internal (SCK = 37.5 kHz) or external clock can be selected, which can easily control various LSI, and communication between controllers. Enabling the SIO1 interrupt jumps the program to address 4 when SIO1 execution is complete. On the falling edge of the SCK2 pin, SIO2 can input 26-bit serial data to the SI2 pin. SIO2 incorporates a data detector. Enabling the SIO2 interrupt triggers the interrupt on the falling edge of the SCK2 pin and jumps the program to address 6. The SIO1 and SIO2 inputs all incorporate Schmitt circuits. SIO1 and SIO2 and their associated controls can be operated and set by software.	
58	P4-1 /SI1 /SI2	Serial data input 1 /Serial data input 2		
59	P4-2 /SO1 /SO2	Serial data input/output 1 /Serial data input 2		
60	P4-3 /SCK1 /SCK2	Serial clock input/output 1 /Serial clock input 2		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
61 62 63 64	P5-0/BUZR P5-1 /SI3 P5-2 /SO3 /SO4 P5-3 /SCK3 /SCK4	I/O port 5 /buzzer output /Serial data input 3 /Serial data input/output 3 /Serial data input/output 4 /Serial clock input/output 3 /Serial clock input/output 4	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units. Pin 5-0 is also used to output a buzzer signal. Pins P5-1 to P5-3 are also used to input/output the two serial interface circuits (SIO3, SIO4). The buzzer output can be selected from eight frequency settings (0.625 to 3 kHz), which can be output in four modes: Continuous, Single-Shot, 10 Hz-Intermittent, and 10-Hz Intermittent at 1-Hz Intervals. SIO3 is a serial interface supporting three lines, while the SIO4 serial interface supports two lines. On the clock edge of the SCK3/SCK4 pin, SIO3/SIO4 can input 4- or 8-bit serial data to pin SI3 or output data to the SO3/SO4 pin. As the serial operating clock (SCK3/SCK4), an internal (450/225/150/75 kHz) clock or external clock can be selected. Rising and falling shift can also be selected. The clock data output is N-channel open drain. This design facilitates LSI control and communication between controllers. Enabling the SIO3 or SIO4 interrupts triggers the interrupt and jumps the program to address 3 when interface SIO3 or SIO4 completes execution. This is effective for high-speed serial communications. The SIO3 and SIO4 inputs all incorporate Schmitt circuits. SIO3, SIO4, and their associated controls can be operated and set by software.	 Input instruction (P5-0)  Input instruction + SIOon (P5-1~P5-3)
65	MUTE	Muting output port	1-bit output port. Normally used as a muting control signal output. This pin can set the internal MUTE bit to 1 according to changes in the I/O port 8 input and $\overline{\text{HOLD}}$ input. The MUTE bit output logic can be changed.	
66	TEST	Test mode control input	Input pin for controlling Test mode. When the pins are at High level, the device is in Test mode; at Low level, in normal operation. Normally, set the pins to Low level or NC (pull-down resistors are incorporated).	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
67	$\overline{\text{HOLD}}$	Hold mode control input	Input pin for requesting and releasing Hold mode. Normally used to input radio mode selection or battery detection signals. Hold mode includes Clock Stop mode (crystal oscillator stopped) and Wait mode (CPU stopped), which can be set by the CKSTP and WAIT instructions respectively. Clock Stop mode can be entered by software in one of two ways: on command or when Low level is detected on the $\overline{\text{HOLD}}$ pin. Clock Stop mode can be released when High level is detected on the $\overline{\text{HOLD}}$ pin or when the input changes. Executing the CKSTP instruction stops the clock generator and CPU, entering memory backup mode. In this state the device is set to low current dissipation (10 μA max). Wait mode is executed, regardless of the $\overline{\text{HOLD}}$ pin input state, and the device is set to low current dissipation. To set wait mode, specify by software either crystal oscillator only operating or CPU suspended. Wait mode is released when the $\overline{\text{HOLD}}$ pin input changes.	
68 69	INTR1 INTR2 /PCTRin	External interrupt input /pulse count input	External interrupt input pins. Enabling the interrupt function and inputting a pulse (of at least 1.11 to 3.33 μs when the 4.5 MHz clock is in use, or at least 13.3 to 40 μs when the 75 kHz clock is used) to these input pins generates an interrupt (INTR1/2) and jumps the program to address 1/2. The input logic and the clock edge (rising/falling) can be individually selected for each interrupt input. The internal 8-bit timer clock can be selected as input to the pins. At the pulse count or when the count reaches a specified value, an interrupt can be generated (to address 5). These pins are also used to input an 8-bit pulse counter. This counter can be selected from either rising or falling edge input and either an up-counter or a down-counter. These pins are Schmitt inputs and can also be used as input ports. The pins can also be utilized as ports for inputting remote control signals or tape counts.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
70 71	IF_{IN1}/IN1 IF_{IN2}/IN2	IF signal inputs /input port	IF signal input pins for the IF counter to count the IF signals of the FM and AM bands and detect the automatic stop position. The input frequency is in the range 0.3 to 20 MHz. A built-in input amp and capacitive coupling support low-amplitude operation. The IF counter is a 20-bit counter with selectable gate times of 1, 4, 16, and 64 ms. 20 bits of data can be easily stored in memory. In Manual mode, the gates can be switched on and off by instruction. These input pins can also be programmed as an input port (IN port). At that time, they become CMOS inputs and the clocks of those inputs can be counted using the IF counter. Note: Pins set as IF input go Low in PLL Off mode.	
73	FMIN	FM local oscillation signal input	Programmable counter input pins for the FM/AM band. Their input mode can be switched by software from either 1/2 + pulse swallow (VHF/FM) mode for FM input, or pulse swallow (HF) or direct division (LF) mode for AM input. The local oscillation output (voltage-controlled oscillator or V_{CO} output) is normally input at the following frequencies: 50 to 230 MHz in VHF mode, 50 to 140 MHz in FM1 mode, 10 to 60 MHz in FM2 mode, 1 to 30 MHz in HF mode, and 0.5 to 20 MHz in LF mode. A built-in input amp and capacitive coupling support low-amplitude operation. Note: In PLL Off mode or when the pins are not set for input, the input goes to high impedance.	
74	AMIN	AM local oscillation signal input		

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
77 78	DO1 DO2/OUT	Phase comparator output /output port	PLL phase comparator output pins. In tri-state output, when the programmable counter divider output is higher than the reference frequency, the pins output High level; when the output is lower than the reference frequency, the pins output Low level. When the outputs match, the pins go to high impedance. Because DO1 and DO2 are output in parallel, optimal filter constants can be designed for both the AM and FM bands. The DO2 pin can be programmed to high impedance or set as an output port (OUT). Therefore, lockup time can be improved using the DO1 and DO2 pins or the pins can be effectively used as output ports. Lock-up time can also be improved by using DO1 and DO2 together by setting the pins to High-Speed Lock mode when using a 4.5 MHz oscillator. When the phase difference equals or exceeds ±1.11 μs, DO1 and DO2 output the phase difference pulse. When the phase difference is less than ±1.11 μs, the DO2 output goes to high impedance and only DO1 outputs the phase difference pulse.	
79	TEST2	Test mode control input 2	Input pin for controlling Test mode. When the pins are at High level, the device is in Test mode; at Low level, in normal operation. Normally, set the pins to Low level or NC (pull-down resistors are incorporated).	
80~83	P6-0 ι P6-3	I/O port 6	4-bit CMOS I/O ports. Input and output can be programmed in 1-bit units.	
84~87	P7-0 ι P7-3	I/O port 7		
88~91	P8-0 ι P8-3	I/O port 8	4-bit CMOS I/O port. Input and output can be programmed in 1-bit units. As the pins can be pulled up or pulled down by software they can be used as key input pins. When set to an I/O port input, that input can be varied to release Clock Stop or Wait modes or to set the MUTE bit of the MUTE pin to 1.	

Pin No.	Symbol	Pin Name	Function and Operation	Remarks
94	X_{OUT2}	75 kHz crystal oscillator pins	Crystal oscillator pins. Connect a 4.5 MHz crystal (Ci = Co = 30 pF typ.) to X_{IN1} and X_{OUT1} and a 75 kHz crystal (Ci = Co = 30 pF typ.) to X_{IN2} and X_{OUT2}. Two different types of crystal resonators (4.5 MHz and 75 kHz) can be connected, or simply connect one (either 4.5 MHz or 75 kHz). Note that if a 75 kHz crystal only is connected, X_{IN1} must be fixed to GND level. If both 4.5 MHz and 75 kHz crystal oscillators are connected, after a reset the CPU operates on the 4.5 MHz crystal oscillator clock. The clock can be readily switched by software between the CPU operating clock and the peripheral clock. Oscillation stops during execution of the CKSTP instruction.	
95	X_{IN2}			
97	X_{OUT1}	4.5 MHz crystal oscillator pins		
98	XIN1			
100	V_{EE}	LCD driver bias voltage output pin	This is the bias voltage output pin for the LCD driver.	—
76 96	V_{DD}	Power supply pins	Pins used for supplying power. The pins supply V_{DD} = 3.0 to 3.6 V. In backup state (on execution of the CKSTP instruction), current dissipation becomes low (10 μA max), reducing the power supply voltage to 2.0 V. If 3.0 V or more is applied to these pins when the voltage is 0 V, a system reset is applied to the device and the program starts from address 0 (power-on reset). Note: To operate the power-on reset, allow 10 to 100 ms while the device power supply voltage rises.	
41 55 72 93	GND			
39	V_{DD1}			
99	GND1			
56	V_{DD2}	Power supply pins For I/O Port4,5	Pins used for supplying power for I/O port 4,5.The pins supply $V_{DD} = V_{DD}$ to 5.5 V.	
72 93	NC	No connection	No connection	

Description of Operations

○ CPU

The CPU consists of a program counter, a stack register, an ALU, program memory, data memory, a G-register, a data register, a DAL address register, a carry flip-flop (F/F), a judge circuit, and an interrupt circuit.

1. Program Counter (PC)

The program counter is a 14-bit binary up counter used to address program memory (ROM). The program counter is cleared by a system reset and starts from address 0.

The PC is normally incremented by 1 at the execution of each instruction. However, executing a Jump or Call instruction loads the address specified in the instruction's operand to the PC.

When an instruction with a skip function (for example, the AIS, SLTI, TMT, and RNS instructions) is executed and the result matches the skip condition, the PC is incremented by 2 and the next instruction is skipped.

When an interrupt is received, the system loads the vector address corresponding to the interrupt.

Note: Program memory (ROM) uses the address range 0000H to 3FFFH. Access to addresses outside this range is prohibited.

Instruction	Contents of Program Counter (PC)													
	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
JUMP ADDR1	← Instruction operand (ADDR1) →													
CALL ADDR2	0	0	← Instruction operand (ADDR2) →											
DAL ADDR3, (r) (DAL bit = 0)	0	0	0	0	← Instruction operand (ADDR3) →						← Contents of general register (r) →			
DAL (DA) (DAL bit = 1)	← DAL address register (DA) →													
RN, RNS, RNI	← Contents of stack register →													
When interrupt received	← Vector address for interrupt →													
Power-on reset, reset by RESET pin	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Priority	Interrupt Source	Vector Address
1	INTR1 pin	0001H
2	INTR2 pin	0002H
3	Serial interface 1	0003H
4	Serial interface 3/4	0004H
5	Timer-counter	0005H
6	Serial interface 2	0006H

2. Stack Register

The stack register consists of 16 × 14 bits. When a subroutine call instruction is executed or an interrupt is processed, this register stores a value equal to the contents of the program counter + 1 (that is, the return address). Executing a return instruction (RN, RNS, RNI) loads the contents of the stack register to the program counter.

The stack register can nest to 16 stack levels.

3. ALU

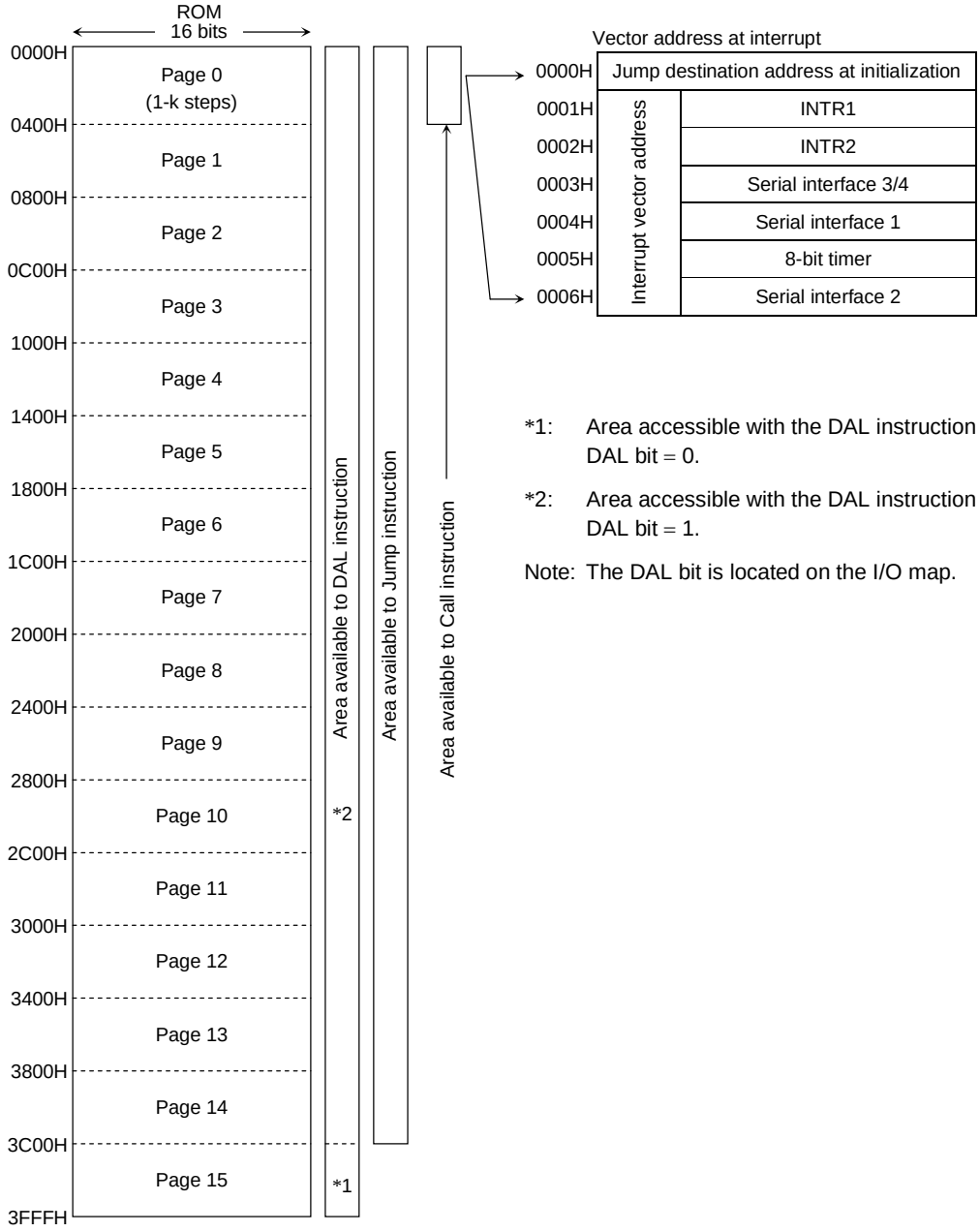
The arithmetic and logic unit (ALU) has a binary 4-bit parallel addition-subtraction function, a logical operation function, a compare function, and a multiple bit judge function. The CPU does not include an accumulator; all operations directly use the contents of the data memory.

4. Program Memory (ROM)

Program memory, which stores the program, is made up of 16 bits × 16,384 steps. The useable address range is the 16,384 steps of the range 0000H to 3FFFH.

The program memory divides the 16,384 steps into 16 pages (pages 0 to 15). The address area available to Jump instructions is from 0000H to 3BFFH (pages 0 to 14). The area for Call instructions is 0000H to 03FFH (page 0). When the DAL bit (located in the I/O map) is set to 0 (DAL ADDR3, (r) instruction), area 3C00H to 3FFFH (page 15) of program memory can be used as data area. When the DAL bit is set to 1 (DAL (DA) instruction) the area 0000H to 3FFFH (pages 0 to 7) is available as data area. At that time the DAL instruction can load any 16 bits within the data area to the data register.

Note: Set the data area in program memory to addresses outside the program loop.



*1: Area accessible with the DAL instruction when DAL bit = 0.

*2: Area accessible with the DAL instruction when DAL bit = 1.

Note: The DAL bit is located on the I/O map.

5. Data Memory (RAM)

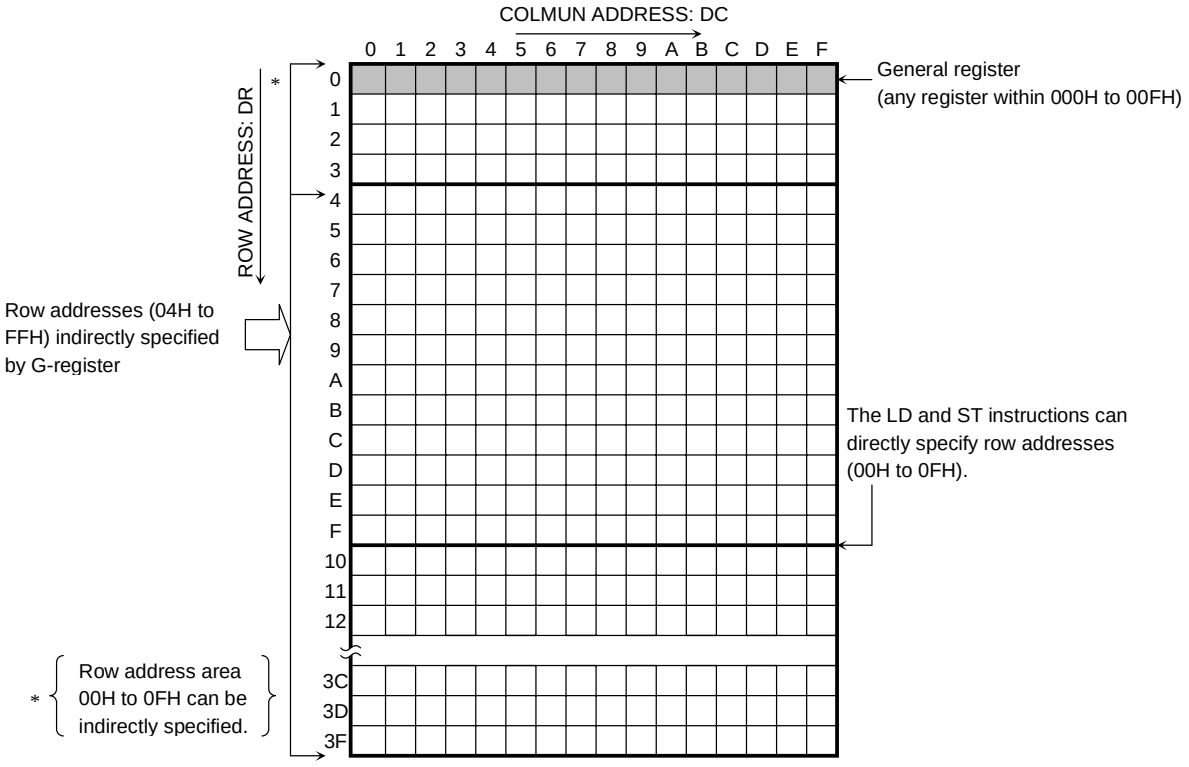
Data memory, which stores the data, is made up of 4 bits x 1,024 words. The 1,024 words are identified by a row address (8 bits) and a column address (4 bits). 1,020 words (row address = 04H to 3FH) are for indirect addressing by the G-register. Accordingly, when processing data in this area be sure to first set the G-register to specify the row address.

Data memory areas 00H to 0FH are called the general registers and can be used simply by specifying the (4 bits) column address. The 16 general registers can be used in data memory operations and transfers. The general registers can also be used as normal data memory.

Note: The (4 bits) column address specifying the general register is used as the general register's register number.

Note: All row addresses (00H to 3FH) can be indirectly specified by the G-register.

Note: The LD and ST instructions can directly address 256 words of data memory (row address area 00H to 0FH).



6. G-register (G-REG)

The G-register is an 8-bit register for addressing the 1,024 words of row address in data memory (row address = 04H to 3FH).

The MVGD or MVGS instruction validates the contents of the G-register. Other instructions have no effect. The G-register is treated as a port. OUT1, an I/O instruction, sets the contents of the G-register. (See the section on register ports.)

The STIG instruction can also be used to set directly 8-bit content in the G-register.

7. Data Register (DATA REG)

This register, which consists of 1 × 16 bits, is loaded with 16 bits of data from anywhere in program memory on execution of the DAL instruction. The data register is treated as a port. Executing I/O instruction IN1 reads the contents of the register to data memory using four bits. (See the section on register ports.)

This register, which can also be written from data memory, can be used for saving and restoring data when an interrupt occurs.

8. DAL Address Register (DA)

This register consists of 1 × 14 bits. Executing the DAL instruction with the DAL bit set to 1 loads 16 bits of data from any program memory address specified by the DAL address register. Setting the (DATA) → DA bit to 1 transfers the contents of the data register (DATA REG) to the DAL address register (DA). This register and its control bit are treated as a port and can be accessed by the IN3/OUT3 I/O instruction. (See the section on register ports.)

9. Carry F/F (Ca Flag)

This F/F is set when a Carry or Borrow occurs as the result of an arithmetic instruction. When a Carry or Borrow does not occur the F/F is reset.

The contents of the Carry F/F change only on execution of an addition/subtraction, CLT, or CLTC instruction. The contents are not affected by the execution of any other instruction.

The Carry F/F can also be accessed by the IN1/OUT1 I/O instruction. Accordingly, an I/O instruction is used to save and restore data in data memory at an interrupt. (See the section on register ports.)

10. Judge Circuit (J)

This circuit is used to determine the skip condition when an instruction with a skip function is executed. If the skip condition is satisfied, the program counter is incremented by 2 and the next instruction is skipped.

A total of 15 instructions have skip functions. (See instructions with the * symbol in the list of instruction functions and operations in 11.)

11. Interrupt Circuit

The interrupt circuit branches to various vector addresses in response to demands from peripheral hardware and handles interrupts. (See the section on interrupt functions.)

12. Instruction Set List

The TC9325FG has a total of 57 instruction sets, all using one-word instructions. These instructions use 6-bit instruction code.

Upper 2 bits / Lower 4 bits		00		01		10	11	
		0		1		2	3	
0000	0	AI	M, I	TMTR	r, M		SLTI	M, I
0001	1	AIC	M, I	TMFR	r, M		SGEI	M, I
0010	2	SI	M, I	SEQ	r, M		SEQI	M, I
0011	3	SIB	M, I	SNE	r, M		SNEI	M, I
0100	4	ORIM	M, I	LD	r, M*		TMTN	M, N
0101	5	ANIM	M, I				TMT	M, N
0110	6	XORIM	M, I				TMFN	M, N
0111	7	MVIM	M, I			JUMP ADDR1	TMF	M, N
1000	8	AD	r, M	ST	M*, r		IN1	M, C
1001	9	AC	r, M				IN2	M, C
1010	A	SU	r, M				IN3	M, C
1011	B	SB	r, M				OUT1	M, C
1100	C	ORR	r, M	CLT	r, M		OUT2	M, C
1101	D	ANDR	r, M	CLTC	r, M		OUT3	M, C
1110	E	XORR	r, M	MVGD	r, M		DAL	ADDR3, r
1111	F	MVSR	M1, M2	MVGS	M, r	CAL ADDR2	SHRC RORC STIG SKP, SKPN RN, RNS WAIT CKSTP XCH DI, EI, RNI NOOP	M M I* P M

13. List of Instruction Functions and Operations

(Description of symbols in list)

M	; Data memory address Normally, an address in the data memory range 000H to 01FH.
M*	; Data memory address (1,024 words) An address in the data memory range 000H to 3FFH. (Valid only at ST, LD instruction execution)
r	; General register An address in the data memory range 000H to 00FH.
PC	; Program counter (14 bits)
STACK	; Stack register (14 bits)
G	; G-register (8 bits)
DATA	; Data register (16 bits)
I	; Immediate data (4 bits)
I*	; Immediate data (6 bits; valid only at execution of STIG instruction)
N	; Bit position (4 bits)
–	; All 0
C	; Code number of port (4 bits)
CN	; Code number of port (4 bits)
RN	; General register No. (4 bits)
ADDR1	; Program memory address (14 bits)
ADDR2	; Program memory address in page 0 (10 bits)
ADDR3	; Upper 6 bits of program memory address in page 0
DA	; DAL address register (14 bits, valid only at execution of DAL instruction when DAL bit set to 1)
Ca	; Carry
CY	; Carry flag
P	; Wait condition
b	; Borrow
IN1~IN3	; IN1 to IN3: The ports used at IN1 to IN3 instruction execution
OUT1 to OUT3	; The ports used at OUT1 to OUT3 instruction execution
( )	; Contents of registers or data memory
[ ] C	; Contents of the port indicated by code No. C (4 bits)
[ ]	; Contents of data memory indicated by the register or data memory
[ ] P	; Contents of program memory (16 bits)
IC	; Instruction code (6 bits)
*	; Instruction with skip function
DC	; Data memory column address (4 bits)
DR	; Data memory row address (4 bits)
DR*	; Data memory row address (4 bits, valid only at execution of ST or LD instruction)
(M) b0 to (M) b3	; Bit data of data memory contents (1 bit)

Inst-ruction Set	Mnemonic		Skip Func-tion	Description	Operation	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Addition instruction	AI	M, I		Add immediate data to memory	M ← (M) + I	000000	DR	DC	I
	AIC	M, I		Add immediate data to memory with carry	M ← (M) + I + ca	000001	DR	DC	I
	AD	r, M		Add memory to general register	r ← (r) + (M)	001000	DR	DC	RN
	AC	r, M		Add memory to general register with carry	r ← (r) + (M) + ca	001001	DR	DC	RN
Subtraction instruction	SI	M, I		Subtract immediate data from memory	M ← (M) − I	000010	DR	DC	I
	SIB	M, I		Subtract immediate data from memory with borrow	M ← (M) − I − b	000011	DR	DC	I
	SU	r, M		Subtract memory from general register	r ← (r) − (M)	001010	DR	DC	RN
	SB	r, M		Subtract memory from general register with borrow	r ← (r) − (M) − b	001011	DR	DC	RN
Compare instruction	SLTI	M, I	*	Skip if memory is less than immediate data	Skip if (M) < I	110000	DR	DC	I
	SGEI	M, I	*	Skip if memory is greater than or equal to immediate data	Skip if (M) ≧ I	110001	DR	DC	I
	SEQI	M, I	*	Skip if memory is equal to immediate data	Skip if (M) = I	110010	DR	DC	I
	SNEI	M, I	*	Skip if memory is not equal to immediate data	Skip if (M) ≠ I	110011	DR	DC	I
	SEQ	r, M	*	Skip if general register is equal to memory	Skip if (r) = (M)	010010	DR	DC	RN
	SNE	r, M	*	Skip if general register is not equal to memory	Skip if (r) ≠ (M)	010011	DR	DC	RN
	CLT	r, M		Set carry flag if general register is less than memory, or reset if not	(CY) ← 1 if (r) < (M) or (CY) ← 0 if (r) ≧ (M)	011100	DR	DC	RN
	CLTC	r, M		Set carry flag if general register is less than memory with carry or reset if not	(CY) ← 1 if (r) < (M) + (ca) or (CY) ← 0 if (r) ≧ (M) + (Ca)	011101	DR	DC	RN

Inst-ruction Set	Mnemonic		Skip Func-tion	Description	Operation	Machine Language (16 bits)			
						IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Transfer instruction	LD	r, M*		Load memory to general register	r ← (M*)	0101	DR* (4 bits)	DC	RN
	ST	M*, r		Store memory to general register	M* ← (r)	0110	DR* (4 bits)	DC	RN
	MVSR	M1, M2		Move memory to memory in same row	(DR, DC1) ← (DR, DC2)	001111	DR	DC1	DC2
	MVIM	M, I		Move immediate data to memory	M ← I	000111	DR	DC	I
	MVGD	r, M		Move memory to destination memory referring to G-register and general register	[(G), (r)] ← (M)	011110	DR	DC	RN
	MVGS	M, r		Move source memory referring to G-register and general register to memory (Note)	(M) ← [(G), (r)]	011111	DR	DC	RN
	STIG	I*		Move immediate data to G-register	G ← I*	111111	I*		0010
I/O instruction	IN1	M, C		Input IN1 port data to memory	M ← [IN1] C	111000	DR	DC	CN
	OUT1	M, C		Output contents of memory to OUT1 port	[OUT1] C ← (M)	111011	DR	DC	CN
	IN2	M, C		Input IN2 port data to memory	M ← [IN2] C	111001	DR	DC	CN
	OUT2	M, C		Output contents of memory to OUT2 port	[OUT2] C ← (M)	111100	DR	DC	CN
	IN3	M, C		Input IN3 port data to memory	M ← [IN3] C	111010	DR	DC	CN
	OUT3	M, C		Output contents of memory to OUT3 port	[OUT3] C ← (M)	111101	DR	DC	CN
Logical operation instruction	ORR	r, M		Logical OR of general register and memory	r ← (r) ∨ (M)	001100	DR	DC	RN
	ANDR	r, M		Logical AND of general register and memory	r ← (r) ∧ (M)	001101	DR	DC	RN
	ORIM	M, I		Logical OR of memory and immediate data	M ← (M) ∨ I	000100	DR	DC	I
	ANIM	M, I		Logical AND of memory and immediate data	M ← (M) ∧ I	000101	DR	DC	I
	XORIM	M, I		Logical exclusive OR of memory and immediate data	M ← (M) ∀ I	000110	DR	DC	I
	XORR	r, M		Logical exclusive OR of general register and memory	r ← (r) ∀ (M)	001110	DR	DC	RN

Note: The MVGS instruction execution time is two machine cycles.

Inst-ruction Set	Mnemonic	Skip Func-tion	Description	Operation	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Bit judge instruction	TMTR r, M	*	Test general register bits by memory bits, then skip if all bits specified are true	Skip if r [N (M)] = all "1"	010000	DR	DC	RN
	TMFR r, M	*	Test general register bits by memory bits, then skip if all bits specified are false	Skip if r [N (M)] = all "0"	010001	DR	DC	RN
	TMT M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = all "1"	110101	DR	DC	N
	TMF M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = all "0"	110111	DR	DC	N
	TMTN M, N	*	Test memory bits, then skip if all bits specified are true	Skip if M (N) = not all "1"	110100	DR	DC	N
	TMFN M, N	*	Test memory bits, then not skip if all bits specified are false	Skip if M (N) = not all "0"	110110	DR	DC	N
	SKP	*	Skip if carry flag is true	Skip if (CY) = 1	111111	00	—	0011
	SKPN	*	Skip if carry flag is false	Skip if (CY) = 0	111111	01	—	0011
Subroutine instruction	CALL ADDR2		Call subroutine	STACK ← (PC) + 1 and PC ← ADDR2	101111	ADDR2 (10 bits)		
	RN		Return to main routine	PC ← (STACK)	111111	10	—	0011
	RNS		Return to main routine and skip unconditionally	PC ← (STACK) and skip	111111	11	—	0011
Jump instruction	JUMP ADDR1		Jump to address specified	PC ← ADDR1	10	ADDR1 (14 bits) (excluding 3C00H to 3FFFH)		
Interrupt instruction	DI		Reset IMF (Note)	IMF ← 0	111111	00	—	0111
	EI		Set IMF (Note)	IMF ← 1	111111	01	—	0111
	RNI		Return to main routine and set IMF (Note)	PC ← (STACK) IMF ← 1	111111	11	—	0111

Note: The IMF bit is an interrupt master enable flag located on the I/O map. (See the section on interrupt functions.)

Inst-ruction Set	Mnemonic	Skip Func-tion	Description	Operation	Machine Language (16 bits)			
					IC (6 bits)	A (2 bits)	B (4 bits)	C (4 bits)
Other instructions	SHRC M		Shift memory bits to right direction with carry	0 → (M) b3 → (M) b2 → (M) b1 → (M) b0→ (CY)	111111	DR	DC	0000
	RORC M		Rotate memory bits to right direction with carry	→ (M) b3 → (M) b2 → (M) b1→ (M) b0 → (CY)	111111	DR	DC	0001
	XCH M		Exchange memory bits mutually	(M) b3 ↔ (M) b0, (M) b2 ↔ (M) b1	111111	DR	DC	0110
	DAL ADDR3, r		IF DAL bit = 0 then load program in page 0 to DATA register. (Note)	DATA ← [ADDR3 + (r)] p in page 0	111110	ADDR3 (6 bits)		RN
	WAIT P		At P = "0" H, the condition is CPU waiting (soft wait mode) At P = "1" H, expect for clock generator, all function is waiting (hard wait mode)	Wait at condition P	111111	P	—	0100
	CKSTP		Clock generator stop	Stop clock generator to MODE condition	111111	—	—	0101
	NOOP		No operation	—	111111	—	—	1111

Note: The lower 4 bits of the 10 bits of program memory specified by the DAL instruction (DAL ADDR3r) are used for indirectly addressing the contents of the general registers.

Note: The DAL instruction execution time is two machine cycles.

Note: The DAL bit and the DAL address register (DA) are located on the I/O map. (See the section on register ports.)

Note: Executing the DAL instruction with the DAL bit set to 1 invalidates the operand. At this time the DAL address register (DA) is used for all the addresses to reference. To specify 0, 0 to be operand parts as dummy data at this time.

○ I/O Map

All the ports in the device are accessed by six I/O instructions (OUT1 to 3 and IN1 to 3) and 4-bit code number matrices.

The following pages show the port allocations as an I/O map. On the I/O map, the ports used by I/O instructions are in horizontal positions and the port code numbers are in vertical positions. The G-register, data register, DAL address register, and DAL bit are treated as ports.

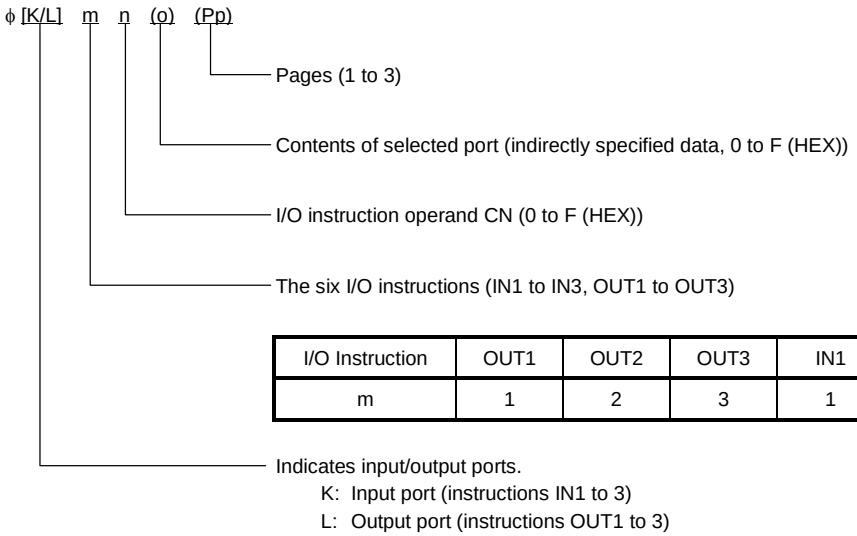
The OUT1 to 3 instructions specify output ports. The IN1 to 3 instructions specify input ports.

Note: The diagonal lines on the I/O map indicate ports that do not exist in the device. Executing an output instruction to output data to a non-existent output port has no effect on other ports or on data memory contents.
When a non-existent input port is specified by an input instruction, all the content read to the data memory is undefined.

Note: Output ports indicated by an asterisk (*) on the I/O map are unused ports. Any data output to these ports are “don’t care”.

Note: The contents of the ports are represented by four bits where Y1 corresponds to the lowest bit of the data in data memory, and Y8 to the highest bit.

The ports specified by the six input/output instructions and by code No. C are represented in this document by the following notation.



I/O Instruction	OUT1	OUT2	OUT3	IN1	IN2	IN3
m	1	2	3	1	2	3

Example: The G-register is set by the OUT1 instruction with codes C and D. Therefore, the notation is ϕL1C and ϕL1D.

I/O Map (IN1 (M, C), IN2 (M, C), IN3 (M, C), OUT1 (M, C), OUT2 (M, C), OUT3 (M, C))

Page 1	ϕL1				ϕL2				ϕL3				ϕK1				ϕK2				ϕK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	HF	PW	*	FM	I/O control 1				I/O port 1				IF monitor			0	SI02 decode data				I/O port 1			
					-0	-1	-2	-3	-0	-1	-2	-3	BUSY	MANUAL	OVER		DCD0	DCD1	DCD2	DCD3	-0	-1	-2	-3
1	Programmable counter 1				I/O control 2				I/O port 2				IF data 1				SI02 information data 1				I/O port 2			
	P0	P1	P2	P3	-0	-1	-2	-3	-0	-1	-2	-3	F0	F1	F2	F3	INF0	INF1	INF2	INF3	-0	-1	-2	-3
2	Programmable counter 2				I/O control 3				I/O port 3				IF data 2				SI02 information data 2				I/O port 3			
	P4	P5	P6	P7	-0	-1	-2	-3	-0	-1	-2	-3	F4	F5	F6	F7	INF4	INF5	INF6	INF7	-0	-1	-2	-3
3	Programmable counter 3				I/O control 4				I/O port 4				IF data 3				SI02 information data 3				I/O port 4			
	P8	P9	P10	P11	-0	-1	-2	-3	-0	-1	-2	-3	F8	F9	F10	F11	INF8	INF9	INF10	INF11	-0	-1	-2	-3
4	Programmable counter 4				I/O control 5				I/O port 5				IF data 4				SI02 information data 4				I/O port 5			
	P12	P13	P14	P15	-0	-1	-2	-3	-0	-1	-2	-3	F12	F13	F14	F15	INF12	INF13	INF14	INF15	-0	-1	-2	-3
5	Programmable counter 4				I/O control 6				I/O port 6				IF data 5				SI02 offset/check data 1				I/O port 6			
	P16	*	*	*	-0	-1	-2	-3	-0	-1	-2	-3	F16	F17	F18	F19	OFS0/ CHK0	OFS1/ CHK1	OFS2/ CHK2	OFS3/ CHK3	-0	-1	-2	-3
6	Reference select				I/O control 7				I/O port 7								SI02 offset/check data 2				I/O port 7			
	R0	R1	R2	P3	-0	-1	-2	-3	-0	-1	-2	-3					OFS4/ CHK4	OFS5/ CHK5	OFS6/ CHK6	OFS7/ CHK7	-0	-1	-2	-3
7	I/F counter control 1				I/O control 8				I/O port 8								SI02 offset/check data 2				I/O port 8			
	IF1/$\overline{IF2}$	*	IF1/$\overline{IN1}$	IF2/$\overline{IN2}$	-0	-1	-2	-3	-0	-1	-2	-3					OFS8/ CHK8	OFS9/ CHK9	0	0	-0	-1	-2	-3
8	I/F counter control 2				I/O control 9				I/O port 9								HOLD	INTR1	INTR2	STOP F/F	I/O port 9			
	STA/$\overline{STP}$	MANUAL	G0	G1	-0	-1	-2	-3	-0	-1	-2	-3									-0	-1	-2	-3
9	MUTE	Mute control			I/O control 10				I/O port 10								MUTE	Mute control			I/O port 10			
		I/O-8	POL	HOLD	-0	-1	-2	-3	-0	-1	-2	-3						IO1	POL	HOLD	-0	-1	-2	-3
A	Unlock detect	D02 control			I/O port 8 pulled down				DAL	(DATA) → DA	OT Count Up	I/O port 8 pulled up					Unlock detect		Input port		DAL	0	0	0
	RESET	PN	M0	M1	-0	-1	-2	-3									F/F	ENA	IN1	IN2				
B	CA flag	*	*	*	Data selection				DAL address/pulse counter control				CA flag	0	0	0	Data selection				DAL address			
					S1	S2	S4	S8	DA0	DA1	DA2	DA3					S1	S2	S4	S8	DA0	DA1	DA2	DA3
C	G-register 1				General-purpose output data/serial interface output data/segment I/O control				Data register 1				G-register 1								Data register 1			
	G0	G1	G2	G3	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	d0	d1	d2	d3	G0	G1	G2	G3					d0	d1	d2	d3
D	G-register 2				Segment data 1				Data register 2				G-register 2								Data register 2			
	G4	G5	G6	G7	COM1	COM2	COM3	COM4	d4	d5	d6	d7	G4	G5	G6	G7					d4	d5	d6	d7
E	Test port 1				Segment data 2				Data register 3												Data register 3			
	#0	#1	#2	#3	COM1	COM2	COM3	COM4	d8	d9	d10	d11									d8	d9	d10	d11
F	Page		*	Test port 2	Segment data 3/LCD driver control				Data register 4				Page		0	0	Timer				Data register 4			
	Page 2	Page 3		#4	COM1	COM2	COM3	COM4	d12	d13	d14	d15	Page 2	Page 3			2 Hz F/F	10 Hz	100 Hz	500 Hz	d12	d13	d14	d15

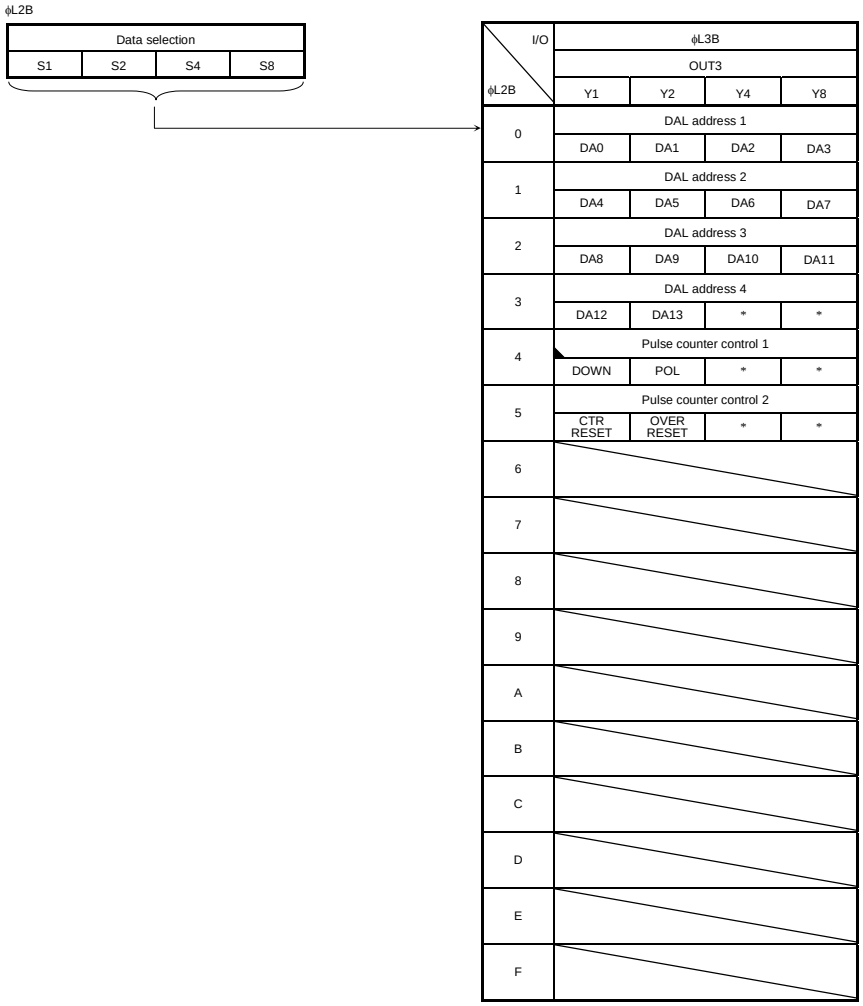
Page 2	φL1				φL2				φL3				φK1				φK2				φK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	Interrupt control				I/O control 1				I/O port 1				Interrupt control				SI02 decode data				I/O port 1			
	POL1 (INTR1)	POL2 (INTR2)	IE	*	-0	-1	-2	-3	-0	-1	-2	-3	POL1 (INTR1)	POL2 (INTR2)	IE	IMF	DCD0	DCD1	DCD2	DCD3	-0	-1	-2	-3
1	Interrupt enable flag 1				I/O control 2				I/O port 2				Interrupt enable flag 1				SI02 information data 1				I/O port 2			
	EF1 (INTR1)	EF2 (INTR2)	EF3 (SIO-3/4)	EF4 (SIO-1)	-0	-1	-2	-3	-0	-1	-2	-3	EF1 (INTR1)	EF2 (INTR2)	EF3 (SIO-3/4)	EF4 (SIO-1)	INF0	INF1	INF2	INF3	-0	-1	-2	-3
2	Interrupt enable flag 2				I/O control 3				I/O port 3				Interrupt enable flag 2				SI02 information data 2				I/O port 3			
	EF5 (timer)	EF6 (SIO-2)	*	*	-0	-1	-2	-3	-0	-1	-2	-3	EF5 (timer)	EF6 (SIO-2)	0	0	INF4	INF5	INF6	INF7	-0	-1	-2	-3
3	Interrupt latch reset 1				I/O control 4				I/O port 4				Interrupt latch 1				SI02 information data 3				I/O port 4			
	ILR1 (INTR1)	ILR2 (INTR2)	ILR3 (SIO-3/4)	ILR4 (SIO-1)	-0	-1	-2	-3	-0	-1	-2	-3	IL1 (INTR1)	IL2 (INTR2)	IL3 (SIO-3/4)	IL4 (SIO-1)	INF8	INF9	INF10	INF11	-0	-1	-2	-3
4	Interrupt latch reset 2				I/O control 5				I/O port 5				Interrupt latch 2				SI02 information data 4				I/O port 5			
	ILR5 (timer)	ILR6 (SIO-2)	*	*	-0	-1	-2	-3	-0	-1	-2	-3	IL5 (timer)	IL6 (SIO-2)	0	0	INF12	INF13	INF14	INF15	-0	-1	-2	-3
5	Timer-counter interrupt detect data 1				I/O control 6				I/O port 6				Timer-counter data 1				SI02 offset/check data 1				I/O port 6			
	ID0	ID1	ID2	ID3	-0	-1	-2	-3	-0	-1	-2	-3	CT0	CT1	CT2	CT3	OFS0/ CHK0	OFS1/ CHK1	OFS2/ CHK2	OFS3/ CHK3	-0	-1	-2	-3
6	Timer-counter interrupt detect data 2				I/O control 7				I/O port 7				Timer-counter data 2				SI02 offset/check data 2				I/O port 7			
	ID4	ID5	ID6	ID7	-0	-1	-2	-3	-0	-1	-2	-3	CT4	CT5	CT6	CT7	OFS4/ CHK4	OFS5/ CHK5	OFS6/ CHK6	OFS7/ CHK7	-0	-1	-2	-3
7	Timer-counter control				I/O control 8				I/O port 8								SI02 offset/check data 2				I/O port 8			
	CK SEL0	CK SEL1	GT	Counter Reset	-0	-1	-2	-3	-0	-1	-2	-3					OFS8/ CHK8	OFS9/ CHK9	0	0	-0	-1	-2	-3
8	Timer reset		CKSTP モード	*	I/O control 9				I/O port 9								HOLD	INTR1	INTR2	STOP F/F	I/O port 9			
	2 Hz F/F Reset	Counter Reset			-0	-1	-2	-3	-0	-1	-2	-3									-0	-1	-2	-3
9	HOLD PLL off control	IF counter sprit	*	Prescaler IN	I/O control 10				I/O port 10								MUTE	Mute control			I/O port 10			
					-0	-1	-2	-3	-0	-1	-2	-3						IO1	POL	HOLD	-0	-1	-2	-3
A	Oscillation control				I/O port 8 pulled-down				DAL	(DATA) → DA	OT Count Up	I/O port 8 pulled up					Unlock detect		Input port		DAL	0	0	0
	OSC1 ON (4.5 MHz)	OSC2 ON (4.5 MHz)	CPU CK SEL	TIMER/RE F CK SEL	-0	-1	-2	-3									F/F	ENA	IN1	IN2				
B	CA flag	*	*	*	Data selection				DAL address/pulse counter control				CA flag	0	0	0	Data selection				DAL address			
					S1	S2	S4	S8	DA0	DA1	DA2	DA3					S1	S2	S4	S8	DA0	DA1	DA2	DA3
C	G-register 1				General-purpose output data/serial interface output data/segment I/O control				Data register 1				G-register 1								Data register 1			
	G0	G1	G2	G3	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	d0	d1	d2	d3	G0	G1	G2	G3					d0	d1	d2	d3
D	G-register 2				Segment data 1				Data register 2				G-register 2								Data register 2			
	G4	G5	G6	G7	COM1	COM2	COM3	COM4	d4	d5	d6	d7	G4	G5	G6	G7					d4	d5	d6	d7
E	Test port 1				Segment data 2				Data register 3												Data register 3			
	#0	#1	#2	#3	COM1	COM2	COM3	COM4	d8	d9	d10	d11									d8	d9	d10	d11
F	Page		*	Test port 2	Segment data 3/LCD driver control				Data register 4				Page		0	0	Timer				Data register 4			
	Page 2	Page 3		#4	COM1	COM2	COM3	COM4	d12	d13	d14	d15	Page 2	Page 3			2 Hz F/F	10 Hz	100 Hz	500 Hz	d12	d13	d14	d15

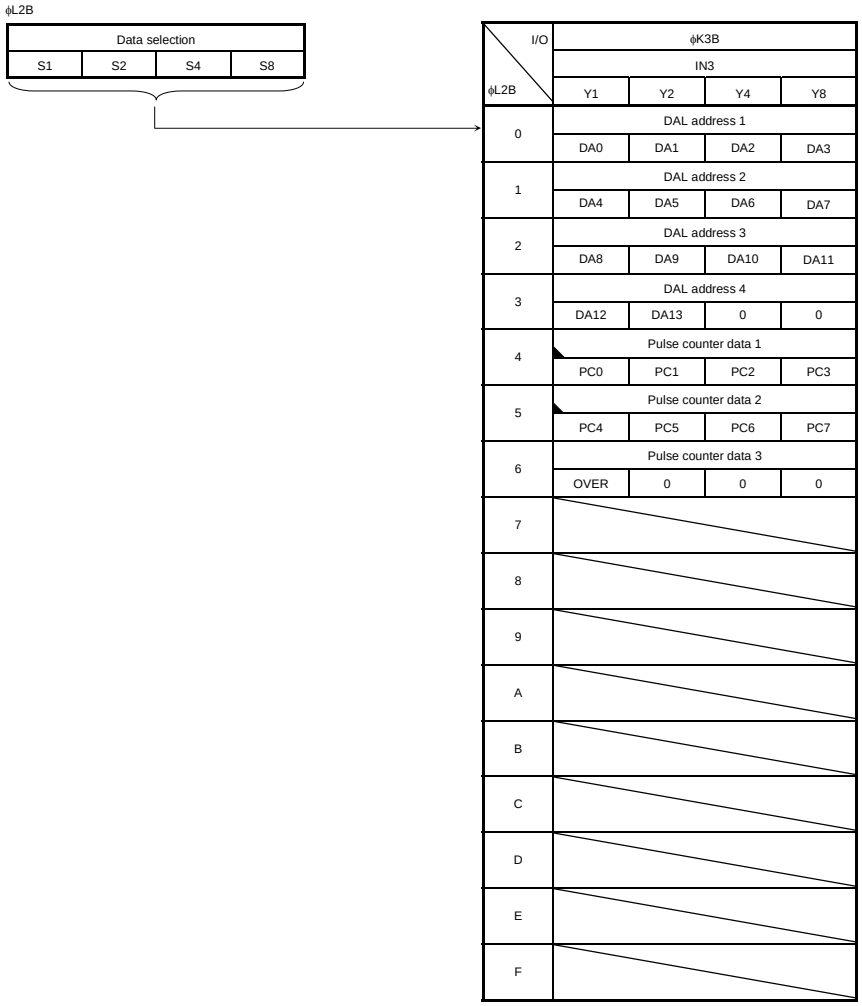
Page 3	ϕL1				ϕL2				ϕL3				ϕK1				ϕK2				ϕK3			
	OUT1				OUT2				OUT3				IN1				IN2				IN3			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	A/D control 1				I/O control 1				I/O port 1				A/D data				SI02 decode data				I/O port 1			
	AD SEL0	AD SEL1	AD SEL2	STA	-0	-1	-2	-3	-0	-1	-2	-3	AD0	AD1	AD2	AD3	DCD0	DCD1	DCD2	DCD3	-0	-1	-2	-3
1	A/D control 2				I/O control 2				I/O port 2				A/D data				SI02 information data 1				I/O port 2			
	CK SEL1	CK SEL2	*	*	-0	-1	-2	-3	-0	-1	-2	-3	AD4	AD5	AD6	AD7	INF0	INF1	INF2	INF3	-0	-1	-2	-3
2	Serial I/F-3/4 control 1				I/O control 3				I/O port 3				A/D data				SI02 information data 2				I/O port 3			
	edge	SCK INV	SCK0	SIO ON	-0	-1	-2	-3	-0	-1	-2	-3	BUSY	0	0	0	INF4	INF5	INF6	INF7	-0	-1	-2	-3
3	Serial I/F-3/4 control 2				I/O control 4				I/O port 4				Serial I/F-3/4 monitor 1				SI02 information data 3				I/O port 4			
	STA	SI1S	8 bit	Nch	-0	-1	-2	-3	-0	-1	-2	-3	BUSY	COUNT	SIO F/F	SO-NG F/F	INF8	INF9	INF10	INF11	-0	-1	-2	-3
4	Serial I/F-3/4 control 3				I/O control 5				I/O port 5				Serial I/F-3/4 monitor 2				SI02 information data 4				I/O port 5			
	SO3/SO4	SCK3 /SCK4	ENA	MOD	-0	-1	-2	-3	-0	-1	-2	-3	SO/SDA	SCK/SCL	ENA	0	INF12	INF13	INF14	INF15	-0	-1	-2	-3
5	Serial I/F-3/4 control 4				I/O control 6				I/O port 6				Serial I/F-3/4 monitor 3				SI02 offset/check data 1				I/O port 6			
	CK0	CK1	F/F Reset	MSB	-0	-1	-2	-3	-0	-1	-2	-3	STA F/F	STP F/F	BUSY2	ACK	OFS0/ CHK0	OFS1/ CHK1	OFS2/ CHK2	OFS3/ CHK3	-0	-1	-2	-3
6	Serial I/F-3/4 control 5				I/O control 7				I/O port 7				Serial I/F-1/2 monitor				SI02 offset/check data 2				I/O port 7			
	STP	*	*	*	-0	-1	-2	-3	-0	-1	-2	-3	BUSY	COUNT	SIO F/F	0	OFS4/ CHK4	OFS5/ CHK5	OFS6/ CHK6	OFS7/ CHK7	-0	-1	-2	-3
7	Serial I/F-1/2 control 1				I/O control 8				I/O port 8				Serial I/F-3/4 input data 1				SI02 offset/check data 2				I/O port 8			
	edge	SCK INV	SCK0	SIO ON	-0	-1	-2	-3	-0	-1	-2	-3	SI0	SI1	SI2	SI3	OFS8/ CHK8	OFS9/ CHK9	0	0	-0	-1	-2	-3
8	Serial I/F-1/2 control 2				I/O control 9				I/O port 9				Serial I/F-3/4 input data 2				HOLD	INTR1	INTR2	STOP F/F	I/O port 9			
	STA	SOI	8 BIT/CHK	MOD	-0	-1	-2	-3	-0	-1	-2	-3	SI4	SI5	SI6	SI7					-0	-1	-2	-3
9	Buzzer output control 1				I/O control 10				I/O port 10				Serial I/F-1 input data 1				MUTE	Mute control			I/O port 10			
	BF0	BF1	BF2	BEN	-0	-1	-2	-3	-0	-1	-2	-3	SI0	SI1	SI2	SI3		IO1	POL	HOLD	-0	-1	-2	-3
A	Buzzer output control 2				I/O port 8 pulled down				DAL	(DATA) → DA	OT Count Up	I/O port 8 pulled up	Serial I/F-1 input data 2				Unlock detect		Input port		DAL	0	0	0
	BM0	BM1	ON	POL	-0	-1	-2	-3					SI4	SI5	SI6	SI7	F/F	ENA	IN1	IN2				
B	CA flag	*	*	*	Data selection				DAL address/pulse counter control				CA flag	0	0	0	Data selection				DAL address			
					S1	S2	S4	S8	DA0	DA1	DA2	DA3					S1	S2	S4	S8	DA0	DA1	DA2	DA3
C	G-register 1				General-purpose output data/serial interface output data/segment I/O control				Data register 1				G-register 1								Data register 1			
	G0	G1	G2	G3	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	OT/SO /SEG	d0	d1	d2	d3	G0	G1	G2	G3					d0	d1	d2	d3
D	G-register 2				Segment data 1				Data register 2				G-register 2								Data register 2			
	G4	G5	G6	G7	COM1	COM2	COM3	COM4	d4	d5	d6	d7	G4	G5	G6	G7					d4	d5	d6	d7
E	Test port 1				Segment data 2				Data register 3												Data register 3			
	#0	#1	#2	#3	COM1	COM2	COM3	COM4	d8	d9	d10	d11									d8	d9	d10	d11
F	Page		*	Test port 2	Segment data 3/LCD driver control				Data register 4				Page		0	0	Timer				Data register 4			
	Page 2	Page 3		#4	COM1	COM2	COM3	COM4	d12	d13	d14	d15	Page 2	Page 3			2 Hz F/F	10 Hz	100 Hz	500 Hz	d12	d13	d14	d15

ϕL2B

Data selection			
S1	S2	S4	S8

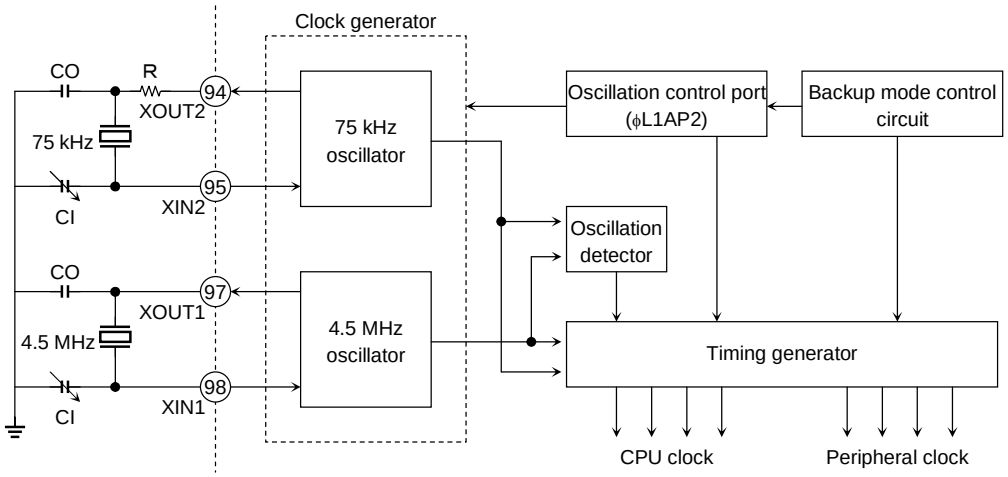
I/O / ϕL2B	ϕL2C OUT2				ϕL2D OUT2				ϕL2E OUT2				ϕL2F OUT2			
	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
0	General-purpose output port data 1				S1				S17				S33			
	OT1	OT2	OT3	OT4	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4
1	General-purpose output port data 2				S2				S18				S34			
	OT5	OT6	OT7	OT8	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4
2	General-purpose output port data 3				S3				S19				S35			
	OT9	OT10	OT11	OT12	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	COM1	COM2	COM3	*
3	General-purpose output port data 4				S4				S20				S36			
	OT13	OT14	OT15	OT16	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	COM1	COM2	*	*
4	General-purpose output port data 5				S5				S21							
	OT17	OT18	OT19	OT20	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
5	General-purpose output port data 6				S6				S22							
	OT21	OT22	OT23	OT24	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
6	General-purpose output port data 7				S7				S23							
	OT25	OT26	OT27	OT28	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
7	General-purpose output port data 8				S8				S24							
	OT29	OT30	*	*	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
8	Serial I/F-3/4 output data 1				S9				S25							
	SO0	SO1	SO2	SO3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
9	Serial I/F-3/4 output data 2				S10				S26							
	SO4	SO5	SO6	SO7	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
A	Serial I/F-1/2 output data 1				S11				S27							
	SO0	SO1	SO2	SO3	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
B	Serial I/F-1/2 output data 2				S12				S28							
	SO4	SO5	SO6	SO7	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
C					S13				S29							
					COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
D					S14				S30							
					COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4				
E	Segment I/O control 1				S15				S31				LCD control 1			
	SEG27	SEG28	SEG29	SEG30	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	DUTY0	DUTY1	BIAS	FRAME
F	Segment I/O control 2				S16				S32				LCD control 2			
	SEG31	SEG32	SEG33	SEG34	COM1	COM2	COM3	COM4	COM1	COM2	COM3	COM4	DISP OFF	LCD OFF	*	*


ϕL2B
Data selection
S1 S2 S4 S8
I/O
ϕL2B
ϕL3B
OUT3
Y1 Y2 Y4 Y8
0 DAL address 1 DA0 DA1 DA2 DA3
1 DAL address 2 DA4 DA5 DA6 DA7
2 DAL address 3 DA8 DA9 DA10 DA11
3 DAL address 4 DA12 DA13 * *
4 Pulse counter control 1 DOWN POL * *
5 Pulse counter control 2 CTR RESET OVER RESET * *
6
7
8
9
A
B
C
D
E
F


ϕL2B
Data selection
S1 S2 S4 S8
I/O
ϕL2B
ϕK3B
IN3
Y1 Y2 Y4 Y8
0 DAL address 1 DA0 DA1 DA2 DA3
1 DAL address 2 DA4 DA5 DA6 DA7
2 DAL address 3 DA8 DA9 DA10 DA11
3 DAL address 4 DA12 DA13 0 0
4 Pulse counter data 1 PC0 PC1 PC2 PC3
5 Pulse counter data 2 PC4 PC5 PC6 PC7
6 Pulse counter data 3 OVER 0 0 0
7
8
9
A
B
C
D
E
F

○ System Clock Control Circuit

The system clock control circuitry consists of a clock generator, an oscillation detector, an oscillation control port, a timing generator, and a backup mode control circuit.



4.5 MHz oscillator: CI = 30 pF, CO = 30 pF (typ.)

75 kHz oscillator: CI = 30 pF, CO = 30 pF, R = 0 Ω (typ.)

Note: Select a crystal oscillator with a low CI value and good startup characteristics.

Note: Determine the constants for external resistors and capacitors in accordance with the crystal oscillator actually used.

Note: Fix to GND level the input pin (XIN1 or XIN2) of any oscillator that is not connected to a crystal oscillator.

Note: The 4.5 MHz and 75 kHz oscillators incorporate Schmitt trigger circuits.

1. Clock Generator and Oscillation Detector

The clock generator is a circuit to generate a reference clock supplied to the CPU core and peripheral hardware. The TC9325FG incorporates both 4.5 MHz and 75 kHz oscillators. Connect the 4.5 MHz oscillator to the XIN1 and XOUT1 pins and the 75 kHz oscillator to the XIN2 and XOUT2 pins.

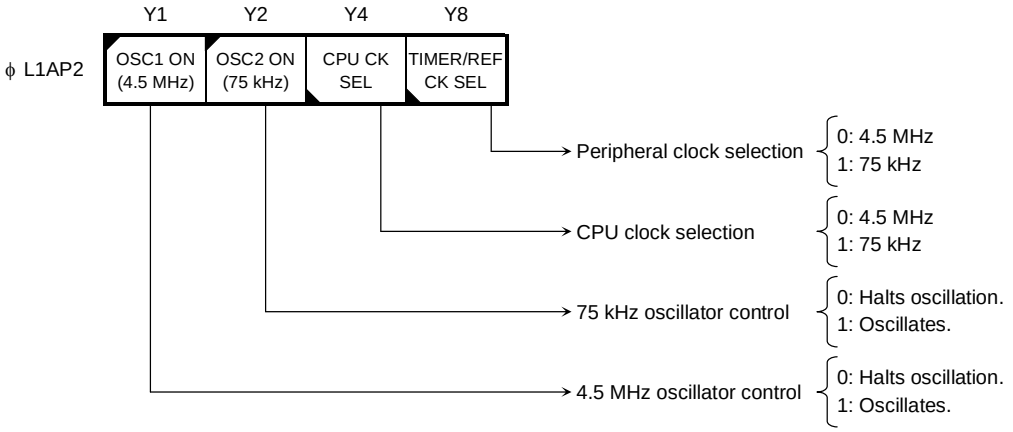
The oscillation detector detects the clocks for the 4.5 MHz and 75 kHz oscillators and selects which to use as the reference clock. If clocks for both oscillators are detected, the clock for the 4.5 MHz oscillator is selected as the reference clock.

Accordingly, either one or both oscillators (4.5 MHz and 75 kHz) can be connected. Note that an input pin (XIN1 or XIN2) that is not connected to an oscillator must be fixed to GND level. If both the 75 kHz and 4.5 MHz oscillators are connected, after a reset the CPU operates on the 4.5 MHz crystal oscillator clock.

The clock can be readily switched by software between the CPU operating clock and the peripheral clock.

2. Oscillation Control Port

The oscillation control port controls the 4.5 MHz and 75 kHz oscillators.



Note: Before switching to the clock for a halted oscillator, wait at least 100 ms after oscillation starts, then switch.

3. Timing Generator

The timing generator is a circuit for generating various system clocks supplied from the selected reference clock to the CPU core or peripheral hardware. The reference clock is selected by the oscillation detector and oscillation control port.

○ **System Reset**

A system reset on the device occurs when an L signal is applied to the $\overline{\text{RESET}}$ pin, or when the voltage supplied to the V_{DD} pin goes from 0 V to more than 3.5 V (a power-on reset). Following a system reset, the program starts from address 0 after a standby period of 100 ms.

Because the power-on reset function is normally used, fix the $\overline{\text{RESET}}$ pin to the H level.

Note: The power-on reset function can be disabled by using the AI switch. Please clearly specify whether you want the power-on reset function disabled or not in your ES order sheet. If the power-on reset function is disabled, use the $\overline{\text{RESET}}$ pin to trigger resets.

Note: During a system reset and during the standby period following the reset, the LCD common signal and segment outputs are fixed at the L level.

Note: After a system reset, the non-initialized internal ports shown in the previous I/O map must be initialized by software. After a reset, the ports and bits on the I/O map indicated by the ◣ symbol are fixed to 0 and the ports and bits indicated by the ◤ symbol are fixed to 1. Ports and bits with no symbol are undefined.

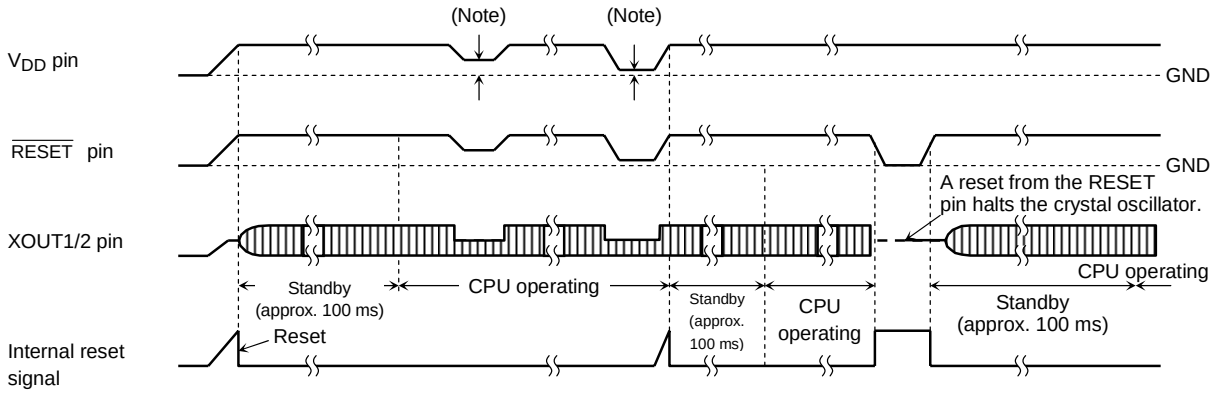
I/O / Code	ϕL2			
	OUT2			
	Y1	Y2	Y4	Y8
0	I/O port 1 control			
	-0	-1	-2	-3

After a system reset, the ports with no symbols are undefined.

I/O / Code	ϕL1			
	OUT1			
	Y1	Y2	Y4	Y8
6	Reference select			
	R0	R1	R2	R3

After a system reset, these ports are all reset to 1.

After a system reset, ports and bits with no symbol are undefined.



<Operation Timing Example>

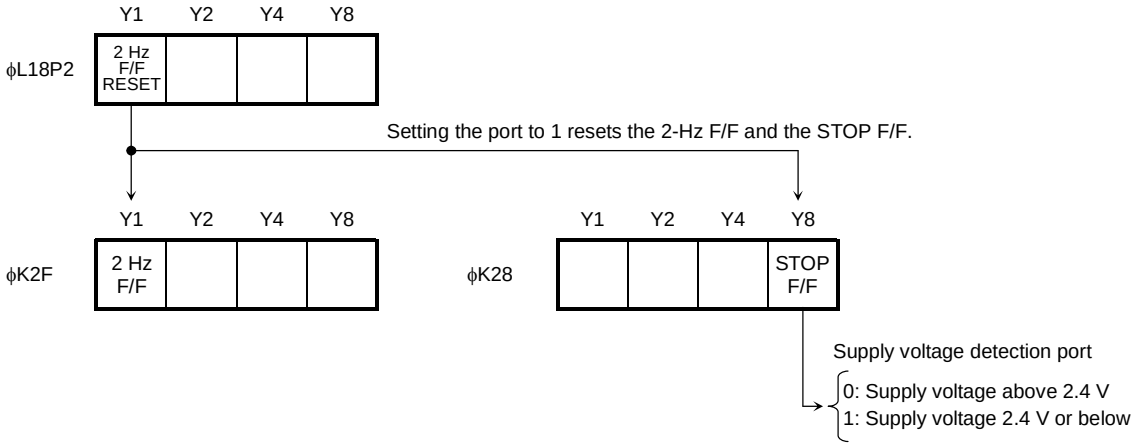
Note: If there is a possibility of the supply voltage falling below 3.5 V, set to Clock Stop mode or trigger a reset. Re-applying the power supply voltage after it has dropped to below 0.3 V to 0.6 V triggers a power-on reset.

1. Reset Control Port

The CPU can be reset using the $\overline{\text{RESET}}$ pin or by a power-on reset.

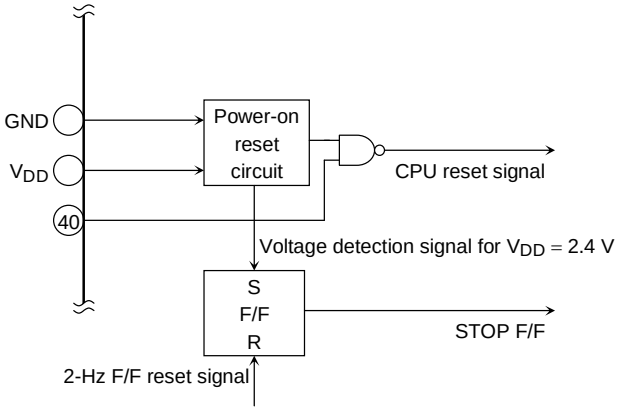
If the power supply falls to 2.4 V or below, the STOP F/F bit is set to 1. This bit can be used for such purposes as detecting a fall in the supply voltage from a momentary interruption or during Backup mode. When such a drop in supply voltage is detected, set Clock Stop mode to prevent CPU malfunction then back up the memory. Setting the 2-Hz reset bit to 1 resets the STOP F/F bit.

The reset control data are read to data memory by the IN1 instruction with the operand [CN = 7H].



Note: For information on the 2-Hz F/F bit, see the timer port section.

2. Reset Circuit Structure and Operation Timing

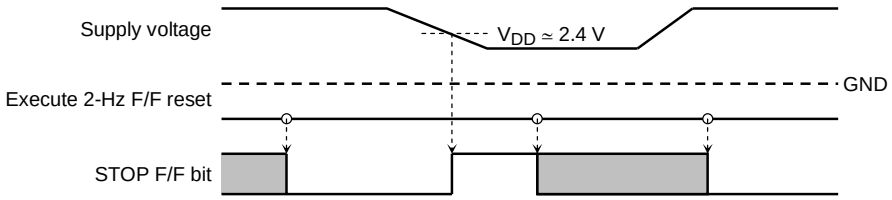


Note: When the supply voltage falls to 2.4 V or below, set Backup mode.

Note: Re-switching on the power supply when the supply voltage falls to or below the range 0.3 to 0.6 V triggers a reset.

Note: When Backup mode is not set, be sure to turn the power supply on from the GND level.

Note: If necessary, use the $\overline{\text{RESET}}$ pin to trigger a reset.



Example of Supply Voltage Detection Bit Operation

○ Backup Modes

To access the three Backup modes, execute the CKSTP or WAIT instruction.

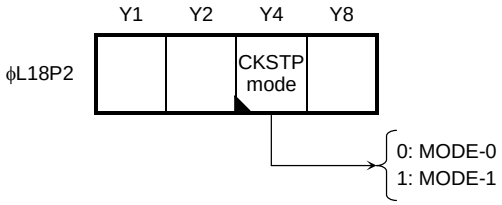
1. Clock Stop Mode

Clock Stop mode halts the system and maintains the internal state of the system immediately prior to halting at low current consumption (1 μA or below). In Clock Stop mode, the crystal oscillator halts and the LCD display output pins and CMOS output ports are all automatically fixed to the L level. The supply voltage can be reduced to 2.0 V.

When the CKSTP instruction is executed, execution halts at the address of the CKSTP instruction. Therefore, execution starts again from the next address when Clock Stop mode is released (after a standby period of around 100ms).

(1) Setting Clock Stop Mode

Clock Stop mode can be set to one of two modes. The CKSTP MODE bit determines which of the two modes are set. This bit is accessed by the OUT1 instruction with the operand [CN = 8H] on I/O map page 2.



1) MODE-0

In mode 0, executing the CKSTP instruction when the $\overline{\text{HOLD}}$ pin is L sets Clock Stop mode. Executing the CKSTP instruction when the $\overline{\text{HOLD}}$ pin is H is equivalent to executing a NOOP instruction.

2) MODE-1

In mode 1, executing the Clock Stop instruction sets Clock Stop mode regardless of the level of the $\overline{\text{HOLD}}$ pin.

Note: The PLL is off during execution of the CKSTP instruction.

Note: Prior to executing the CKSTP instruction, be sure to access the $\overline{\text{HOLD}}$ input and I/O port 8 input ports to reset the 2-Hz F/F. Attempting to set Clock Stop mode without resetting the 2-Hz F/F may result in a failure to set the mode.

(2) Releasing Clock Stop Mode

1) MODE-0

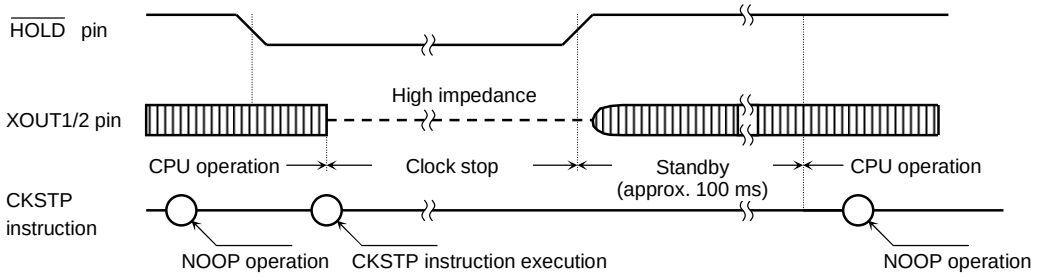
In mode 0, Clock Stop mode is released when the $\overline{\text{HOLD}}$ pin goes to H, or by a change in the input state of any I/O port (P8-0 to 3) pin set to input mode.

2) MODE-1

In mode 1, Clock Stop mode is released by a change in the input state of the $\overline{\text{HOLD}}$ pin or of any I/O port (P8-0 to 3) pin set to input mode.

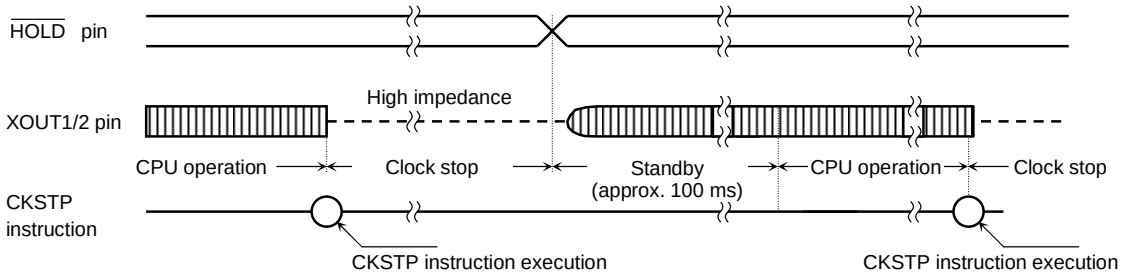
(3) Clock Stop Mode Timing

1) MODE-0



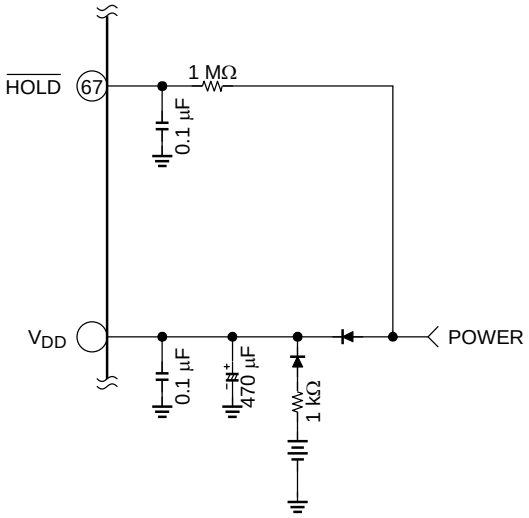
(Executing the CKSTP instruction while the $\overline{\text{HOLD}}$ pin input is Low sets the device to Clock Stop mode.)

2) MODE-1

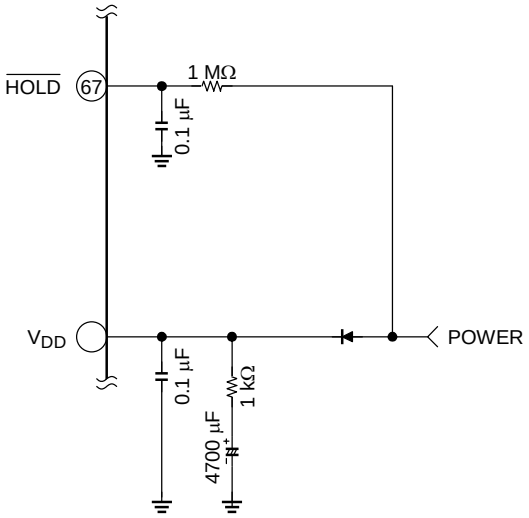


(Executing the CKSTP instruction always sets the device to Clock Stop mode.)

(4) Backup Circuit Example (Mode 0)



Example of Backup Circuit Using Battery



Example of Backup Circuit Using Capacitor

2. Wait Mode

Wait mode halts the system and maintains, with reduced current consumption, the internal state of the system immediately prior to halting. Two Wait modes are supported: soft wait and hard wait. When the Wait instruction is executed, execution halts at the address of the WAIT instruction. Therefore, when Wait mode is released, execution starts again from the next address (without delaying for the standby time).

(1) Soft Wait Mode

Executing the WAIT instruction with the operand [P = 0H] stops the device's internal CPU only. In this mode, the crystal oscillator and other circuitry continue to operate normally. Using Soft Wait mode in the software for clock functions reduces the current consumed during clock operation.

Note: The current consumption varies according to the software because the current consumed is dependent on the time for executing CPU operations.

(2) Hard Wait Mode

Executing a WAIT instruction with the operand [P = 1H] stops all operation other than the crystal oscillator. This reduces current consumption still further than Soft Wait mode. In this state, CPU operation is halted.

Note: During Hard Wait mode, the output ports are retained and the LCD output pins are all fixed to L.

(3) Setting Wait Mode

Executing the WAIT instruction always sets Wait mode.

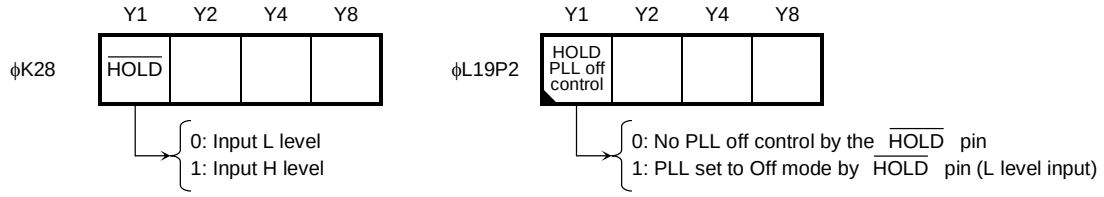
Note: In Wait mode, the PLL is automatically turned off.

(4) Wait Mode Release Conditions

Wait mode is released by the following conditions.

1) At a change in the input state of the $\overline{\text{HOLD}}$ pin.
2) At a change in the input state of an I/O port (P8-0 to 3) set as an input port.
3) When the 2-Hz timer F/F is set to 1. (In Soft Wait mode only)

3. $\overline{\text{HOLD}}$ Input Port



The $\overline{\text{HOLD}}$ pin can be used as an input port. Executing the IN2 instruction with the operand [CN = 8H] reads the data input from this bit to data memory.

When setting Clock Stop or Wait mode, always access this port prior to executing the backup instruction. Note that if the instruction is executed without first accessing this port, the device may not enter Clock Stop or Wait mode.

When the HOLD PLL off control bit is set to 1, inputting L level to the $\overline{\text{HOLD}}$ pin sets PLL Off mode. PLL Off mode can be quickly set when changing the batteries. This bit is accessed by the OUT1 instruction with the operand [CN = 9H] on I/O map page 2. PLL Off mode can also be set by setting all the reference ports to 1. (See the section on the reference frequency divider.)

○ Interrupt Function

Peripheral hardware that can use interrupts are the INTR1 and INTR2 pins, serial interfaces 1 to 4, and the timer-counter.

When the peripheral hardware satisfies the conditions, the hardware outputs an interrupt request signal and issues an interrupt request. When the interrupt is accepted, processing branches to the vector address determined by the interrupt source, and the interrupt handling routine commences.

At the start and end of normal interrupt handling in an interrupt routine, prior processing and post processing are needed to restore the state that prevailed when the interrupt occurred. The registers used by the ALU and any data memory that was not corrupted must be saved and restored to the interrupt data memory. When the interrupt handling is complete, the program is restored by an interrupt return instruction.

1. Interrupt Control Circuit

The interrupt control circuit consists of an interrupt enable flag, an interrupt latch, and an interrupt priority circuit block. These are controlled and set by the OUT1/IN1 instructions on page 2 of the I/O map.

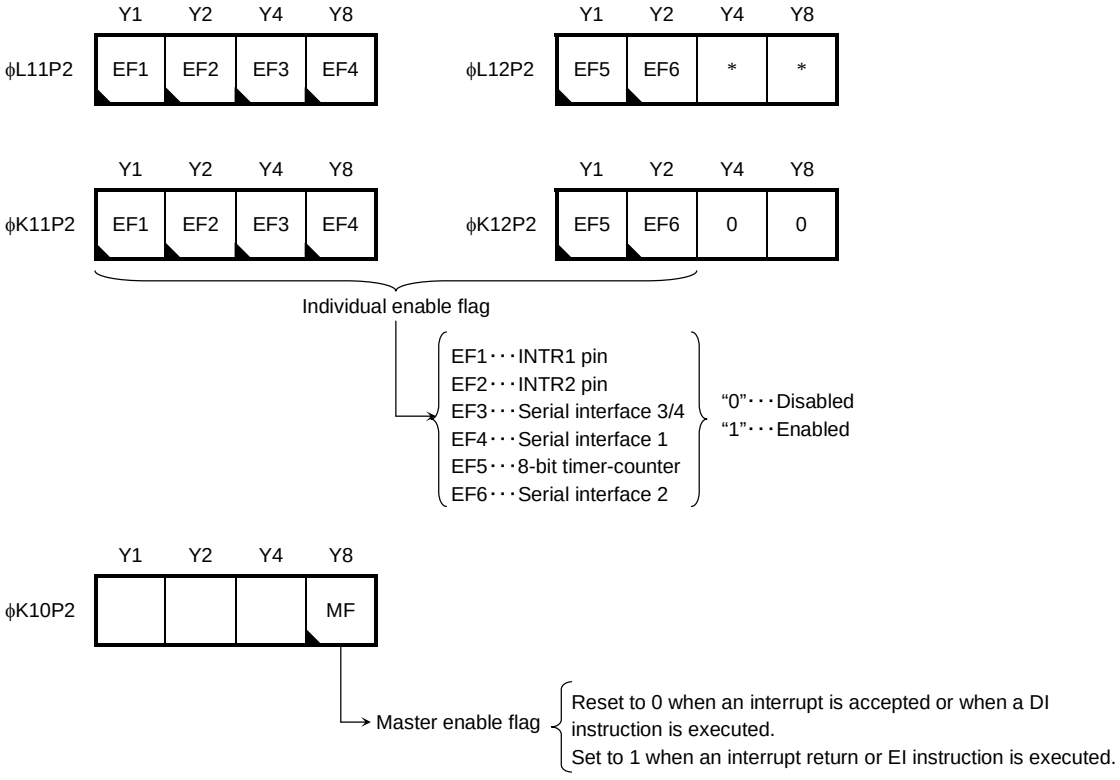
(1) Interrupt Enable Flag

The interrupt enable flags include the master enable flag and individual enable flags for each interrupt source. The individual enable flags enable or disable interrupts in accordance with the interrupt source. The master enable flag can enable or disable any interrupt. Setting the enable register to 1 enables an interrupt while 0 disables the interrupt.

The individual enable flags are accessed by the OUT1/IN1 instruction with the operand [CN = 1H, 2H] on I/O map page 2.

The master enable flag enables/disables an interrupt on execution of the EI/DI instruction. To disable an interrupt during program execution use the DI instruction. To enable an interrupt, use the EI instruction. Interrupts are enabled while the program between the EI and DI instructions is executing.

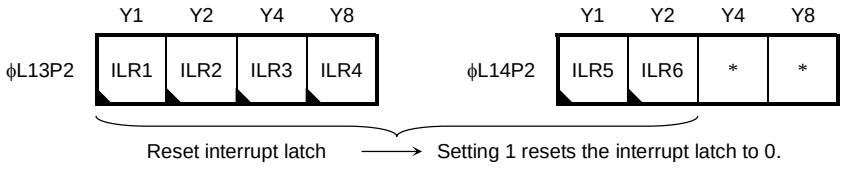
The master enable flag is reset to 0 when an interrupt request is received and all interrupts are disabled. An interrupt return instruction sets the flag to 1. The master enable flag can be read by the IN1 instruction with the operand [CN = 0H] on I/O map page 2 to data memory.

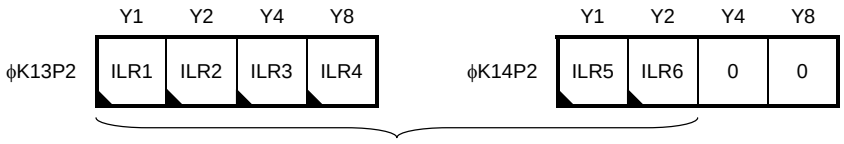


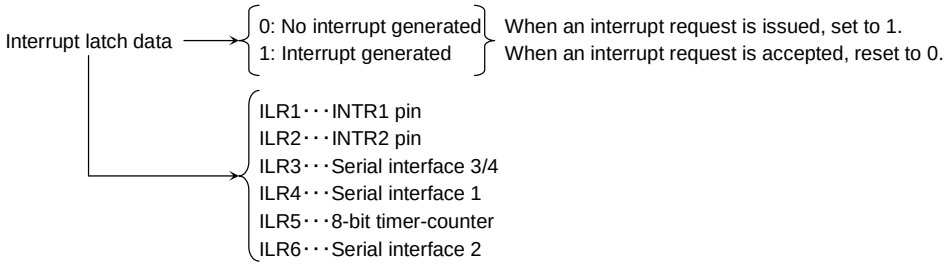
(2) Interrupt Latch

When an interrupt request is issued the interrupt latch is set to 1. If the interrupt is enabled, the interrupt latch passes the request to accept the interrupt to the CPU and branches to the interrupt routine. If the interrupt is accepted, the interrupt latch is automatically reset to 0.

The interrupt latch data can be read by software, allowing each application to check whether an interrupt has been generated or not. In addition, an interrupt latch set to 1 by an interrupt request can be reset to 0 and the interrupt request can be cleared or initialized.







(3) Interrupt Priority Circuit Block

The interrupt priority circuit determines the interrupt handling priority when more than one interrupt is generated at the same time or when an interrupt is enabled after several are generated. This block also generates the vector address for the interrupt routine.

Priority	Interrupt Source	Vector Address
1	INTR1 pin	0001H
2	INTR2 pin	0002H
3	Serial interface 3/4	0003H
4	Serial interface 1	0004H
5	Timer-counter	0005H
6	Serial interface 2	0006H

2. Interrupt Acceptance Procedure

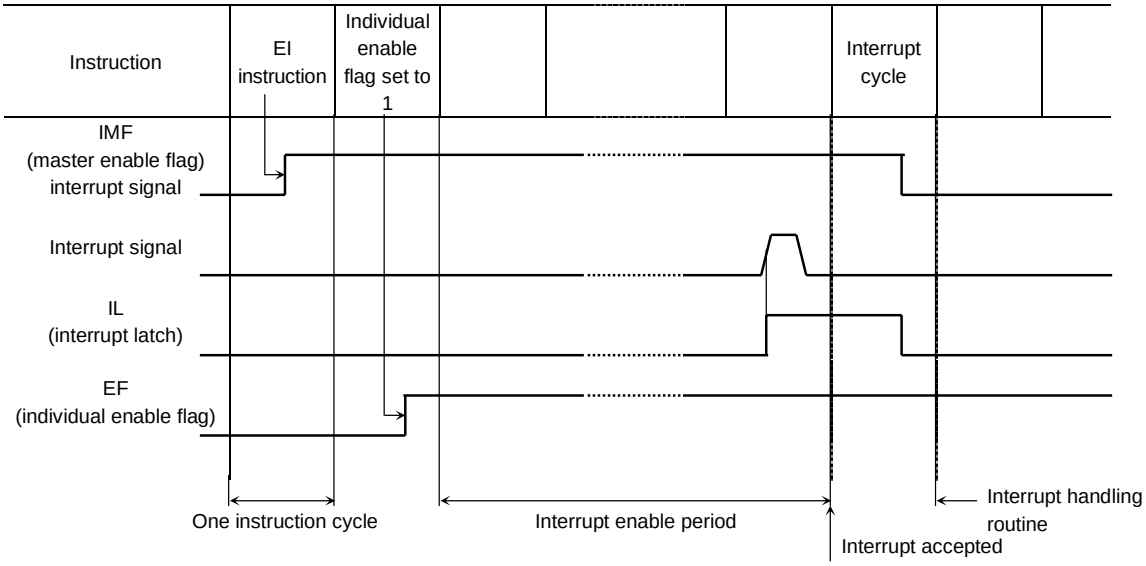
An interrupt request is held until either the interrupt is accepted or the interrupt latch is reset to 0 by a system reset or by software. The following describes the interrupt acceptance operation.

1) The peripheral hardware outputs an interrupt request signal if the interrupt conditions are satisfied and sets the interrupt latch to 1.
2) When the interrupt enable flag for the interrupt source and the master enable flag are set to 1, the interrupt latch for the accepted interrupt source is reset to 0.
3) The interrupt master enable flag is reset to 0 and the interrupt is disabled.
4) The contents of the stack pointer are decremented by 1.
5) The contents of the program counter are saved to the stack register. At that time, the contents of the program counter have the address following the address when the interrupt was accepted or enabled.
6) The contents of the vector address corresponding to the accepted interrupt are loaded to the program counter.
7) The vector address contents are executed.

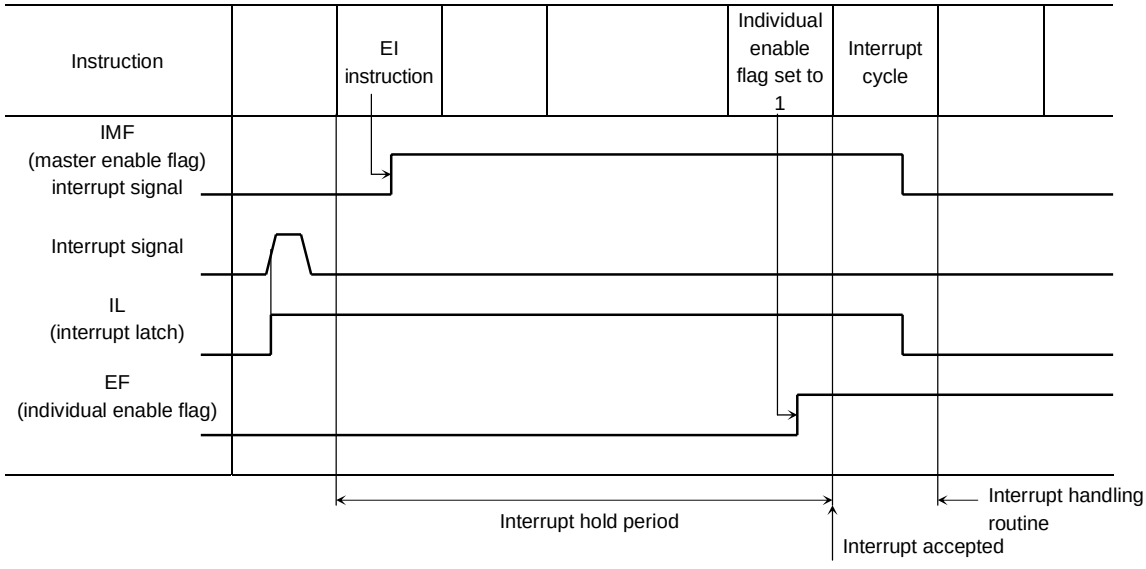
Steps (1) to (6) above are executed in one instruction cycle. This instruction cycle is called an interrupt cycle.

Note: The stack pointer can specify up to 16 stack register levels. The contents of the stack pointer cannot be refered.

With an interrupt enable period



With an interrupt hold period



3. Return from Interrupt Handling Routine

To recover from an interrupt handling routine and return to the processing taking place before the interrupt, a special instruction is used. This is the RNI instruction. When the RNI instruction is issued, the following processing is automatically performed in the order shown.

1) The contents of the address stack specified by the stack pointer are restored to the program counter.
2) The interrupt master enable flag is set to 1 (enabled).
3) The stack pointer contents are incremented by 1.

The RNI instruction completes the above processing in one instruction cycle.

4. Interrupt Handling Routine

If the interrupt occurs in an interrupt-enabled area of the program, the interrupt is accepted at the point the interrupt request is issued regardless of the program being executed at that time. Accordingly, when returning to the original program after the interrupt handling is completed, it is necessary to recover as if no interrupt handling had taken place. Therefore, at the very least, any registers or data memory that might be processed during the interrupt handling routine must be saved before and restored after the interrupt handling routine.

(1) Saving

In save processing, the carry flag must be saved. If an interrupt is accepted during an arithmetic operation, the contents of the carry flag (CY) and other data change, causing the program to make errors of judgment after restoration. This is why it is necessary to use the IN1 instruction to save the contents of the carry flag in the I/O map to data memory.

If necessary, also save the contents of the data memory and general registers used by the interrupt handling routine. When using such instructions as MVGD, MVGS, and DAL in the interrupt routine, also save the G-register, DAL address register, and other contents.

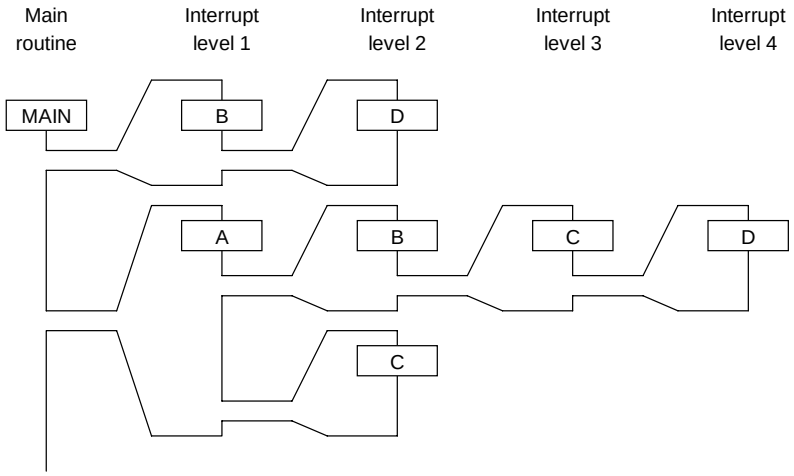
(2) Restoring

The restoration process is simply an inversion of the above saving process.

Because the interrupt master enable flag is reset to 0 when an interrupt is accepted, naturally enough, before the interrupt was accepted the flag must have been set to 1. Therefore, use the RNI instruction to return the master enable flag to its original state.

5. Multiple Interrupts

Multiple interrupt processing allows an interrupt to be handled at the same time another interrupt is being handled. As in the diagram, during handling of an interrupt for interrupt source A or B, another interrupt with source C or D can be handled. The interrupt depth at such a time is known as the interrupt level.



Example of Multiple Interrupts

When using multiple interrupts, note the following.

1) Priority of interrupt sources
2) Restrictions on the address stack levels used when an interrupt request is issued
3) Saving the carry flag and data memory

(1) Priority of interrupt sources

The priority of multiple interrupts is: A < B < C < D as shown in the diagram. Under this priority, a C interrupt must be given preference even though interrupt A or B is being processed. And a D interrupt must be given priority even though a C interrupt is being processed.

A priority for handling multiple interrupts must be determined because of the following hypothetical situation. There are two interrupt sources, A and B. Source A issues a request every 10 ms and the time for handling interrupt A is 4 ms. While source B issues a request every 2 ms and the time for handling interrupt B is 1 ms. If no priority were established for A and B, while interrupt B was being processed, interrupt A would be accepted and processed as a result of an interrupt A request, and interrupt B processing would be repeatedly held up. To prevent this situation, set a priority (A < B) to disable other interrupts during processing of interrupt B and write a program to allow interrupt B to be accepted even during processing of interrupt A.

When all the individual enable flags are set to 1 (interrupts enabled), the priority is determined by the hardware described in the interrupt priority circuit block section. However, by manipulating the individual enable flags by software, the hardware priority can be changed. Normally, in the interrupt handling routine, accepted interrupts and low-priority interrupts are disabled and high-priority interrupts are enabled.

(2) Restrictions on address stack levels

When an interrupt request is issued, the return address is automatically saved to the address stack, as described in the section on interrupt acceptance procedure. The address stack consists of 16 levels, as mentioned in the stack register section, and the address stack can be used even while subroutine call instructions are being executed. Therefore, take care not to exceed the 16 interrupt and subroutine call levels. If these exceed 16, the recorded return addresses are corrupted from the first stack.

(3) Saving

When using multiple interrupts, be sure to secure separate saving areas for each interrupt source.

○ External Interrupt and Timer-Counter Functions

Two types of external interrupts are supported using the INTR1 and INTR2 pins. The rising or falling edges of the signals to these pins are used to issue the interrupt requests.

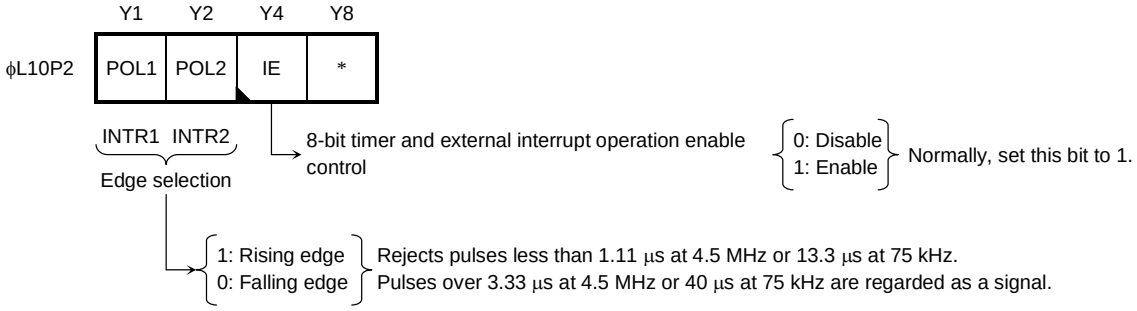
The timer-counter is an 8-bit binary counter with timer and external clock timer functions. The external clock timer function input pins can also be used as external interrupt pins (INTR1, INTR2).

1. External Interrupt Function

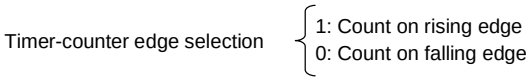
The external interrupts have two input pins: INTR1 and INTR2. Interrupt requests are issued by detecting the rising and falling edges of these pins. The inputs (INTR1 and INTR2) have a Schmitt trigger circuit and noise canceller. When using the CPU operating clock for the noise suppression clock, use a 900 kHz frequency; when using a 75 kHz clock, use a 75 kHz frequency. Pulses that fall below these frequencies are rejected as noise. The input edge can be selected between a rising/falling edge for each pin. The IE bit enables 8-bit timer-counter operations/interrupts and external interrupt requests. This bit is normally set to 1. This bit is controlled by the OUT1 instruction with the operand [CN = 0H] on I/O map page 2.

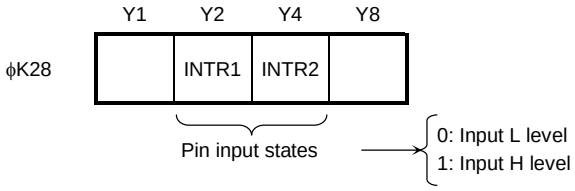
When an INTR1 pin interrupt is accepted, the program branches to address 0001H. When an INTR2 pin interrupt is accepted, the program branches to 0002H.

The INTR1 and INTR2 pins can also be used as input ports. When set to input ports, the input state can be read to data memory by the IN2 instruction with the operand [CN = 8H].



Note: Edge selection also controls the timer-counter external clock edge. Input to the timer-counter does not use the noise canceller function. Care is needed because even when an external interrupt does not occur, clock pulses less than those above are input to the counter.





Note: When the edge is switched by the POL bit, an interrupt request may be issued. Accordingly, when switching the edge, first disable interrupts. To return to normal operation, reset the interrupt latch.

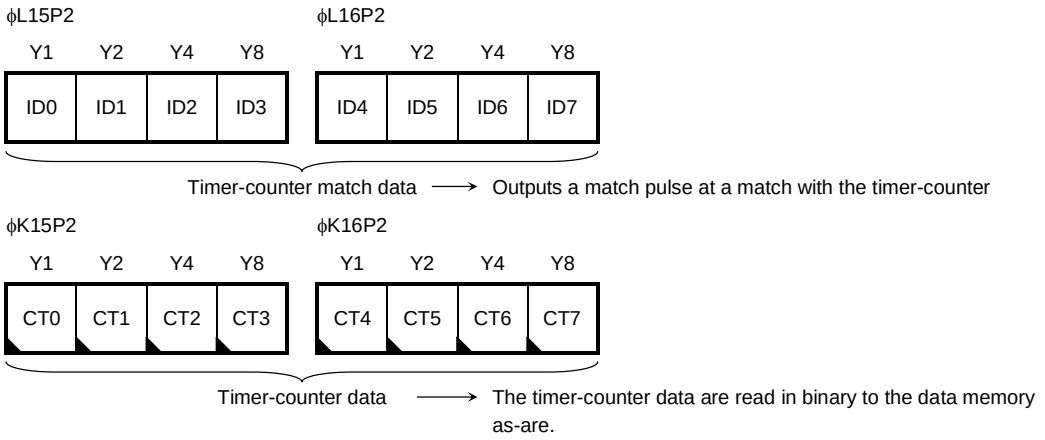
2. Timer-Counter Function

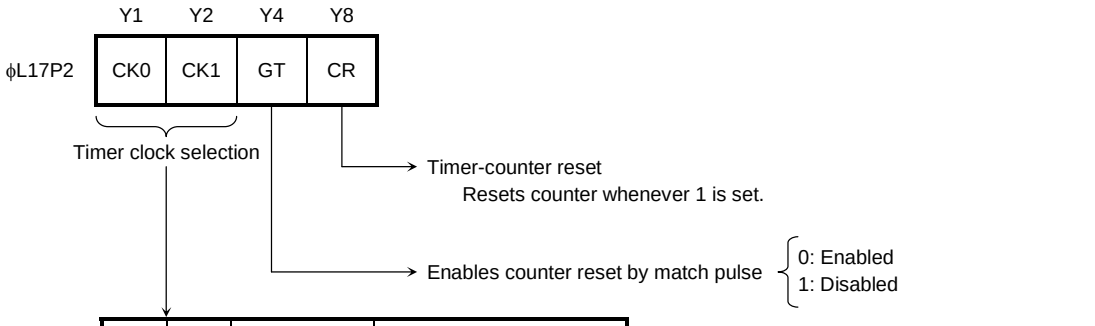
The timer-counter consists of an 8-bit binary counter, a counter match register, a digital comparator, and the control circuits to run these.

The timer-counter inputs a timer clock to an 8-bit binary counter. When the count of the 8-bit binary counter matches the contents of the counter match register, the timer-counter outputs a match signal pulse and generates an interrupt request. The timer-counter can be reset by the match pulse or by software. The reset by match pulse can be enabled or disabled. INTR1/2 input, an instruction cycle, or a frequency of 1 kHz can be selected as a timer clock.

(1) Timer-counter register structure

The timer-counter registers consist of the counter data, a match register, and a control register.





CK0	CK1	CPU clock	Timer clock	
0	0	*	INTR1 pin input	
0	1	4.5 MHz	Instruction cycle clock	562.5 kHz
		75 kHz		25 kHz
1	0	*	25 kHz	
1	1	*	1 kHz	

The clock edge can be selected by the POL bit
0: Counts on rising edge.
1: Counts on falling edge.

Note: When using the timer-counter, the IE bit must be set to 1.

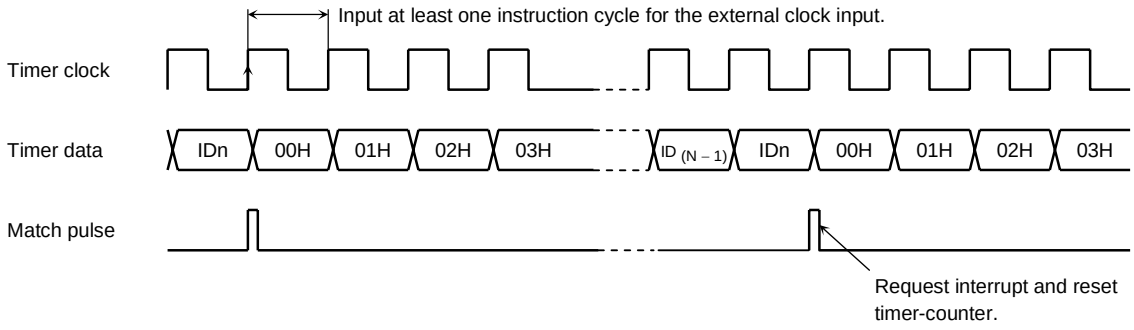
(2) Timer mode

Timer mode is used for detecting a specified period of time. Whenever a specified period is detected, the timer issues an interrupt request and resets the counter. At this time, the control bit is set as a timer clock to 1 kHz or one instruction cycle, the GT bit is set to 0, and the CR bit to 0 (not reset).

Set the timer match data corresponding to the period to be set:

Timer period = IDn (match data) × timer clock cycle

An external pin can be used for the timer clock. Use a clock frequency that is no longer than one instruction cycle. Setting the GT bit to 1 adds up the external clock count.



○ Internal Interrupts and their Functions

The internal interrupts include one timer-counter interrupt and three serial interface interrupts.

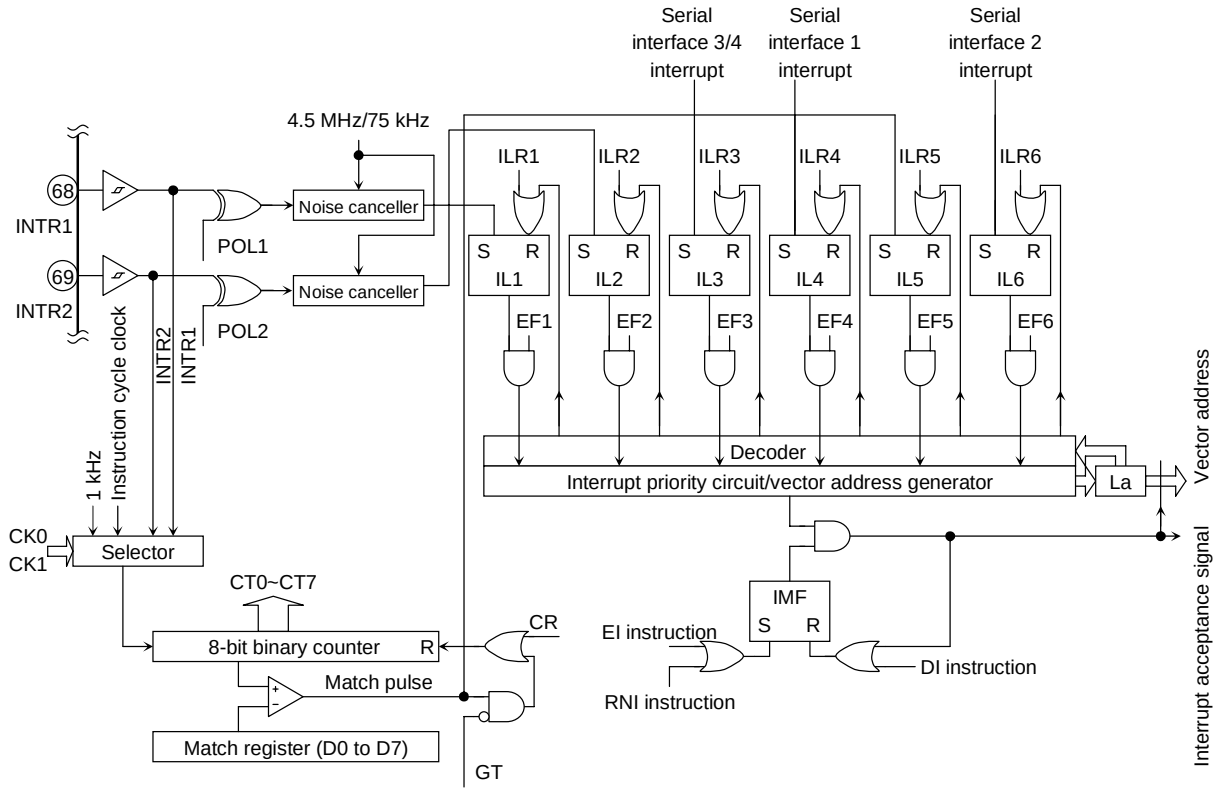
1. Timer-Counter Interrupt

The timer-counter interrupt is triggered at a match between the timer-counter value and the match register value. For details, see the section on the timer-counter function.

2. Serial Interface Interrupt

A serial interface interrupt is triggered at the completion of a serial operation. For details, see the section on serial interface functions.

3. Interrupt Block Structure



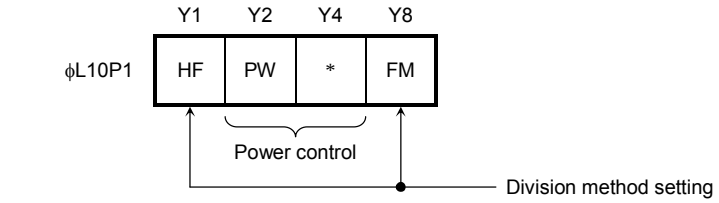
○ Programmable Counter

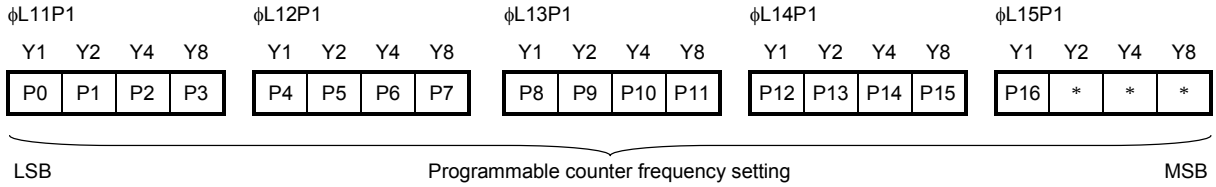
The programmable counter block consists of a 2-modulus prescaler, 4-bit and 13-bit programmable counters, and the ports used to control the block.

The programmable counters can be turned on and off by the contents of the reference ports or the $\overline{\text{HOLD}}$ input state.

1. Programmable Counter Control Ports

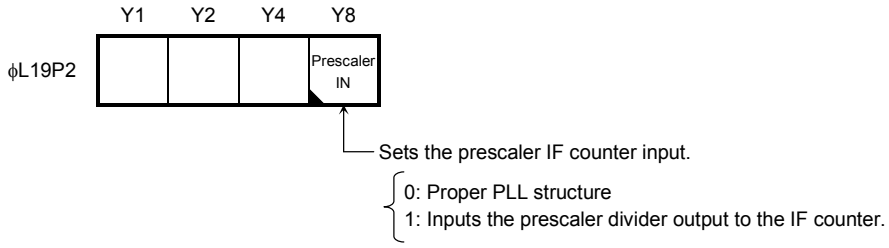
These ports control the frequency, division method, and the prescaler operating current and gain.





The division method and the prescaler power control are accessed using the OUT1 instruction with the operand [CN = 0H] on I/O map page 1.

The frequency is accessed using the OUT1 instruction with the operand [CN = 1 to 5H] on I/O map page 1. The frequency is set by writing to bit P16 (ϕL15P1). When the programmable counter data (P16) are set, all the data from P0 to P16 are updated. Therefore, always access P16 and set it last, even when changing only a portion of the data.



Setting the prescaler IF input: When this bit (Y8) is set to 1 the programmable counter is halted and the prescaler 1/15・16 is fixed to 1/16. Normally when setting a PLL, set 0 to the bit. (See the section on the IF counter.)

2. Setting Division Method

The HF and FM bits select the pulse swallow or direct division method.

The power control (PW) controls the amp and prescaler (1/2 + 1/15・16) gain. Set the power bit for each mode as in the following table.

As the table shows, there are five methods.

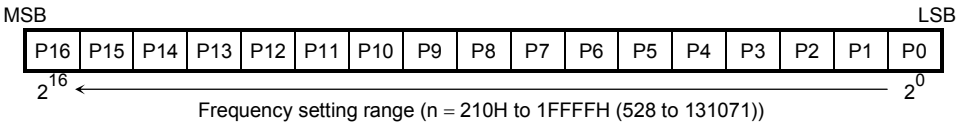
Mode	HF	PW	FM	Division Method	Reception Band Example	Operating Frequency Range	Input Pin	Frequency (Note)
LF	0	*	0	Direct division method	MW/LW	0.5~20 MHz	AMin	n
HF	1	*	0	(1/15•16) pulse swallow method	SW	1~30 MHz		
FM2	0	1	1		FM	10~60 MHz	FMin	
FM1	0	0	1			50~140 MHz		
FM2	1	1	1	(1/2 + 1/15•16) pulse swallow method		10~60 MHz		2・n
FM1	1	0	1			50~140 MHz		
VHF	1	0	1		TV (1 ch~12 ch)	50~230 MHz		

Note: n indicates the programmed divider value.

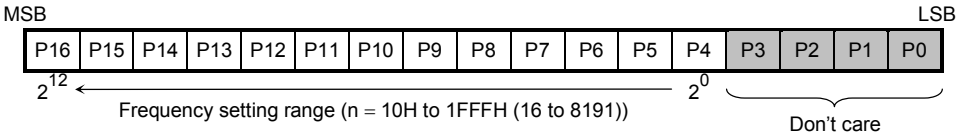
3. Setting Frequency

The programmable counter frequency is set in bits P0 to P16 using a binary value.

- Pulse swallow method (17 bits)



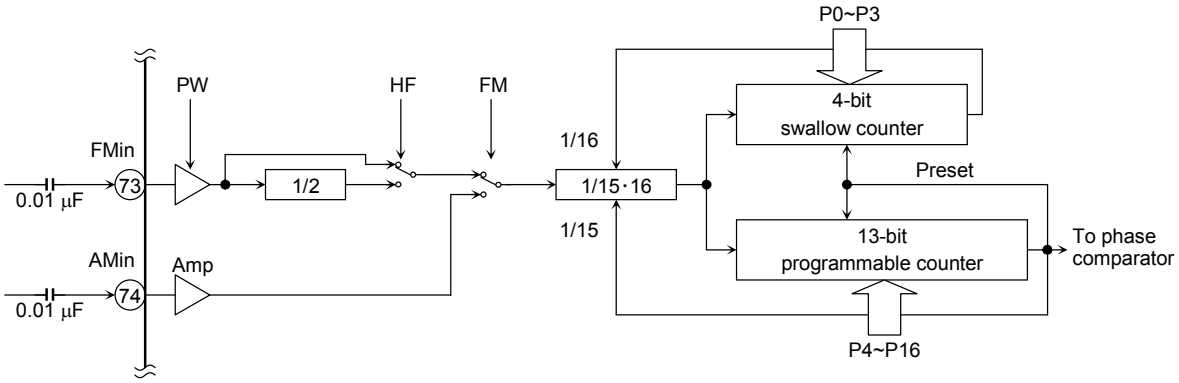
- Direct division method (13 Bits)



4. Programmable Counter Circuit Structure

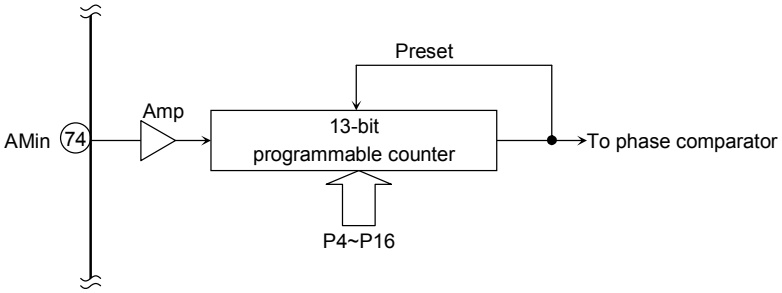
- Pulse Swallow Circuit Structure

  This circuit is made up of an amp, 1/2 prescaler, 1/15・16 2-modulus prescaler, a 4-bit swallow counter, and a 13-bit binary programmable counter. When using FMin input, a 1/2 divider is inserted before the prescaler.



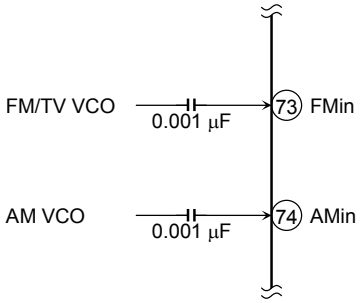
- Direct division circuit structure

  This circuit bypasses the prescaler and uses the 13-bit programmable counter.

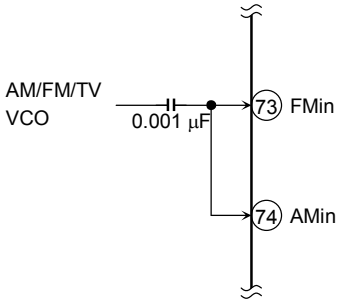


Note: The FMin and AMin pins incorporate amps. Connecting a capacitor permits low-amplitude operation. The input pins not selected by the division method are high impedance. In PLL Off mode the inputs are also high impedance. Therefore, the FMin and AMin pins can be used as a wired OR, as shown below.

Note: In PLL Off mode, the entire programmable counter block is halted. At this time, the contents of all the control ports are saved.



Example of circuit using VCO in both FM and AM bands.



Example of circuit using VCO shared between FM and AM bands.

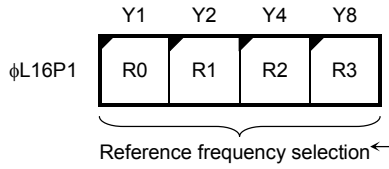
○ Reference Frequency Divider

When the 75-kHz oscillator clock is selected as a peripheral clock, the reference frequency divider divides the frequency of the external 75-kHz crystal oscillator to generate seven PLL reference frequency signals: 1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.25 kHz, 12.5 kHz, and 25 kHz. When the 4.5-MHz oscillator clock is selected, the reference frequency divider divides the frequency of the external 4.5-MHz crystal oscillator to generate a further four PLL reference frequency signals: 9 kHz, 10 kHz, 50 kHz, and 100 kHz, making a total of 11 reference frequency signals. The frequency is selected by the reference port data.

The selected signal is supplied as the reference frequency for the phase comparator, which is described next. The PLL is turned on and off according to the reference port setting.

1. Reference Port

The reference port is an internal port used to select the reference frequency signal, and there are 11 available frequencies. This port is accessed by the OUT1 instruction with the operand [CN = 6H] (øL16P1) on I/O map page 1. When the contents of the reference port are all 1, the programmable counter, IF counter, reference counter, and phase comparator are all halted and the PLL is turned off. When the reference port is set, the frequency setting data of the programmable counter are updated. Therefore, when setting the reference port, be sure first to set the programmable counter frequency, then the reference port.



R3	R2	R1	R0		Reference Frequency
0	0	0	0	0	1 kHz
0	0	0	1	1	3 kHz
0	0	1	0	2	3.125 kHz
0	0	1	1	3	5 kHz
0	1	0	0	4	6.25 kHz
0	1	0	1	5	12.5 kHz
0	1	1	0	6	25 kHz
0	1	1	1	7	9 kHz
1	0	0	0	8	10 kHz
1	0	0	1	9	50 kHz
1	0	1	0	10	100 kHz
1	0	1	1	11	Prohibited
1	1	0	0	12	Prohibited
1	1	0	1	13	Prohibited
1	1	1	0	14	Prohibited
1	1	1	1	15	PLL off mode

○ Phase Comparator, Lock Detection Port

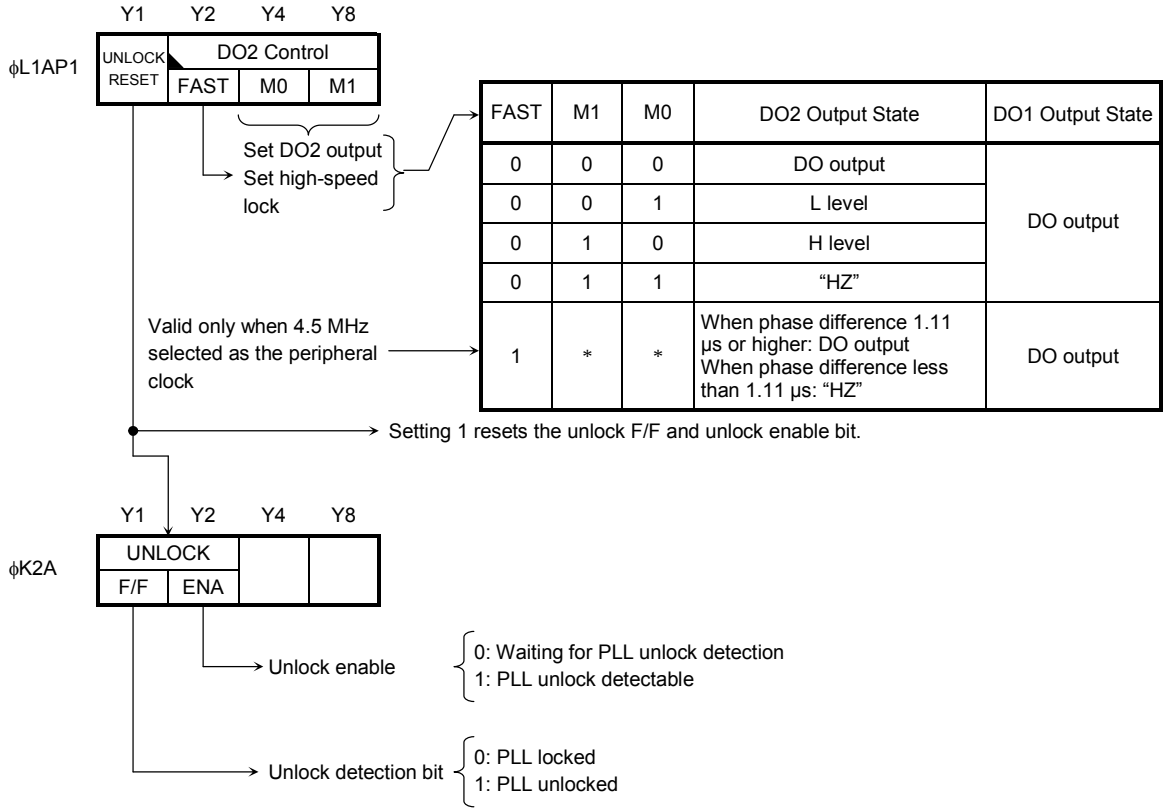
The phase comparator compares the reference frequency supplied by the reference frequency divider with the output frequency of the programmable counter, and outputs the phase difference. This is used to control the VCO (voltage control oscillator) via the low pass filter so as to match the frequencies and phases between the two signals.

The phase comparator outputs in parallel to the tristate buffered DO1 and DO2 pins. This enables the optimal filter constants to be designed for FM, VHF, and AM bands.

Also, the DO2 pin can be set as a general-purpose output by the DO2 control port. By using the DO1 and DO2 pins, the PLL lock loop lockup time characteristics can be improved.

The unlock detection port can be used to detect the PLL lock state.

1. DO1 Control Port, Unlock Detection Port



FAST	M1	M0	DO2 Output State	DO1 Output State
0	0	0	DO output	DO output
0	0	1	L level	
0	1	0	H level	
0	1	1	"HZ"	
1	*	*	When phase difference 1.11 μs or higher: DO output When phase difference less than 1.11 μs: "HZ"	DO output

The M0 and M1 bits of the DO2 control port set DO2 as a general-purpose output port and set DO2 to high impedance. The FAST bit sets the high-speed lock.

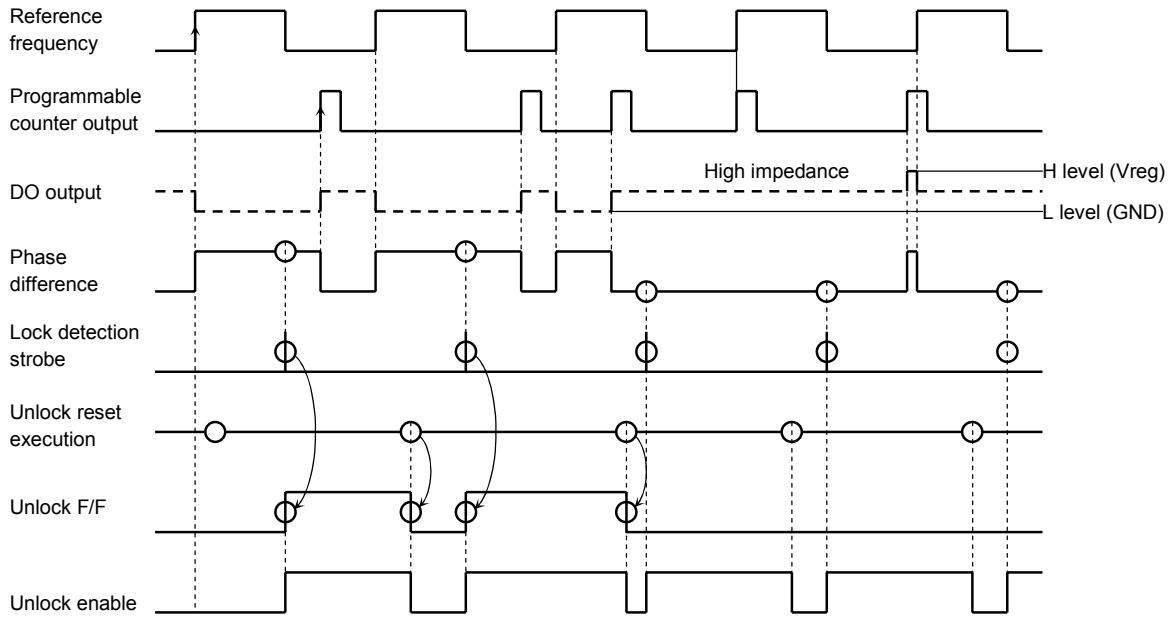
The unlock F/F detects the phase difference between the output frequency of the programmable counter and the reference frequency when the phase is approximately 180°. If the phase does not match, that is, if the PLL is unlocked, the unlock F/F is set. Also, setting the unlock reset bit to 1 resets the unlock F/F.

To detect the phase difference at the reference frequency period, reset the unlock F/F, then access the unlock F/F after waiting for an interval longer than the reference frequency period. An enable bit is supplied for this purpose. After confirming that the unlock enable bit is set to 1, access the unlock F/F.

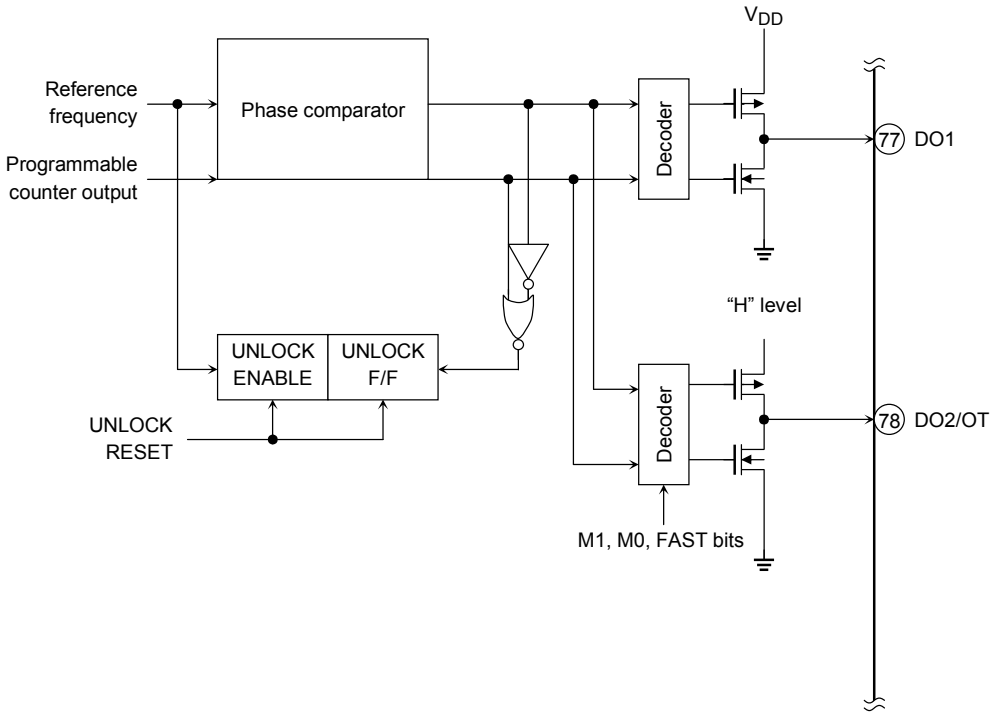
Note: When the PLL is off and the DO output is set, the DO output is high impedance. However, when the DO2 pin outputs an L or H level signal, this state is held if PLL Off mode or Clock Stop mode is set.

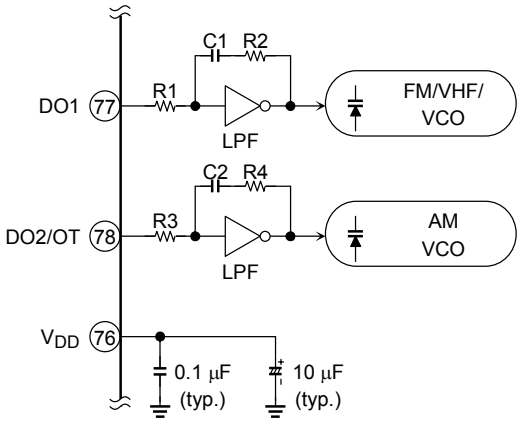
Note: The high-speed lock is effective only when a 4.5-MHz peripheral clock is selected.

2. Phase Comparator, Unlock Port Timing

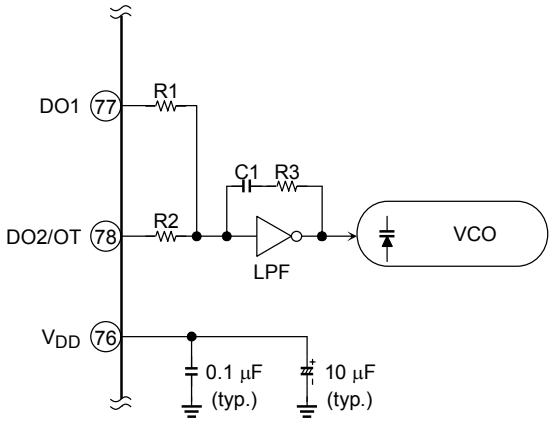


3. Phase Comparator, Unlock Port Circuit Structure





When setting different filter constants for each band



When using the same low pass filter for both bands (High-Speed Lock mode)

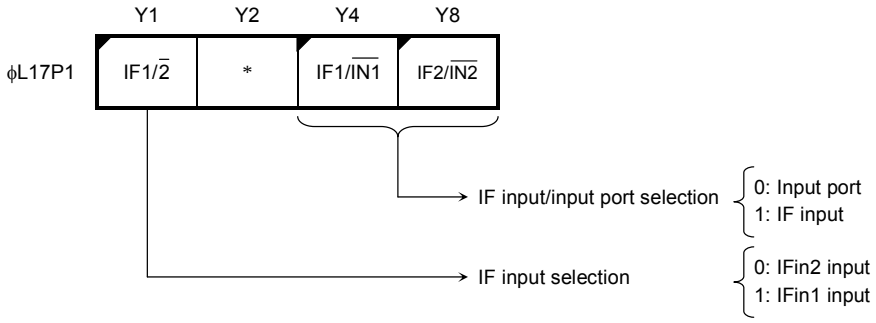
Note: The filter circuit shown above is an example for your reference. Design your own circuit in accordance with the band structure of your system and the characteristics you require.

○ IF Counter

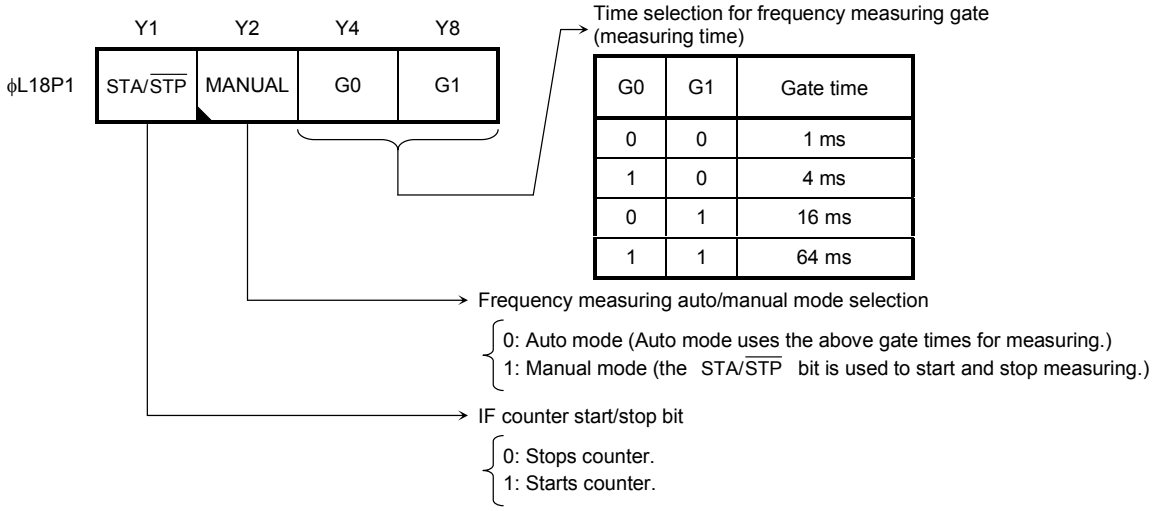
This is a 20-bit general-purpose intermediate frequency (IF) counter used for such purposes as counting the FM or AM intermediate frequency and detecting the auto-stop signal during auto tuning.

The FMin/AMin input can be input via the prescaler to the IF counter. The IF counter can also be used for detecting the reception frequency by measuring the analog tuner's VCO.

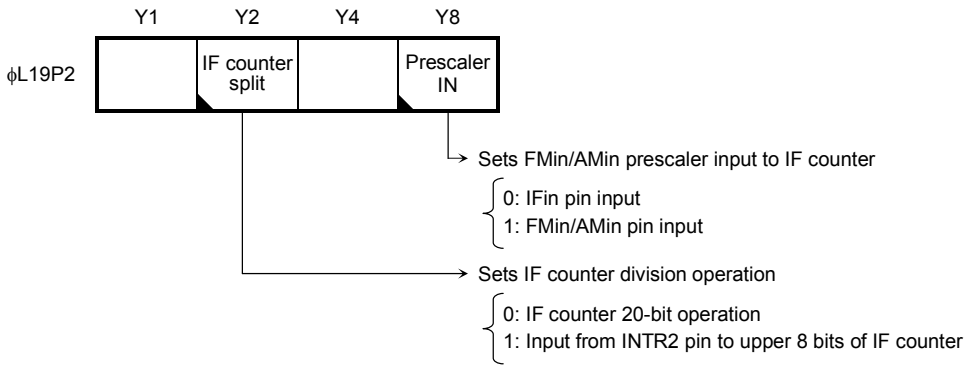
1. IF Counter Control Port, Data Port



Note: When set as an input port, the frequency can be detected by inputting CMOS input to the IF counter.

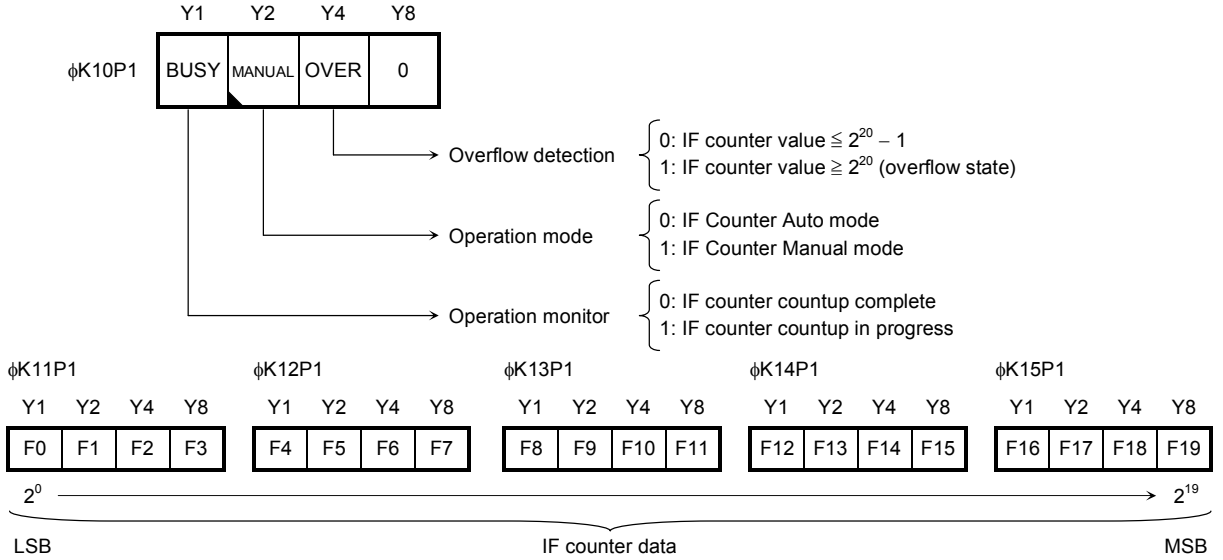


G0	G1	Gate time
0	0	1 ms
1	0	4 ms
0	1	16 ms
1	1	64 ms



Note: If the IF counter input is set to prescaler input, when setting the pulse swallow method, the 1/15•16 prescaler is fixed to 1/16 division and this frequency is input to the IF counter.

Note: When the IF counter is set for division operations, the upper 8-bit counter is input from the INTR2 pin. However, gate time (Auto mode) cannot be set for these upper eight bits only. To reset this counter, set the STA/$\overline{STP}$ bit to 1.



Note: With IF input selected, the IF input amp goes off in PLL Off mode. To use the IF counter in PLL Off mode, select as an input port (CMOS input).

Note: The input amp not selected by the IF 1/2 bit goes off. When the input amp is off, input is set to high impedance.

(1) IF Counter Auto Mode

When IF counter Auto mode is selected, the MANUAL bit is set to 0 and the gate time is set based on the IF input frequency band to be measured. Setting the STA/STP bit to 1 starts the IF counter, inputs the clock during the specified gate time, counts the number of input pulses, then completes. To determine when the IF counter has finished counting, check the BUSY bit. Note that the OVER bit is set to 1 if the count equals or exceeds 2^{20} input pulses.

To measure the input frequency, load the F0 to F19 IF data when the BUSY and OVER bits are both 0.

(2) IF Counter Manual Mode

Use Manual mode to measure the frequency by controlling the gate time with an internal time base (e.g., 10 Hz).

To enter Manual mode, set the MANUAL bit to 1. At this time the gate time setting is "don't care". To start the count, set the STA/$\overline{\text{STP}}$ bit to 1. Setting the STA/$\overline{\text{STP}}$ bit to 0 terminates the count and loads the data in binary format.

(3) IF Counter Input and Division Setting

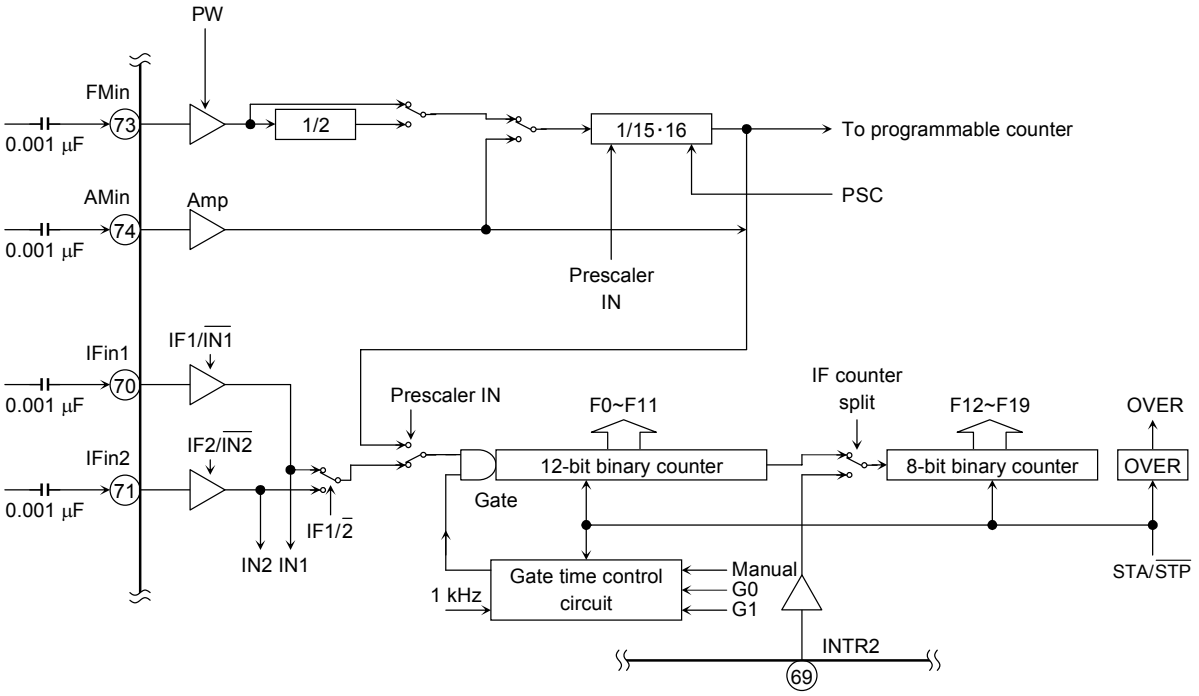
Intermediate frequency (IF) measuring is normally based on the frequency of a signal input to the IFin1 or IFin2 input pins. These pins incorporate input amps and can be used for low-amplitude operation. In addition, input to the IF counter can be set as below. Use the input in accordance with the specifications.

IF1/$\overline{2}$	IF1/$\overline{\text{IN1}}$	IF2/$\overline{\text{IN2}}$	IF Counter Split	Prescaler IN	IF Input Settings		
1	1	*	0	0	IFin1 input (amp operation)		
*	0	*	0	0	IN1 (IFin1) input (CMOS input)		
0	*	1	0	0	IFin2 input (amp operation)		
*	*	0	0	0	IN2 (IFin2) input (CMOS input)		
*	*	*	0	1	VHF mode	FMin input (frequency divided by 32/16)	(Note)
					FM1/FM2 mode		
					HF mode	AMin input (frequency divided by 16)	
					LF mode	AMin input (input frequency)	
*	*	*	1	*	The upper 8 bits only are input from the INTR2 pin.		

Note: For the input frequency range when setting the prescaler input, see the section on the programmable counter.

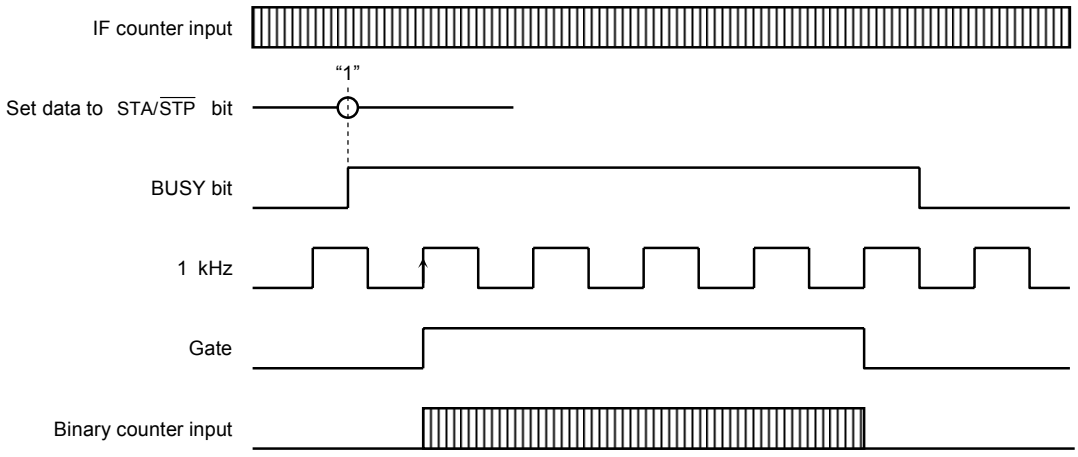
2. IF Counter Structure

The IF counter block consists of an input amp, a gate time control circuit, and a 12- + 8-bit binary counter. The FMin/AMin prescaler clock can be input to the IF counter.



Note: All the binary counters of the IF counter operate on the rising edge.

Note: The prescaler 1/15•16 division is fixed to 1/16 when the IF counter is input. FMin input division is 1/32; AMin input division is 1/16 or direct input can be used.



Example of IF Counter Auto Mode Operation Timing

○ LCD Driver

The LCD driver consists of 38 pins: 30 pins (OT1/COM1 to OT30/S26) that also function as output ports and eight pins (P9-0/S27 to P10-3/S34) that also operate as I/O ports.

The LCD driver has 1/4, 1/3, and 1/2 duty and 1/3 and 1/2 bias drive and can be selected between two frame frequencies.

When 1/4 duty is set, up to 136 segments can be displayed using a matrix of COM1 to 4 and S1 to 34. At 1/3 duty, a maximum of 105 segments can be displayed by a matrix of COM1 to 3 and S1 to 35. At 1/2 duty, up to 72 segments can be displayed by a matrix of COM1, 2 and S1 to 36.

After a system reset, the pins that also function as output ports are set to output ports, and the pins that are also I/O ports are set to I/O port inputs. The LCD OFF bit is used to switch the output ports and LCD driver, switching 30 ports at a time. The I/O ports and segment outputs are switched individually.

1. LCD Driver Ports

The LCD driver control ports consist of a selection port, segment I/O selection ports, segment data ports, and an LCD driver control port. These ports are accessed by the OUT2 instruction with the operand [CN = CH~FH].

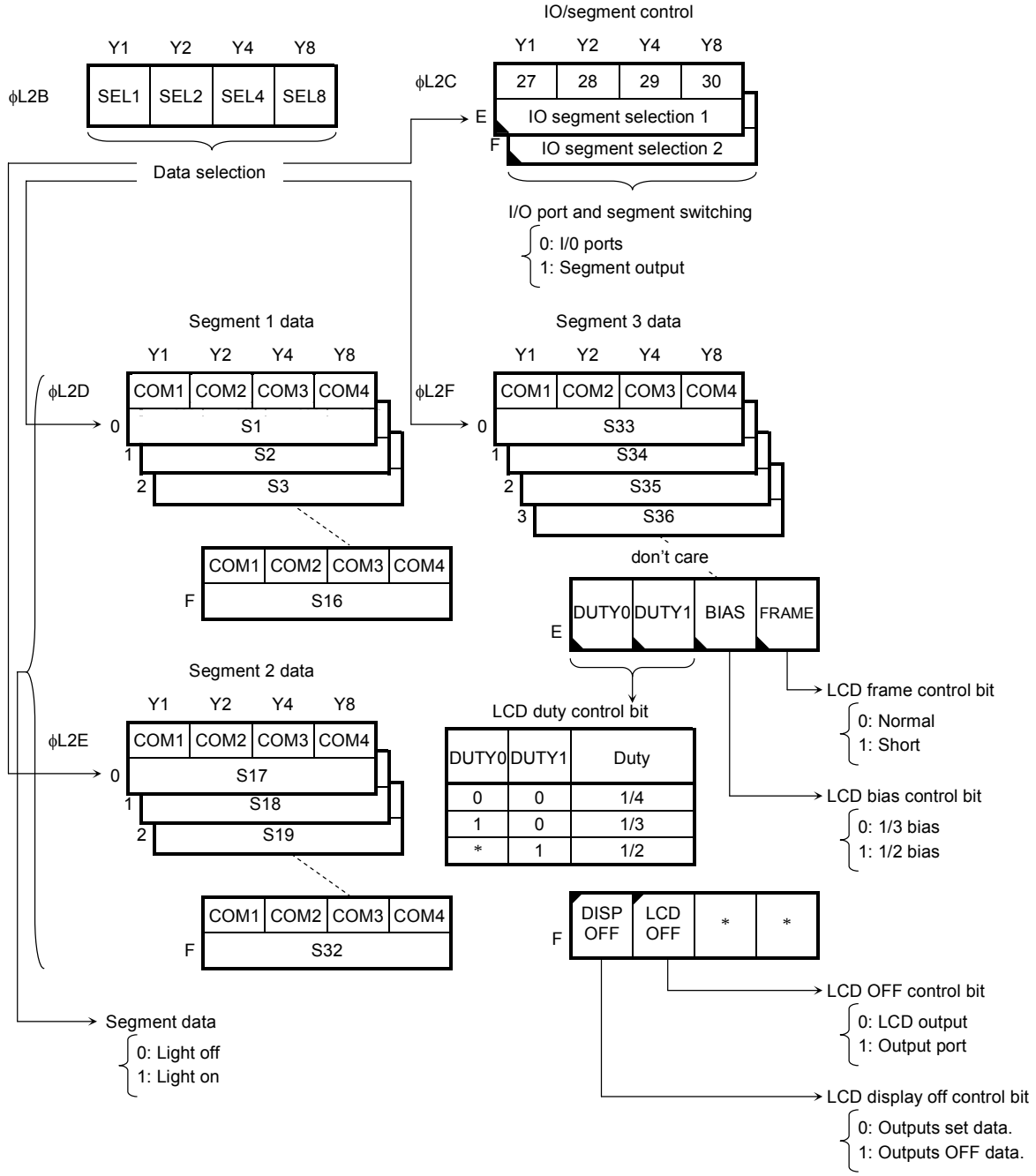
Pins S27 to S34 can also operate as an I/O port under the control of the segment I/O selection ports (ϕL2CE, ϕL2CF). Setting the port to 1 sets segment output, and setting the port to 0 sets the pins as an I/O port. (See the section on I/O ports.)

Set the LCD driver segment data using the segment data ports (ϕL2D, ϕL2E, ϕL2F). Setting the segment data port to 0 turns the LCD display off; setting 1 turns the LCD display on. The LCD drive mode is selected by the LCD driver control port (ϕL2FE), while the LCD driver control port 2 (ϕL2FF) is used to switch between the LCD driver and output port (LCD OFF bit) and to turn the LCD display completely off (DISP OFF bit).

The DISP OFF bit can turn the whole LCD display off without setting segment data. Setting this bit to 1 outputs the turned off waveforms to all the segments. Setting DISP OFF to 0 outputs the set segment data. The segment data settings are independent of the DISP OFF bit settings.

The LCD OFF bit switches the LCD driver on/off. Setting this bit to 1 turns the LCD driver off and sets OT1/COM1 to OT30/S26 pins as output ports (OT1 to OT30). Setting the LCD OFF bit to 0 activates the LCD driver and sets the OT1/COM1 to OT30/S26 pins to LCD driver outputs (COM1 to S26). The segment data settings are independent of the LCD OFF bit settings.

These data can be divided/indirectly specified, and set using the data selection port (ϕL2B). This port is incremented by 1 at each access of segment data port ϕL2C, segment data ports øL2D to ϕL2F, and the LCD driver control port. Accordingly, these data can be repeatedly set after the data selection port is set.



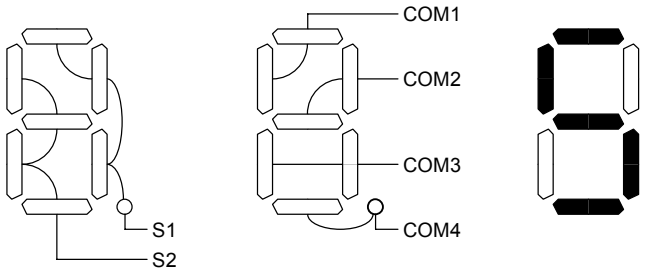
Note: When the DISP OFF bit is set to 1, all segment data are off and the whole display is off.

Note: The segment data control whether the segments corresponding to the common and segment outputs are lit or not.

Note: During Clock Stop mode and for 100 ms after a system reset, all common and segment outputs are fixed to L.

Note: The data selection port is automatically incremented by 1 whenever ϕLC2, ϕL2D, ϕL2E, ϕL2F, ϕL3B, or ϕK3B on the I/O map are accessed.

(1/4 duty, 1/3 bias, frame type: normal)



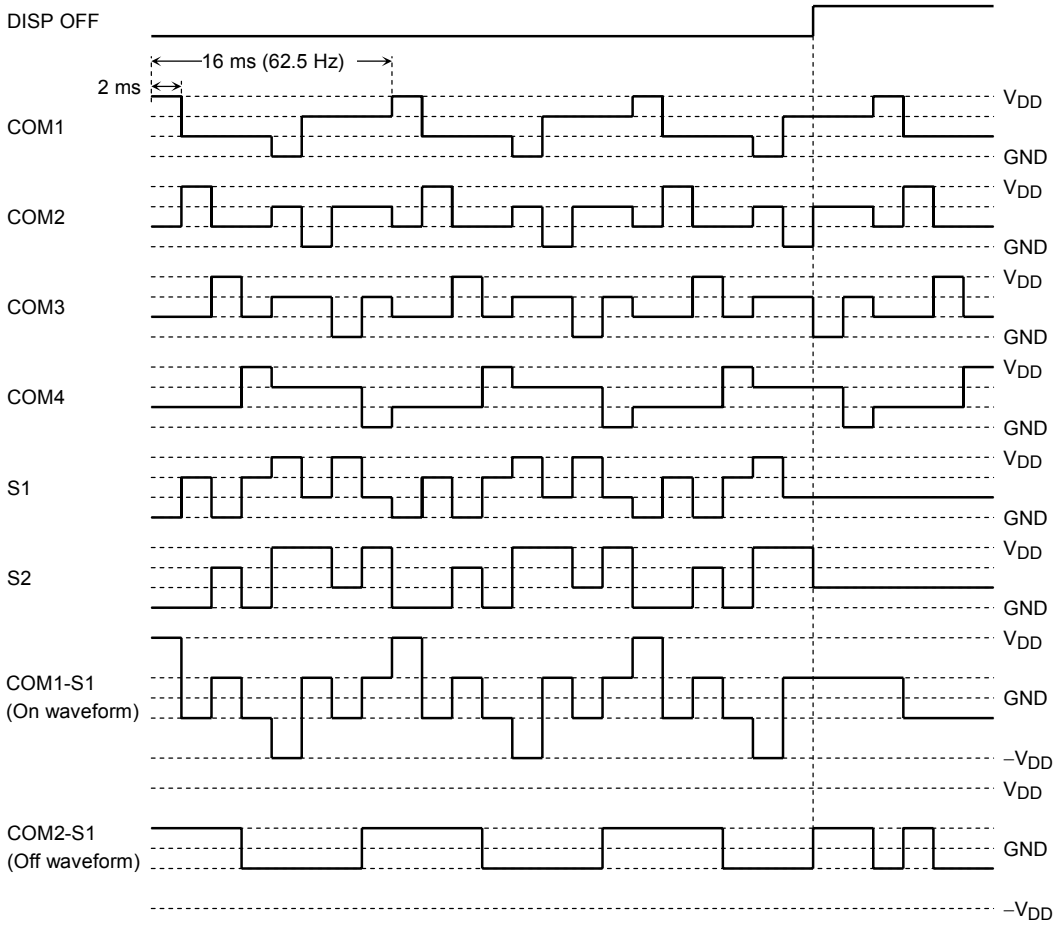
Segment data example

Segment data-1 (φL2D)

	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	0	1	0

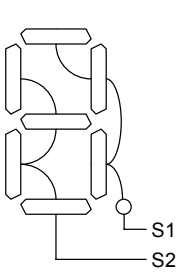
1	COM1	COM2	COM3	COM4
(S2)	1	1	0	1

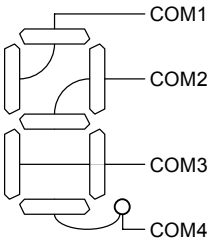
Data selection (φL2B)

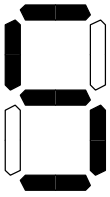


The LCD driver waveform potential output is GND, 1/3 V_{DD}, 2/3 V_{DD}, and V_{DD} level.
The bias voltage is 1/3 V_{DD} and 2/3 V_{DD} at 1/3 bias, and 1/2 V_{DD} at 1/2 bias. (See the following page.)

(1/4 duty, 1/2 bias, frame type: normal)







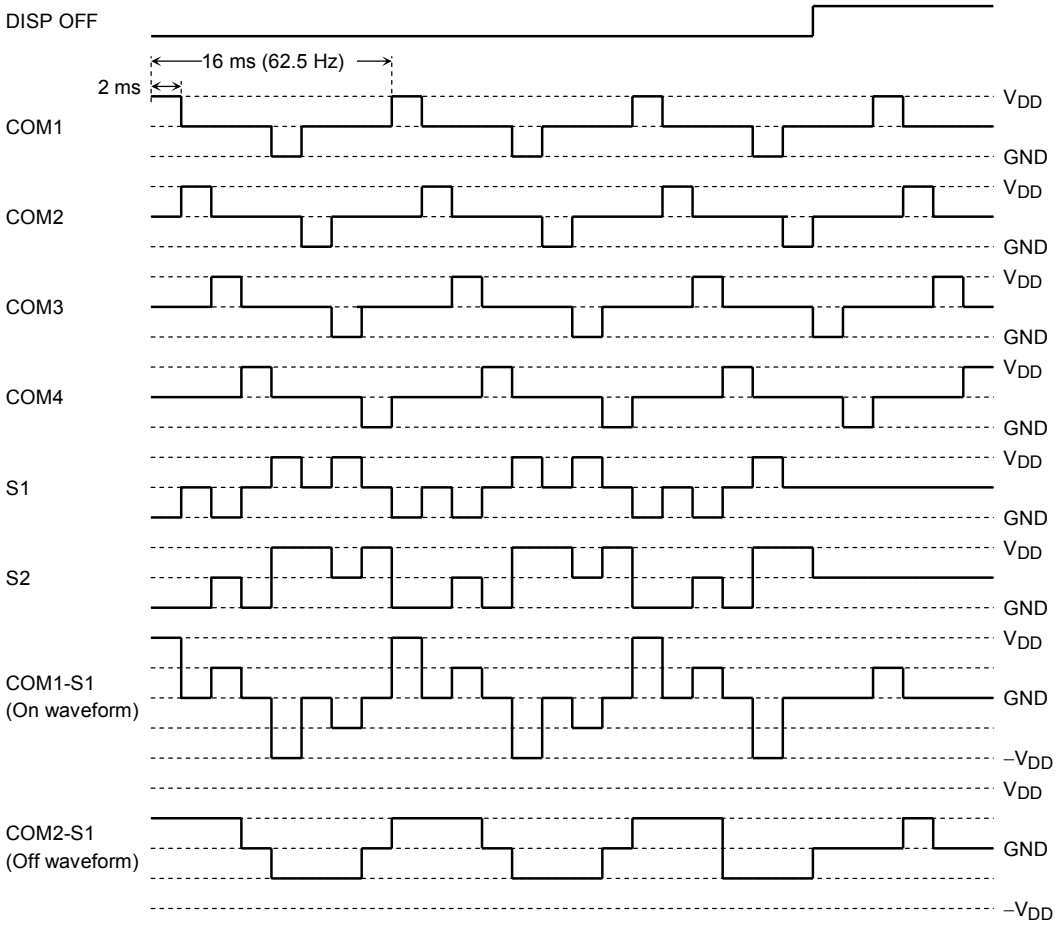
Segment data example

Segment data-1 (ϕL2D)

	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	0	1	0

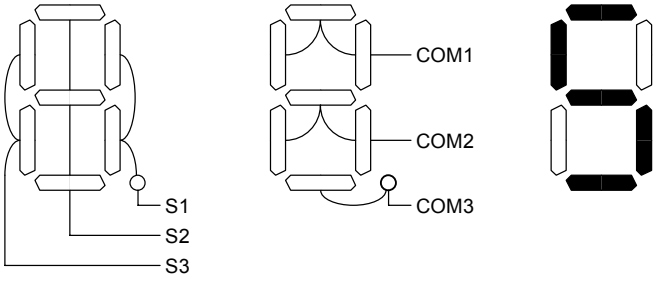
1	COM1	COM2	COM3	COM4
(S2)	1	1	0	1

Data selection (ϕL2B)



The LCD driver waveform potential output is GND, 1/2 V_{DD}, and V_{DD} level.

(1/3 duty, 1/3 bias, frame type: normal)

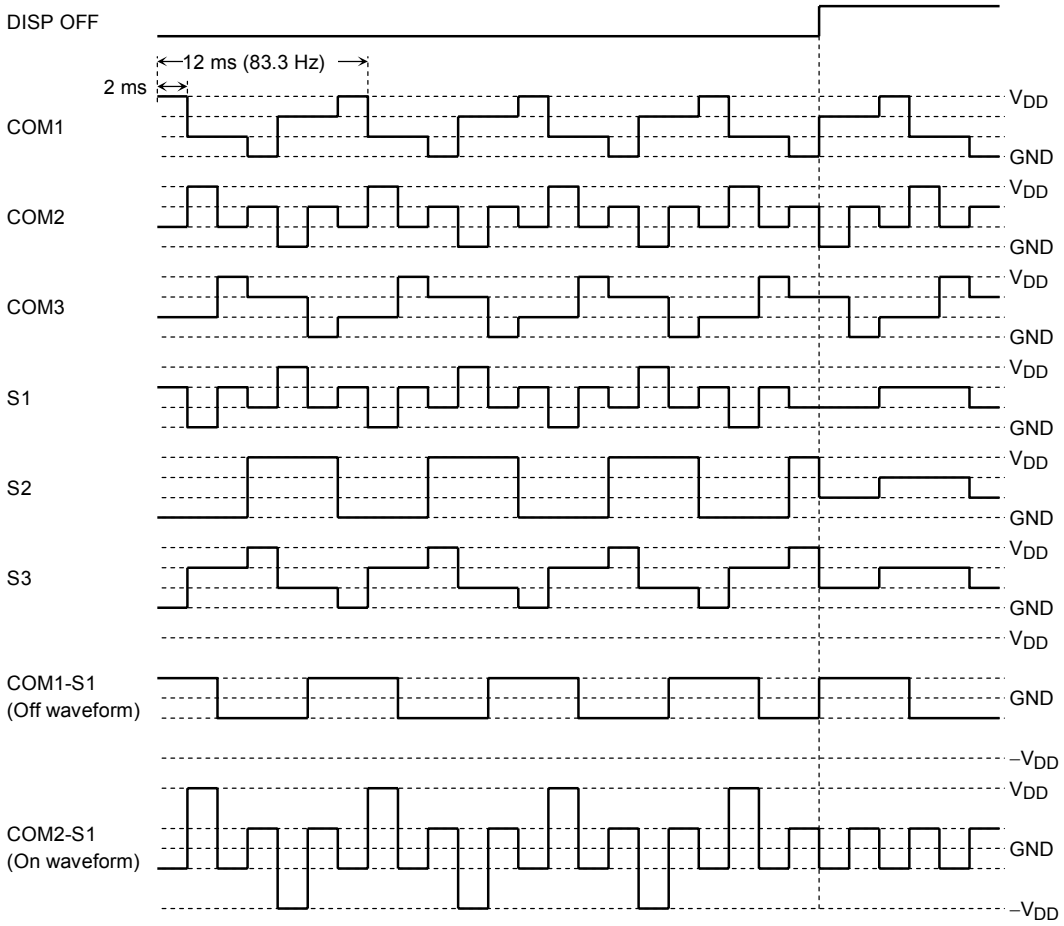


Segment data example

Segment data-1 (ϕL2D)

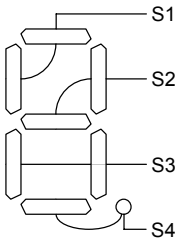
	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	0	1	0	*
1	COM1	COM2	COM3	COM4
(S2)	1	1	1	*
2	COM1	COM2	COM3	COM4
(S3)	1	0	0	*

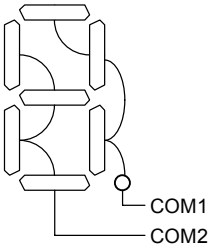
Data selection (ϕL2B)

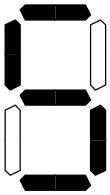


The LCD driver waveform potential output is GND, 1/3 V_{DD}, 2/3 V_{DD}, and V_{DD} level.
The bias voltage is 1/3 V_{DD} and 2/3 V_{DD} at 1/3 bias, and 1/2 V_{DD} at 1/2 bias.

(1/2 duty, 1/3 bias, frame type: normal)





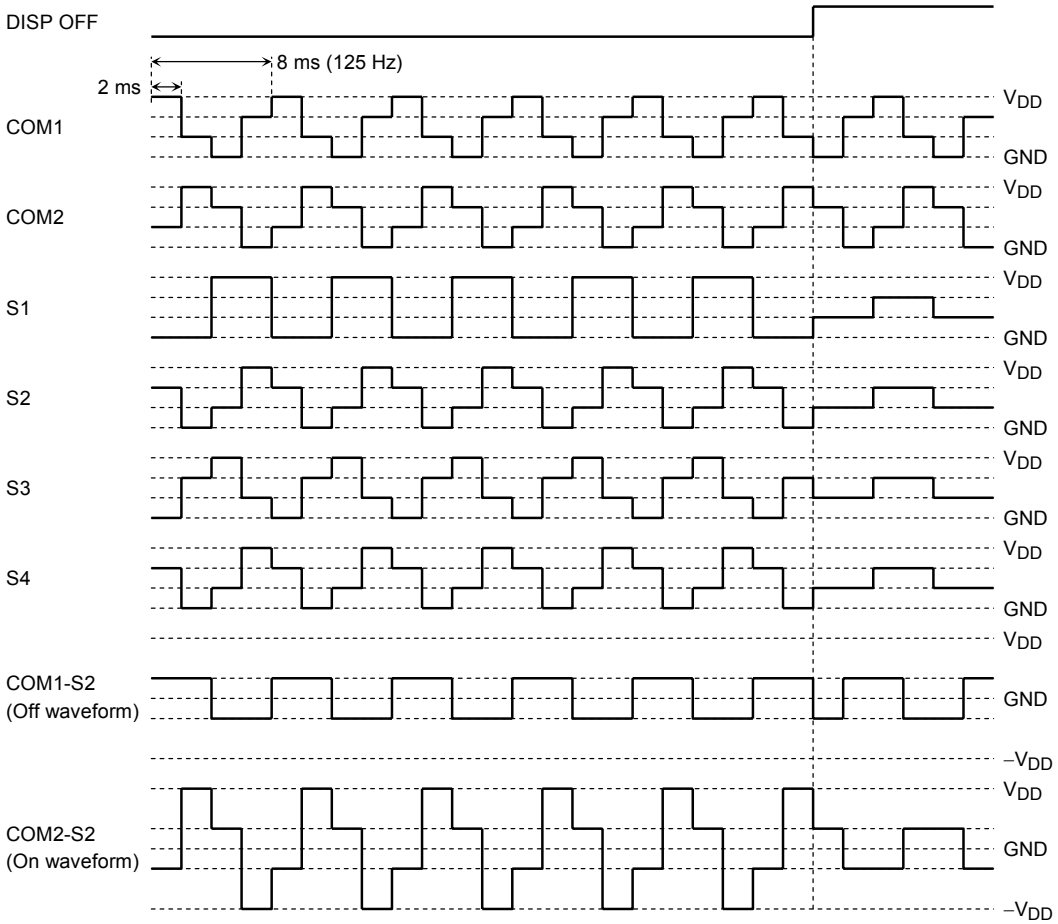


Segment data example

Segment data-1 (ϕL2D)

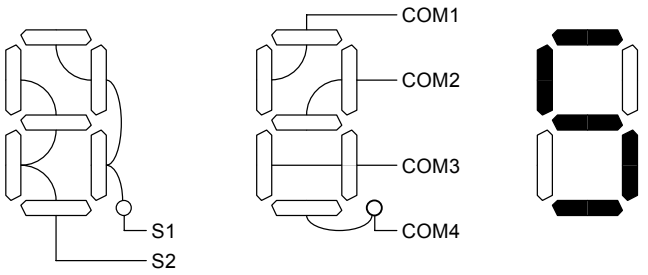
	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	1	*	*
1	COM1	COM2	COM3	COM4
(S2)	0	1	*	*
2	COM1	COM2	COM3	COM4
(S3)	1	0	*	*
3	COM1	COM2	COM3	COM4
(S4)	0	1	*	*

Data selection (ϕL2B)



The LCD driver waveform potential output is GND, 1/3 V_{DD}, 2/3 V_{DD}, and V_{DD} level.
The bias voltage is 1/3 V_{DD} and 2/3 V_{DD} at 1/3 bias, and 1/2 V_{DD} at 1/2 bias.

(1/4 duty, 1/3 bias, frame type: short)



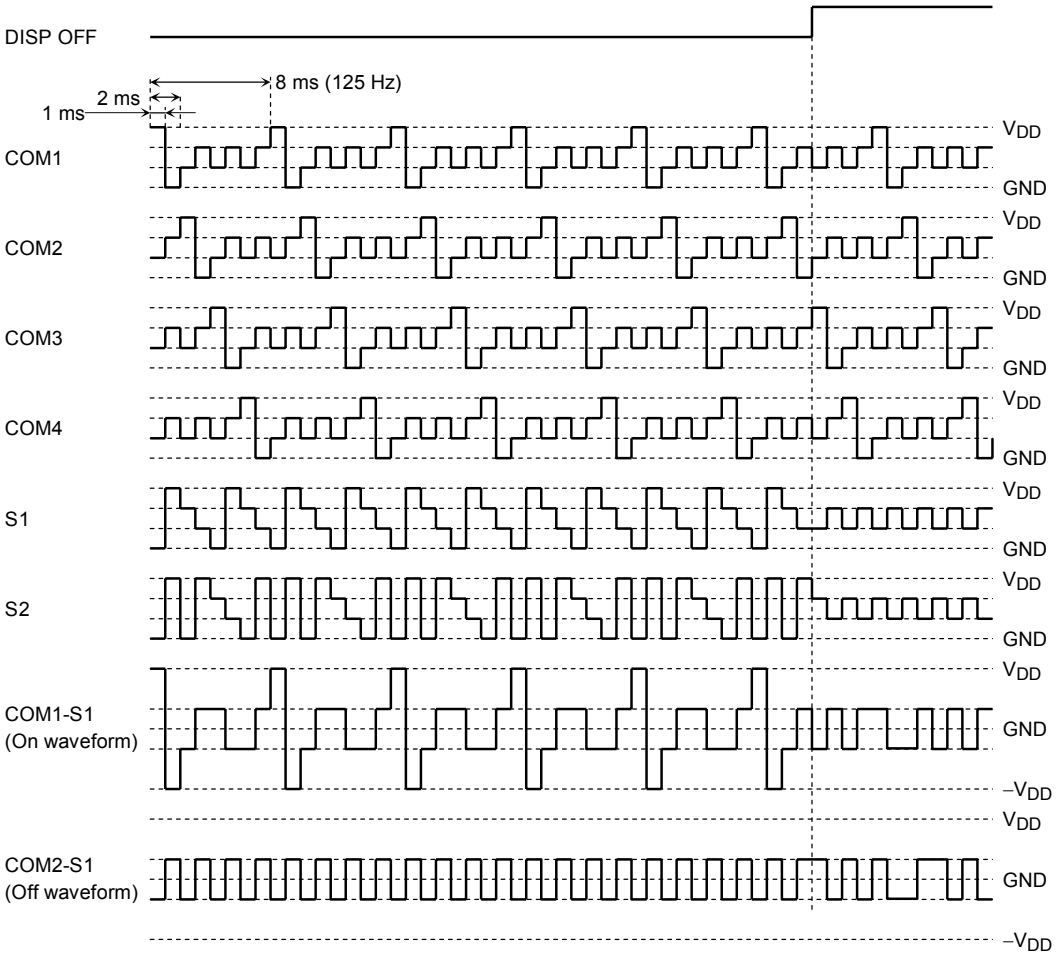
Segment data example

Segment data-1 (ϕL2D)

	Y1	Y2	Y4	Y8
0	COM1	COM2	COM3	COM4
(S1)	1	0	1	0

1	COM1	COM2	COM3	COM4
(S2)	1	1	0	1

Data selection (ϕL2B)



The LCD driver waveform potential output is V_{DD} and GND level, and bias voltages are 1/3 and 2/3 V_{DD} and GND level.

○ Serial Interface (SO1 to 4)

The TC9325FG has four serial interfaces: SIO1, 2, 3, and 4.

Serial interfaces 1 and 2 also function as I/O port 4, while interfaces 3 and 4 also operate as I/O port 5.

SIO1 and SIO3 are 3-line serial interfaces. SIO1 and SIO3 use pins SI(1/3), SO(1/3), and SCK(1/3) to input or output 4-bit or 8-bit data on an internal or external serial clock. At completion of the serial interface operation an interrupt is generated.

SIO2 is a 2-line serial interface. SIO2 uses pins SI2 or SO2 and pin SCK2 to input 26-bit data on an external serial clock. SIO2 has a function for decoding input serial data. An interrupt is generated on each input serial clock edge.

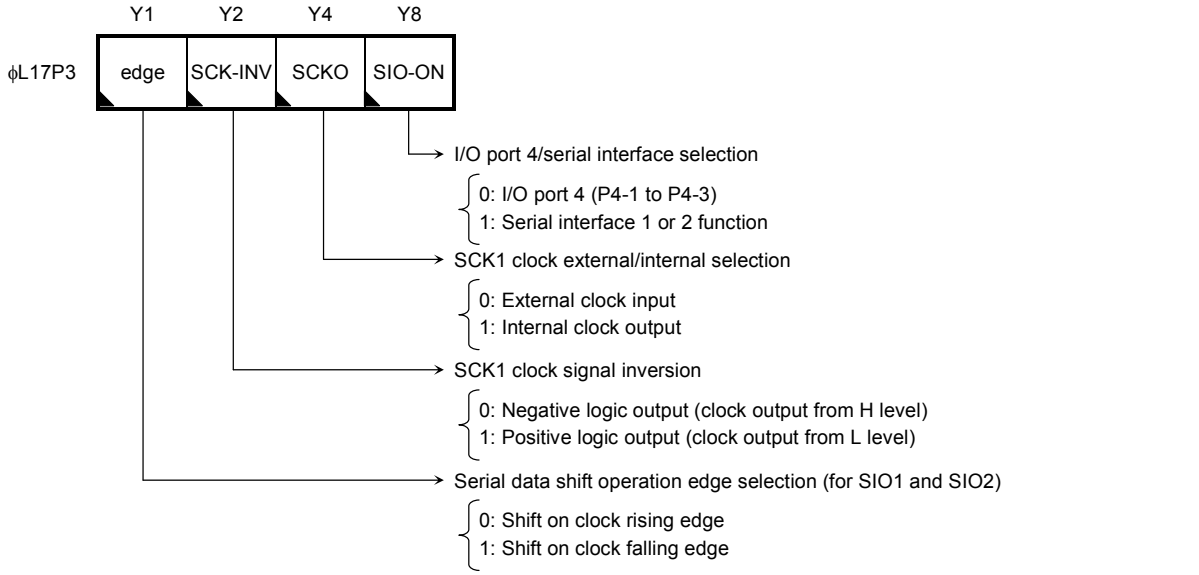
SIO4 is a 2-line serial interface. SIO4 uses pins SO4 and SCK4 to input or output 4-bit or 8-bit data on an internal or external serial clock. On completion of the serial interface operation an interrupt is generated.

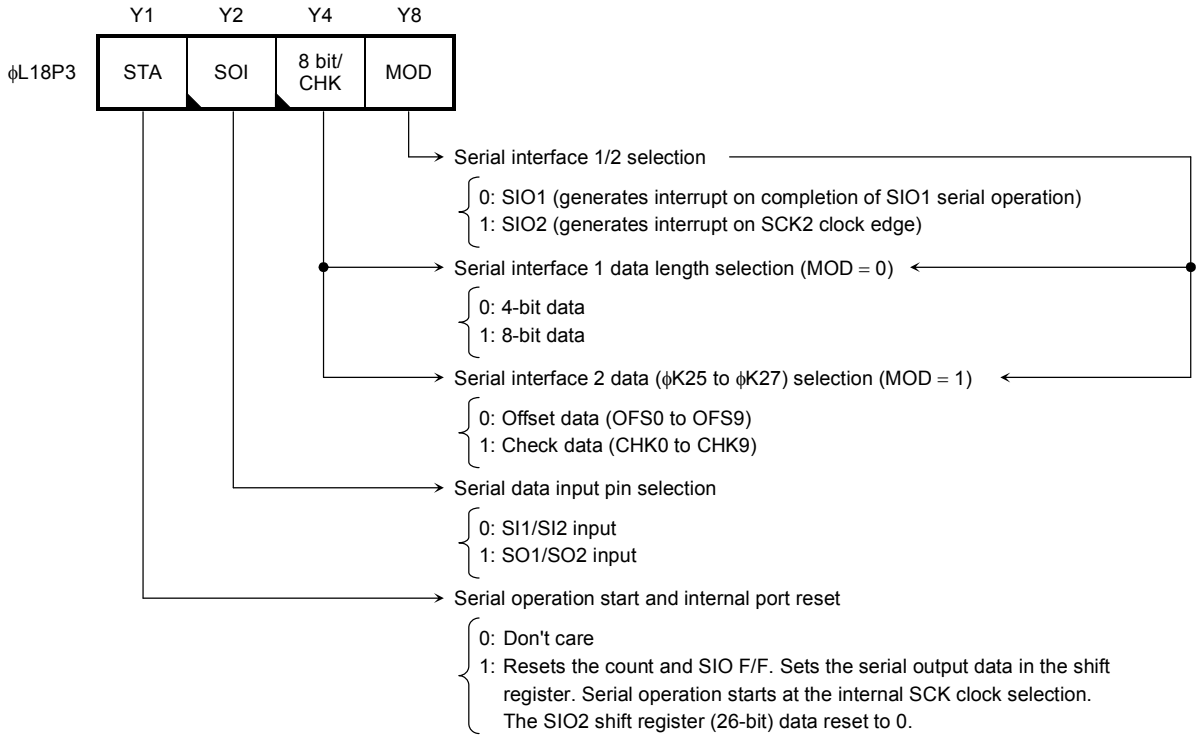
	As I/O Port	Type	Data	Data Length	When Interrupt Generated
SIO1	P4	3-line	Input/output	4/8 bits	On completion of serial interrupt operation
SIO2	P4	2-line	Input	26 bits	On each serial clock edge
SIO3	P5	3-line	Input/output	4/8 bits	On completion of serial interrupt operation
SIO4	P5	2-line	Input/output	4/8 bits	On completion of serial interrupt operation

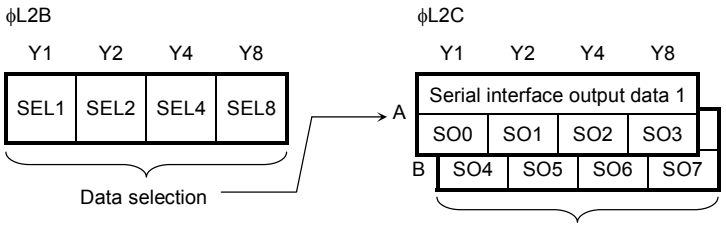
	Pin		
I/O port	P4-1	P4-2	P4-3
SIO1	SI1	SO1	SCK1
SIO2	SI2	SO2	SCK2

	Pin		
I/O port	P5-1	P5-2	P5-3
SIO3	SI3	SO3	SCK3
SIO4	—	SO4	SCK4

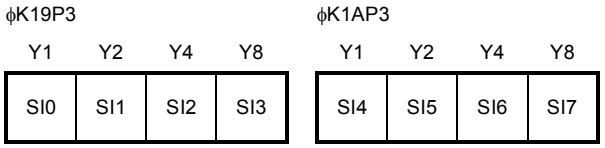
1. Serial Interface 1/2 (SIO1, SIO2) Control Port, Data Port





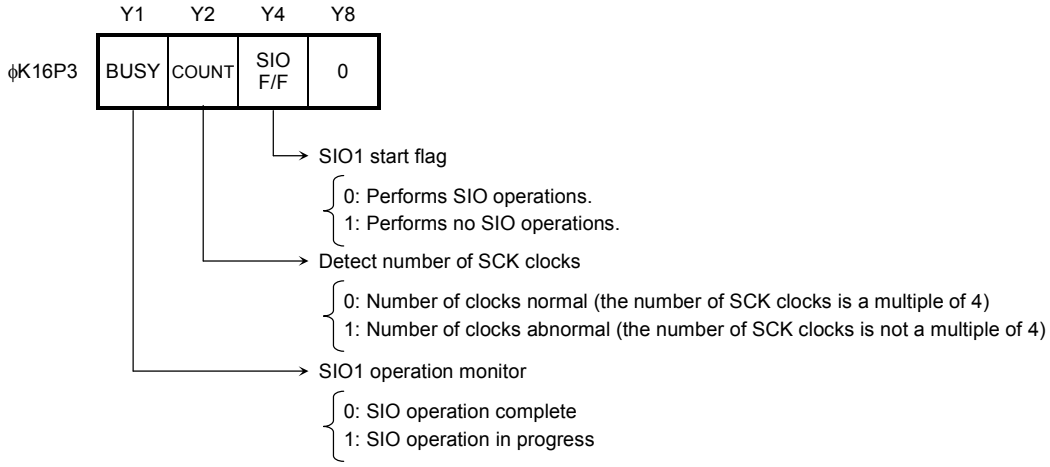


Serial output data: The data set in this port are output to the serial interface.



Note: The serial interface input data are accessed directly from the shift register.

Serial input data: The data input to the serial interface are loaded to data memory.



The serial interface pins can also function as I/O port 4 pins P4-1, P4-2, and P4-3. Setting the SIO ON bit to 1 sets these I/O port 4 pins as the SI1/SI2, SO1/SO2, and SCK1/SCK2 pins, respectively.

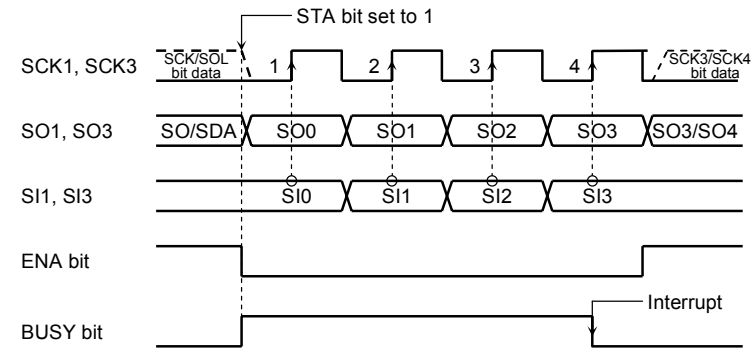
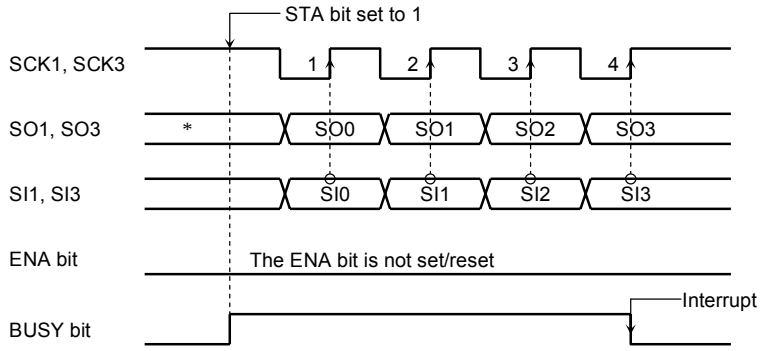
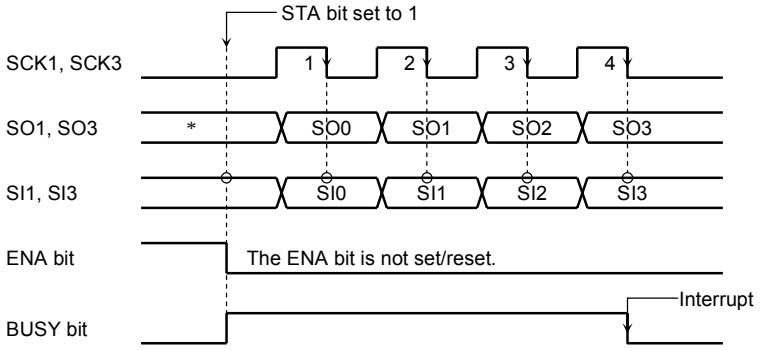
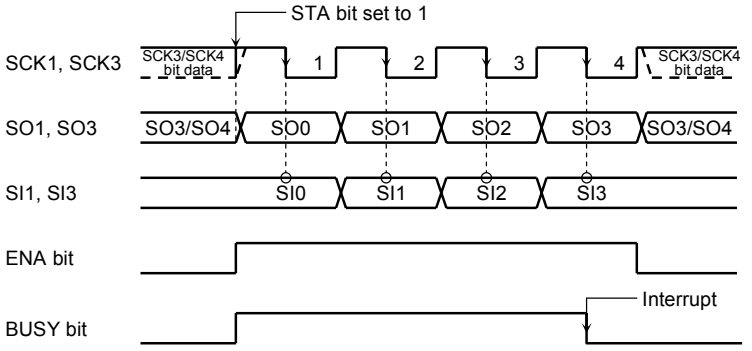
Note: All the serial interface inputs incorporate Schmitt trigger circuits.

Note: Even when the serial interface is selected, the SI pin (P4-1) can still be used as an I/O port and therefore can be used for such purposes as inputting/outputting SIO strobe signals.
When setting this pin as a serial input pin, set the P4-1 output data to 1 to set the pin as an input.

1) EDGE, SCK-INV, SCKO Bits

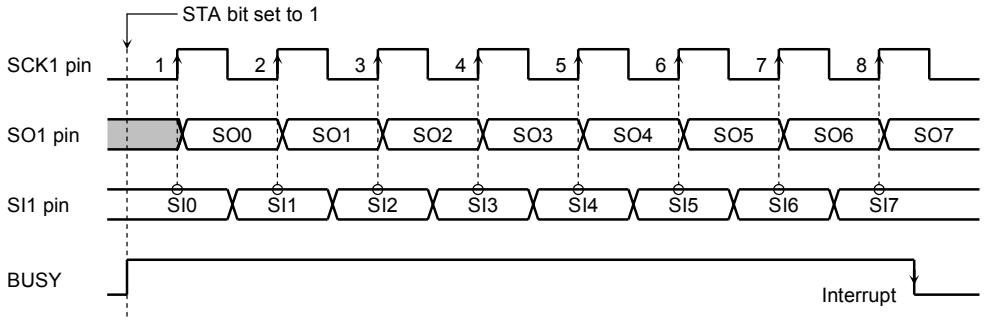
The EDGE bit sets the shift edge. The SCK-INV bit sets the shift clock input/output waveform. When the EDGE bit is set to 0, serial clock (SCK1) shift operations are performed on the rising edge of the clock. When the EDGE bit is set to 1, serial clock (SCK1) shift operations are performed on the falling edge of the clock. The SCK-INV bit sets whether to start shift operations from the serial clock's H level output or L level output. When SCK-INV is set to 0, shift operations start from the H output. When SCK-INV is set to 1, shift operations start from the L output. These bits can be used to allow the kind of serial operations shown in the following table. Set those serial operations in accordance with the controlling serial format.

The SCKO bit sets the serial clock input/output. When using the TC9325FG as the master controller, set SCKO to 1 to output the serial clock. When the TC9325FG is the slave, set SCKO to 0 to input the serial clock.

	SCKINV = 0	SCKINV = 1
edge = 0	 Note: The SCK bit must be set to 0. Note: The settings of this mode can be used for a two-line serial interface.	 Note: The ENA bit must be set to 0.
edge = 1	 Note: The ENA bit must be set to 0.	 Note: The SCK bit must be set to 1.

2) 8BIT Bit

The 8BIT bit selects the length of the serial data. Setting this bit to 0 selects 4-bit data; setting the bit to 1 selects 8-bit data. When the serial clock is set to the internal clock and SIO operations start, a 4-bit or 8-bit clock is continuously output depending on the setting of this bit.

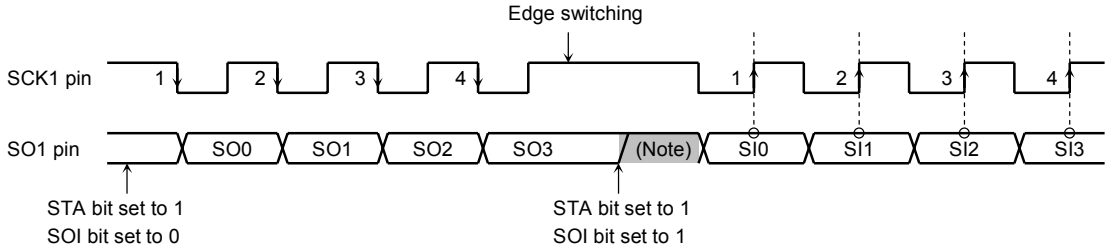


Example of Serial Operation When 8-Bit Data Set

3) SOI Bit

The SOI bit sets the SOI pin as either a serial data input or output.

Setting the SOI bit to 0 sets the SOI pin as a serial data output. Setting 1 sets the pin as a serial data input. This control can be used in serial bus operations where serial data input/output is controlled with a single pin.



Example of Serial Data Input/Output Operation

4) Monitoring Serial Interface 1 Operation

Use the BUSY, COUNT, and SIO F/F bits to check the operating state of the serial interface.

The BUSY bit is set to 1 during SIO operations. Therefore, set the control data and access the serial data when the BUSY bit is 0. Interrupt requests are generated on the falling edge of the BUSY bit.

Use the COUNT bit to determine whether a 4-bit unit of data has been sent or received. When the number of shift operations is a multiple of 4, the COUNT bit outputs 0. When not a multiple of 4, the bit outputs 1.

The SIO F/F bit is set to 1 when the SCK pin starts a shift operation.

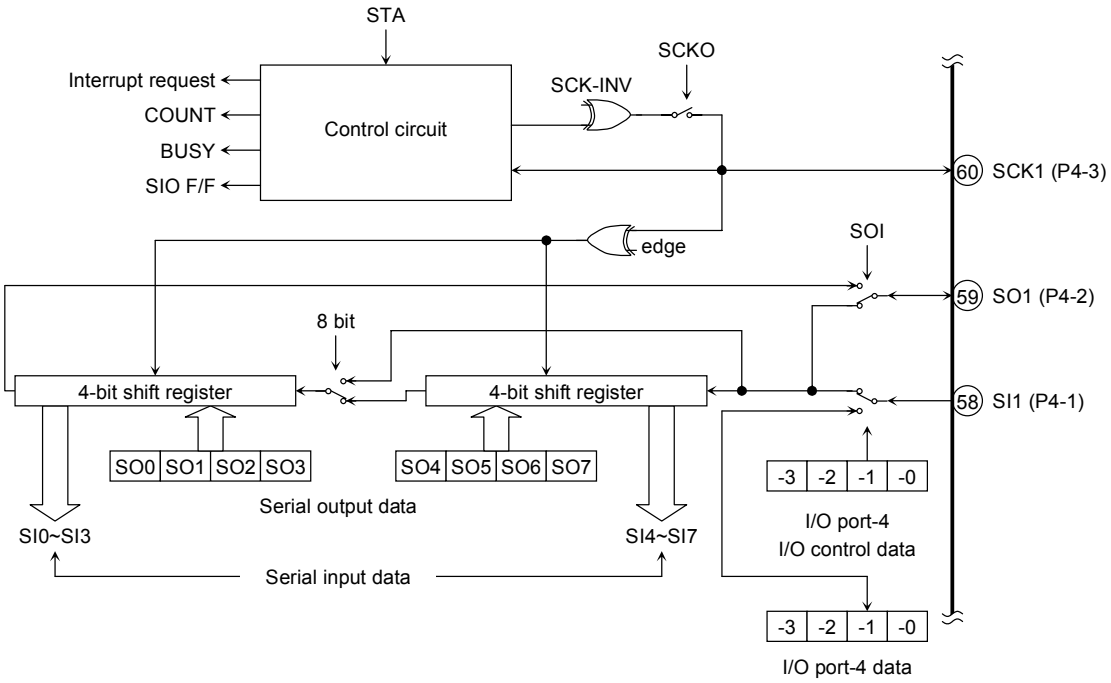
Setting the STA bit to 1 clears both the COUNT bit and SIO F/F bit to 0. These two bits are mainly used when the SCK pin is set as the external clock (slave). The bits can be used to check whether the external clock was input, whether serial data was sent or received, and whether operations were normal.

Because an interrupt normally occurs on completion of a serial interface operation, use interrupt handling for checking whether a serial operation was successful.

5) STA Bit

This bit is used to start serial interface operations. Each setting of the STA bit to 1 starts a serial operation. Setting STA to 1 transfers serial output data to the shift register and resets the COUNT bit and the SIO F/F bit. When the SCK clock is set to an internal clock, a serial clock is output. When the SCK clock is set to an external clock, the interface stands by for serial clock input.

2. Serial Interface 1 (SIO1) Structure



Serial interface 1 consists of a control circuit, a shift register, and I/O ports.

Note: The SI1 pin can be used as I/O port-4 (P4-1).

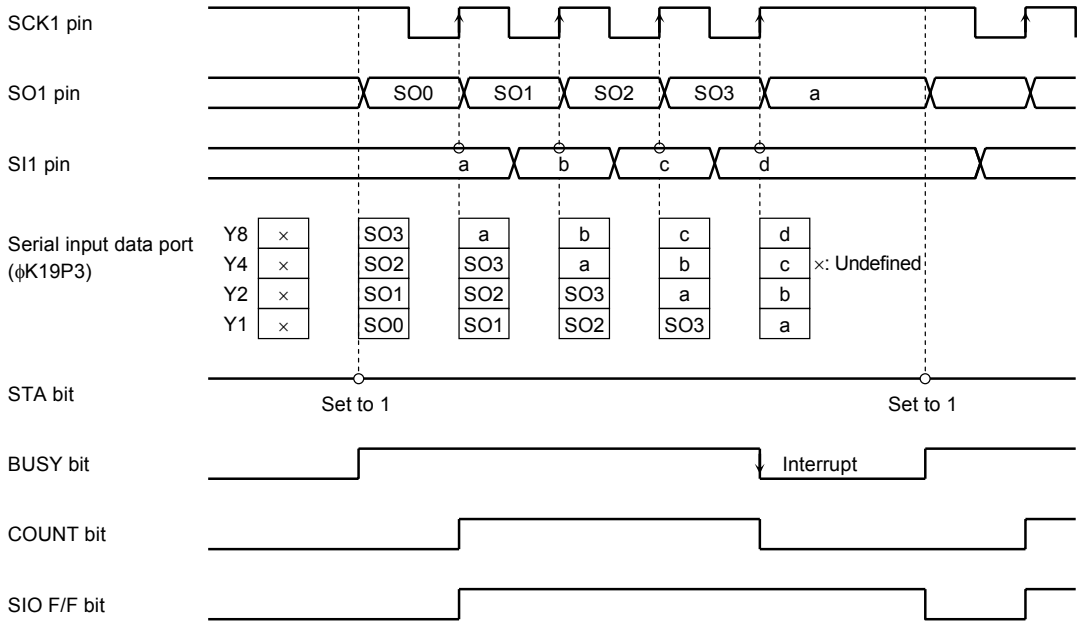
Note: The contents of the shift register are loaded to data memory as the data and serial input data. Accordingly, the data set as the serial output data differ from the serial input data.

Note: All the serial input pins (SI1, SO1/SO2, SCK1/SCK2) are Schmitt trigger inputs.

3. SIO1 Circuit Serial Interface Timing

When SCK1 is set to an internal clock, the frequency of the clock output from the SCK1 pin is 450 kHz (duty: 50%) with the 4.5-MHz peripheral clock selected, and 37.5 kHz (duty: 50%) with the 75-kHz peripheral clock selected.

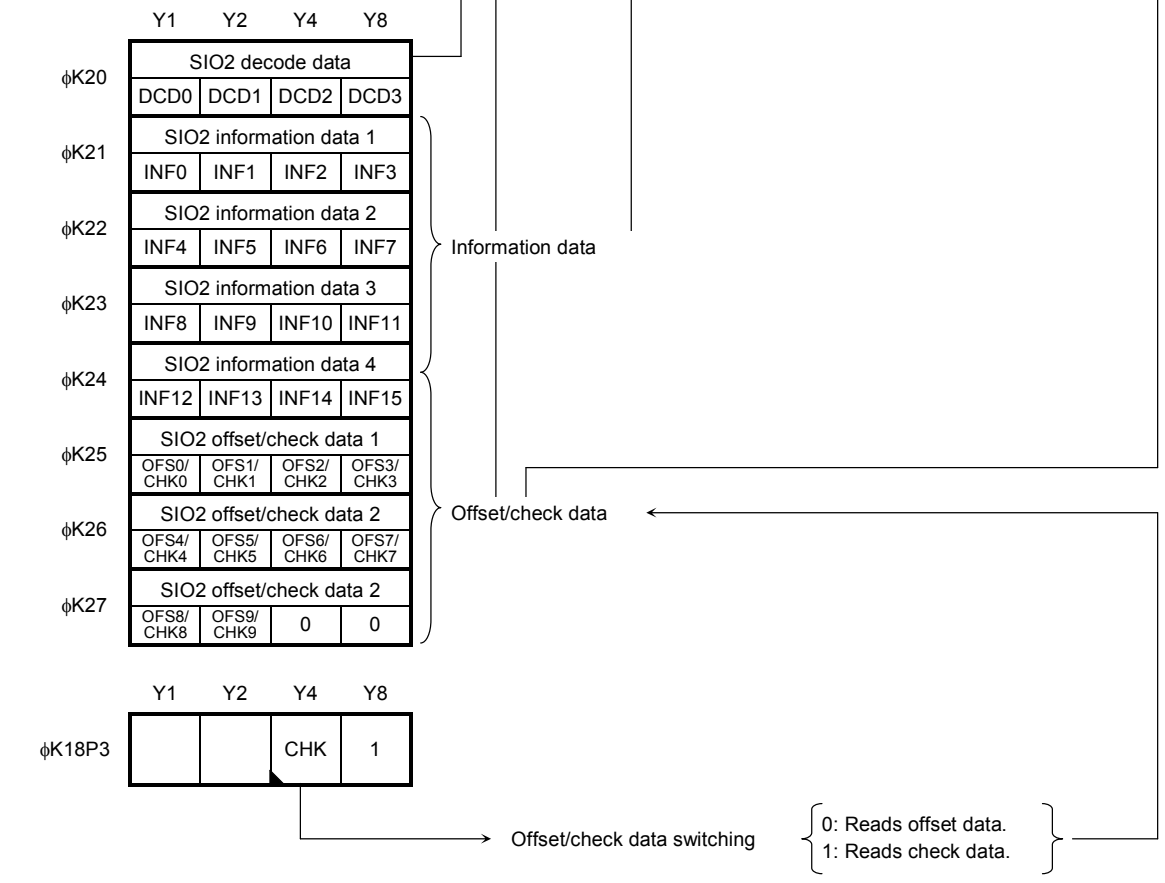
Note: When SCK1 is set to an external clock, input a clock with a frequency no higher than the above frequencies.



4. Serial Interface 2 (SIO2) Control Port, Data Port

Note: ∀ EXOR (exclusive OR)

Other data	0	0	0	1	0	0	0	OFS9 = (INF14 ∀ INF13 ∀ INF12 ∀ INF11 ∀ INF10 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF1)	∀CHK8
	1	0	1	1	1	1	0	OFS8 = (INF13 ∀ INF12 ∀ INF11 ∀ INF10 ∀ INF9 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF1 ∀ INF0)	∀CHK8
	1	0	1	0	0	1	1	OFS7 = (INF14 ∀ INF13 ∀ INF9 ∀ INF8 ∀ INF5 ∀ INF4 ∀ INF0)	∀CHK7
	0	0	0	1	1	0	1	OFS6 = (INF15 ∀ INF14 ∀ INF11 ∀ INF10 ∀ INF8 ∀ INF7 ∀ INF5 ∀ INF2∀INF1)	∀CHK6
	0	0	1	0	1	0	1	OFS5 = (INF15 ∀ INF14 ∀ INF13 ∀ INF10 ∀ INF9 ∀ INF7 ∀ INF6 ∀ INF4 ∀ INF1 ∀ INF0)	∀CHK5
	1	0	1	1	0	1	1	OFS4 = (INF15 ∀ INF11 ∀ INF10 ∀ INF9 ∀ INF8 ∀ INF6 ∀ INF4 ∀ INF2 ∀ INF1 ∀ INF0)	∀CHK4
	0	0	0	0	1	1	1	OFS3 = (INF13 ∀ INF12 ∀ INF11 ∀ INF9 ∀ INF8 ∀ INF7 ∀ INF4 ∀ INF2 ∀ INF0)	∀CHK3
	1	0	1	0	0	0	1	OFS2 = (INF15 ∀ INF14 ∀ INF13 ∀ INF8 ∀ INF7 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF2)	∀CHK2
	0	0	0	0	0	0	0	OFS1 = (INF15 ∀ INF14 ∀ INF13 ∀ INF12 ∀ INF7 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF1)	∀CHK1
	0	0	0	0	0	0	0	OFS0 = (INF15 ∀ INF14 ∀ INF13 ∀ INF12 ∀ INF11 ∀ INF6 ∀ INF5 ∀ INF4 ∀ INF3 ∀ INF2 ∀ INF0)	∀CHK0
—	194h	000h	1B4h	350h	168h	198h	0FCh		
0	6	5	4	B	3	2	1		

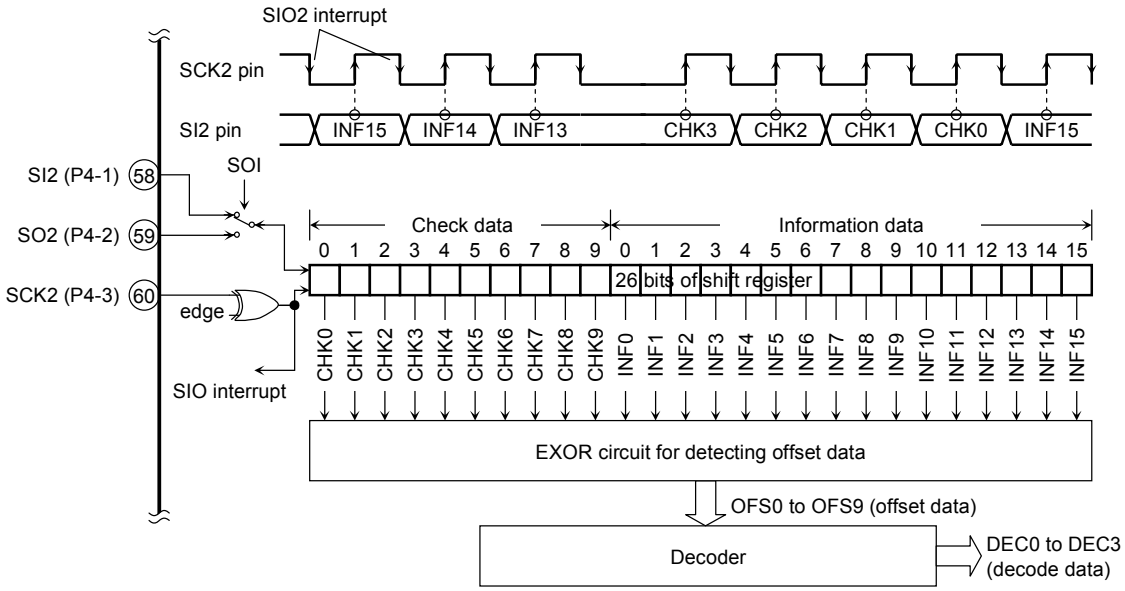


The serial interface 2 (SIO2) data port consists of 16-bit information data (ϕK21 to ϕK24), 10-bit check data (ϕK25 to ϕK27), 10-bit offset data (ϕK25 to ϕK27), and 4-bit decode data (ϕK20). Of the 26 bits of serial data, 16 bits are information data and 10 bits are check data. When some of the 26 bits of data are exclusive OR-ed, as shown in the previous table, they become offset data. When the offset data are special data (described previously), 1 to 6h and Bh are output as 4-bit decode data. The same port (ϕK25 to ϕK27) is used to read both check data and offset data. The SIO2 data selection bit (ϕL18P3) is used to select the data for reading. Setting the bit to 0 reads offset data; setting the bit to 1 reads check data.

To enable a SIO2 operation, set both the SIO_{on} bit (ϕL17P3) and the MOD bit (ϕL18P3) to 1. Setting the STA (ϕL18P3) to 1 resets all 26 bits of shift register. According to the SCK2 pin shift clock, the SI2 pin input states are successively input to the shift register. The shift clock edge can be switched by the EDGE bit (ϕL17P3). Setting EDGE to 0 shifts the data on the rising edge; setting EDGE to 1 shifts the data on the falling edge. Enabling the SIO2 interrupt at this time triggers the interrupt on the opposite edge to the shift edge. In addition, the SO-I/O bit can be used to switch serial input pins between SI2 and SO2. Setting the SO-I/O bit to 0 sets the SI2 pin to a serial data input. Setting the bit to 1 sets the SO2 pin to a serial data input. Note that when the SI2 pin is selected as a serial input, the SO2 pin becomes a SIO1 serial output pin. Accordingly, Toshiba recommend using the SO2 pin for serial input.

Access the serial interface 2 control data using the OUT1 instruction with the operand [CN = 7H, 8H] on I/O map page 3.

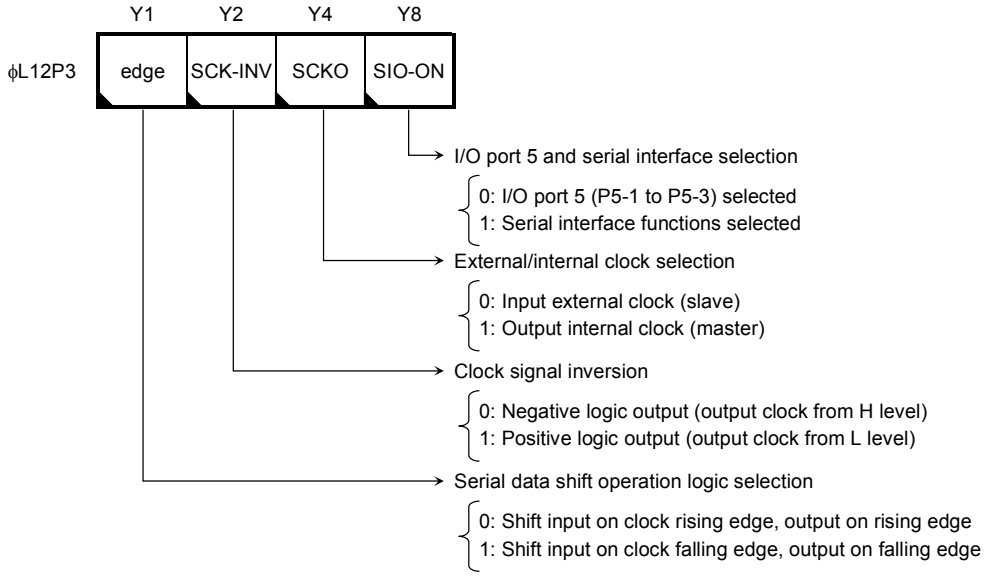
5. Serial Interface 2 (SIO2) Structure



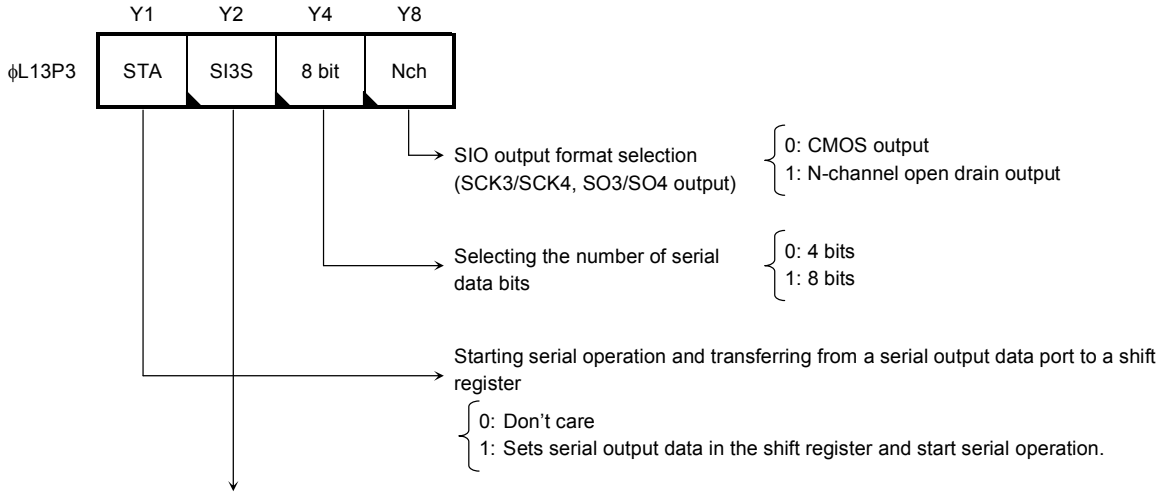
Note: When using the SI2 pin for serial input, the SO2 pin is used for the SIO1 serial output. When setting the SI2 pin to a serial input, set the P4-1 output data to 1 (input state).

Note: Serial input is simultaneously input and shifted to SIO1.

6. Serial Interface 3/4 Control Port, Data Port



Note: When the P5-2 pin is set as a serial data output (SO3/SO4 set), be sure to set the P5-2 I/O control bit (ϕL24) to 1 (output state). Setting the P5-2 I/O control bit to 0 sets pin P5-2 to input state. When using pin P5-1 as a serial input (SI3), be sure to set the P5-1 I/O control bit (ϕL24) to 0 (input). Setting the P5-1 I/O control bit to 1 sets pin P5-1 as an output and outputs the P5-1 output data (ϕL34) as-are.

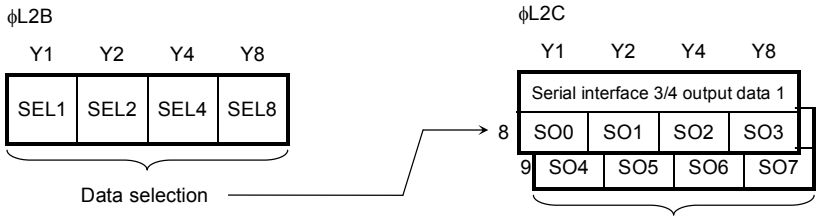


Note: The bit is updated under the following conditions.

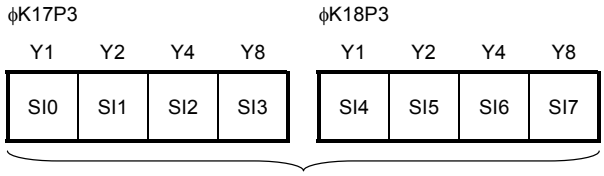
MOD	SIS	SO3/SO4 Pin	SI3/SI4 Pin
0	0	Serial output	Serial input
	1	Serial input	P5-1 input/output
1	0	Serial output	P5-1 input/output
	1	Serial input	

edge	SCKINV	SI3S Updating
0	1	After STA = 1 set, updates on serial clock falling edge.
1	0	After STA = 1 set, updates on serial clock rising edge.
0	0	Updates when STA = 1 set.
1	1	

Note: The output data (pin states) are input to the serial interface.

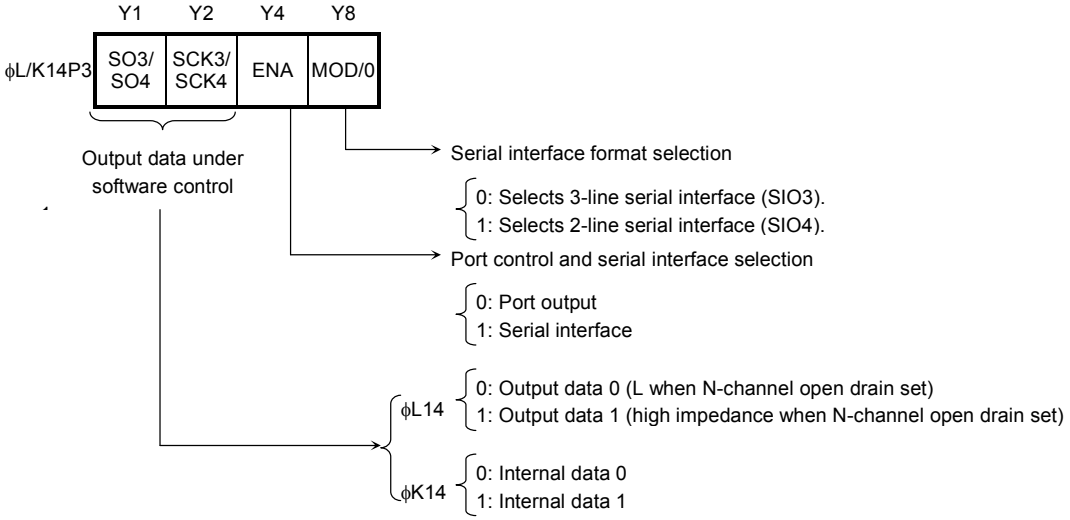


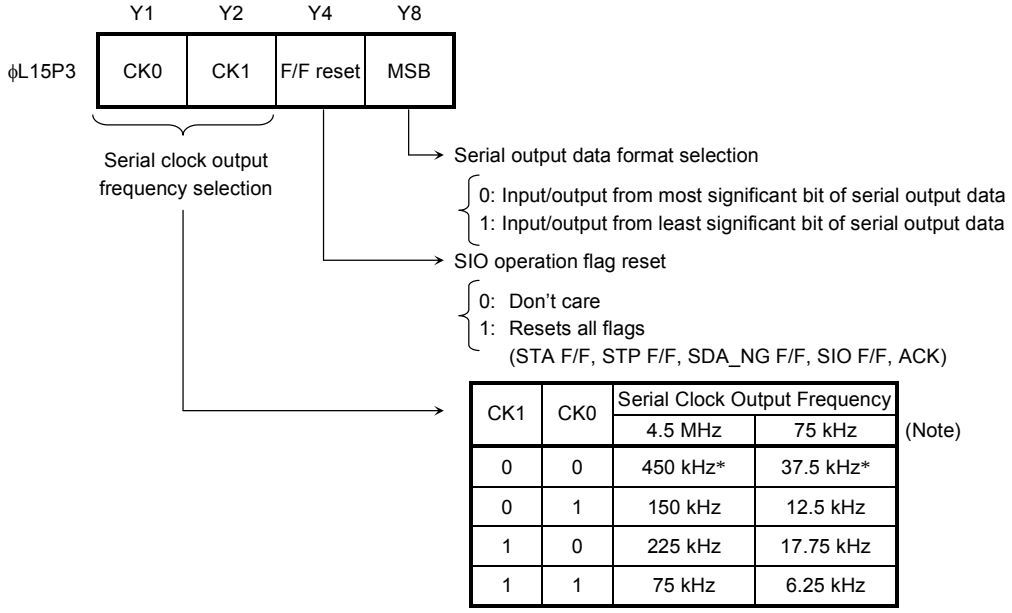
Serial output data: The data set in this port are output to the serial interface.



Note: The serial interface input data are accessed directly from the shift register.

Serial input data: The data input to the serial interface are loaded to data memory.

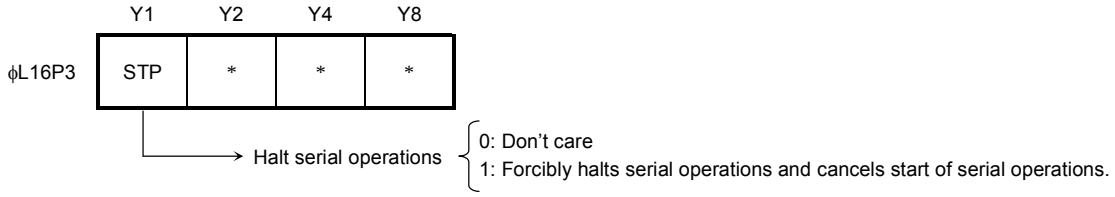


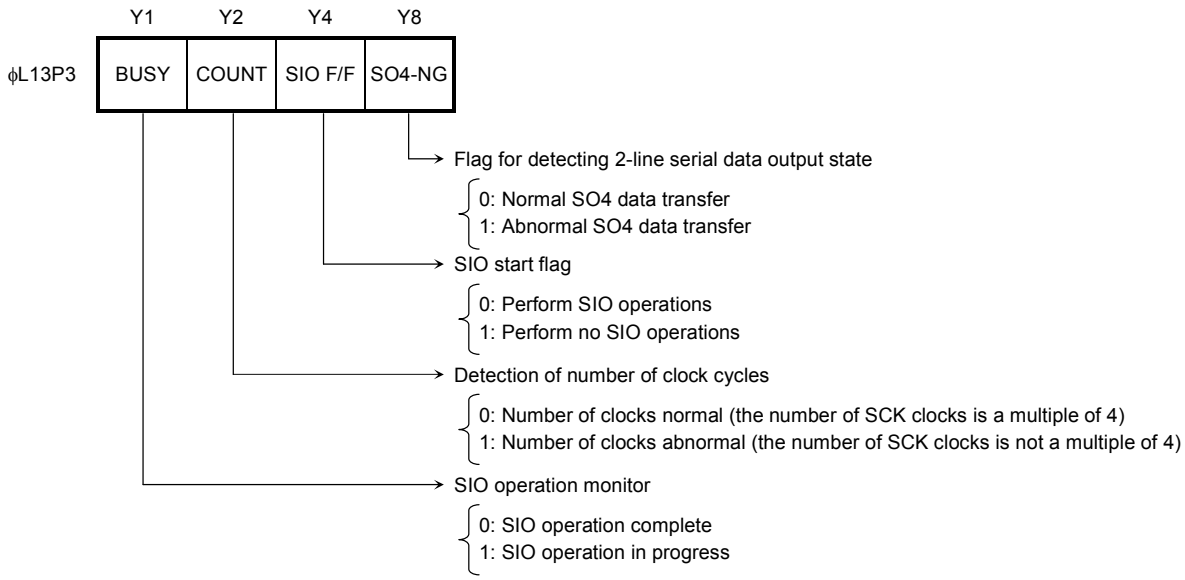


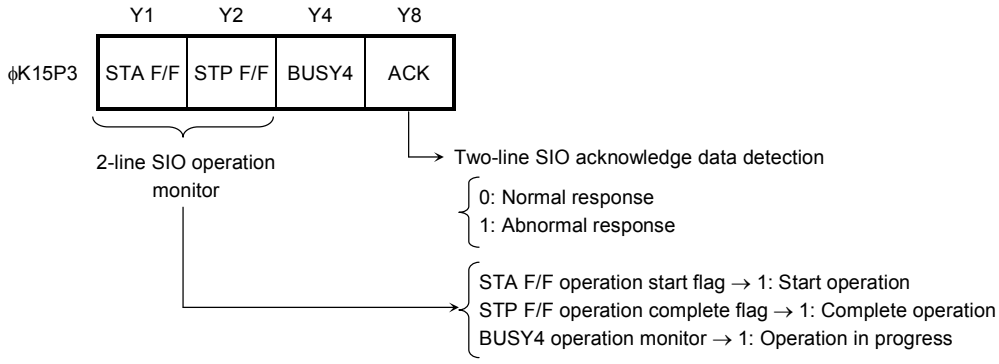
CK1	CK0	Serial Clock Output Frequency		
		4.5 MHz	75 kHz	(Note)
0	0	450 kHz*	37.5 kHz*	
0	1	150 kHz	12.5 kHz	
1	0	225 kHz	17.75 kHz	
1	1	75 kHz	6.25 kHz	

Note: The output frequency varies depending on the CPU operation clock used.

Note: When TC9325FG is set as a slave, CK0 and CK1 are don't care. When set as a slave, input a shift clock no higher than the frequency indicated by the asterisk (*).







Access serial interface control and serial data using the OUT1 instruction with the operand [CN = 2H to 6H] and the IN1 instruction with the operand [CN = 3H to 5H] on I/O map page 3.

The serial interface pins also function as the I/O port 5 P5-1, P5-2, and P5-3 pins. Setting the SIO ON bit to 1 switches the I/O port 5 pins to SI, SO, and SCK pins, respectively.

Note: The serial interface inputs all incorporate Schmitt trigger circuits.

Note: Even when the serial interface is selected, the SI pin (P5-1) can still be used as an I/O port. Therefore, the pin can be used for SIO strobe signals.
When setting this pin as a serial input, set the P5-1 I/O control bit to input.

1) SIO ON Bit

The SIO ON bit switches the P5-2/SO3/SO4 and P5-3/SCK3/SCK4 pins to serial interface function pins SO3/SO4 and SCK3/SCK4.

Setting SIO ON to 1 sets the pins to serial interface function pins; setting the bit to 0 sets the pins as I/O port 5. When serial interface functions are set, these pins can all be controlled by the serial interface control bits. Note, however, that the I/O port input data can still be read.

Setting pin P5-1/SI3 to serial interface functions allows the pin to be used as a serial input. The I/O port function can be used even when the pin is set to serial interface functions. Input/output can be set using the I/O control port and data can be input/output using the I/O data port. Therefore, when this pin is set to serial input, it must also be set as an I/O port input.

2) MOD Bit

The MOD bit selects the serial interface format. Setting MOD to 0 selects 3-line serial interface; setting MOD to 1 selects 2-line serial interface.

When two-line serial interface is selected, the EDGE and SCK-INV bits (described below) are set to 0 and the Nch bit to 1.

When three-line serial interface is selected, the ACK, BUSY4, STA F/F, and STP F/F bits are invalidated.

3) EDGE, SCK-INV, and ENA Bits

The EDGE bit sets the serial clock (SCK3/SCK4) edge. Setting EDGE to 0 inputs serial data on the clock rising edge and outputs serial data on the falling edge. Setting EDGE to 1 inputs serial data on the clock falling edge, and outputs serial data on the rising edge.

The SCK-INV bit sets the shift clock's (SCK3/SCK4) input/output waveform. The bit setting determines whether to start the waveform from the serial clock's H level output or from L level output. When SCK-INV is set to 0 the shift clock waveform starts from L level output, and when the bit is set to 1 the shift clock waveform starts from H output.

The ENA bit switches between serial operations and software control. Setting ENA to 0 selects serial operations. Setting the bit to 1 selects software control. When ENA is set to serial operations, the serial clock (SCK3/SCK4 pin) and serial data (SO3/SO4 pin) are input/output. When ENA is set to software control (ENA = 1), the serial clock is output to the SCK3/SCK4 pin and serial data to the SO3/SO4 pin.

When 3-line serial interface is selected with the EDGE and SCK-INV bits both set to 0 or to 1, setting the STA bit to 1 automatically resets ENA to 0, then sets it back to 1 on completion of serial operations. When the EDGE and SCK-INV bits are set to (1, 0) or (0, 1), neither set nor reset occurs. Therefore, with these settings, normally the ENA bit is set to 0.

When 2-line serial interface is selected, the ENA bit is set to 1 (forcibly terminate serial operations) under the following conditions.

- On a shift clock (SCK4) rising edge after the SDANG_F/F bit is detected as 1 (data output result flag NG)
- On a shift clock (SCK4) rising edge after the STP F/F bit is detected as 1 (2-line serial interface terminated)
- On a shift clock (SCK4) rising edge after the ACK bit is detected as 1 (acknowledge detection NG)
- On a shift clock (SCK4) falling edge at completion of a shift operation

Also, when 2-line serial interface is selected, the ENA bit is reset to 0 (serial operations start) under the following conditions.

- On a shift clock (SCK4) rising edge after the STA bit is detected as 1 (serial operations start)
- On a shift clock (SCK4) rising edge after the STA F/F bit is detected as 1 (2-line serial interface terminated)

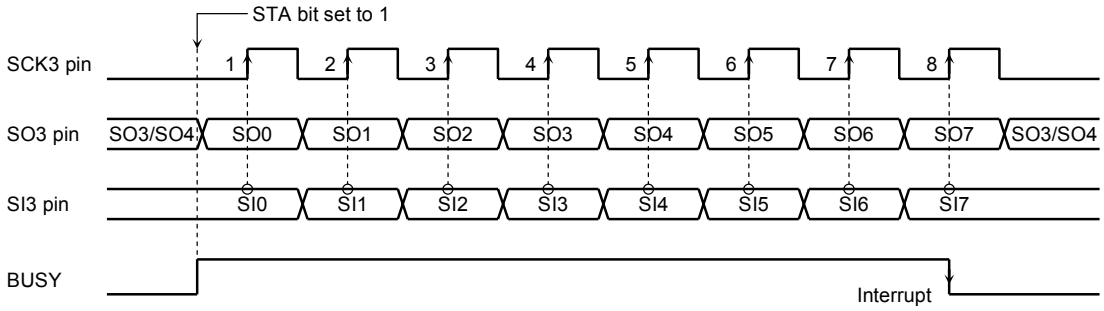
4) MSB Bit, 8BIT Bit, Serial Data Port

The MSB bit controls the sequence of the serial input/output data. Setting MSB to 0 outputs the serial data from the least significant bit (LSB: SO0 to SO7) and inputs serial data from the least significant bit (LSB: SI0 to SI7).

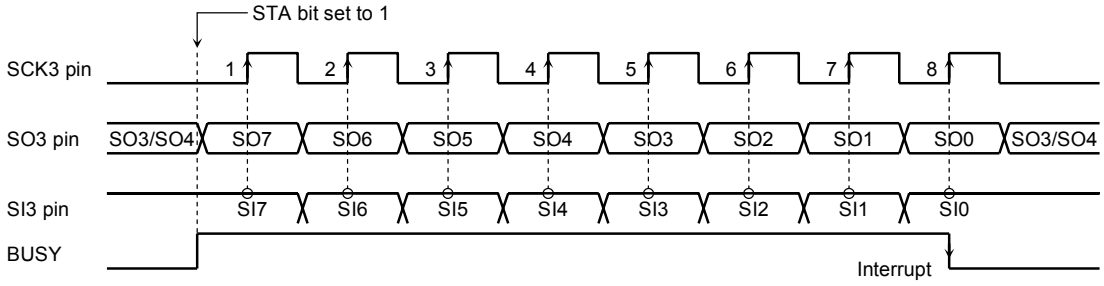
Setting MSB to 1 outputs the serial data from the most significant bit (MSB: SO7 to SO0) and inputs serial data from the most significant bit (MSB: SI7 to SI0).

The 8BIT bit selects the length of the serial data. Setting this bit to 0 selects 4-bit data; setting the bit to 1 selects 8-bit data. When 4-bit data is selected, the lower four bits (SO0 to SO3, SI0 to SI3) of the serial data are used.

The serial output data of the serial data port (SO0 to SO7) are transferred to the shift register at the start of serial operations, then output to the serial interface. Serial input data (SI0 to SI7) are loaded from the shift register.



Serial Operation When 8-Bit Data (8BIT = 1), LSB Output (MSB = 0) Set



Serial Operation When 8-Bit Data (8BIT = 1), MSB Output (MSB = 1) Set

5) SCKO Bit

The SCKO bit sets the serial clock (SCK3/SCK4) input/output. When using the TC9325FG as the master controller, set SCKO to 1 to output the serial clock. When TC9325FG is the slave, set SCKO to 0 to input the serial clock.

6) CK0, CK1 Bits

The CK0, CK1 bits select the serial clock frequency when TC9325FG is selected as the master. Because the frequency varies according to the CPU clock used, select the frequency in accordance with your specifications. The clock duty is 50%.

CK1	CK0	Serial clock output frequency	
		4.5 MHz	75 kHz
0	0	450 kHz*	37.5 kHz*
0	1	150 kHz	12.5 kHz
1	0	225 kHz	17.75 kHz
1	1	75 kHz	6.25 kHz

(Note)

Note: The output frequency varies in accordance with the operating clock of the CPU used.

When TC9325FG is set as a slave, CK0 and CK1 are don't care. When set as a slave, input a shift clock no higher than the frequency indicated by the asterisk (*).

7) SCK3/SCK4, SO3/SO4 Bits

When the ENA bit is set to 1 with the SCK3/SCK4, SO3/SO4 pins set as outputs (by the port 5 I/O control and SCKO/SI1S bits), the SCK3/SCK4 and SO3/SO4 bit data are output as-are.

When two-line serial interface is selected, the SCK3/SCK4 and SO3/SO4 bits are set to 1 under the following conditions.

- On a shift clock (SCK4) rising edge after the SDANG_F/F bit is detected as 1 (data output result flag NG)
- On a shift clock (SCK4) rising edge after the STP F/F bit is detected as 1 (two-line serial interface terminated)

Also, when two-line serial interface is selected, the SCK3/SCK4 bit is reset to 0 under the following condition. (The SO3/SO4 bits are not reset by a serial operation.)

- On a shift clock (SCK4) falling edge at completion of a shift operation

8) SI3S Bit

The SI3S bit switches the serial interface data input/output. Setting SI3S to 1 selects the P5-2/SO3 pin as a serial output and the P5-1/SI3 pin as a serial input. When using the P5-1/SI3 pin as a serial input, the P5-1 I/O control port must be set to input. Setting SI3S to 0 selects the P5-2/SO3 pin as a serial input and the P5-1/SI3 pin as an I/O port input/output (P5-1).

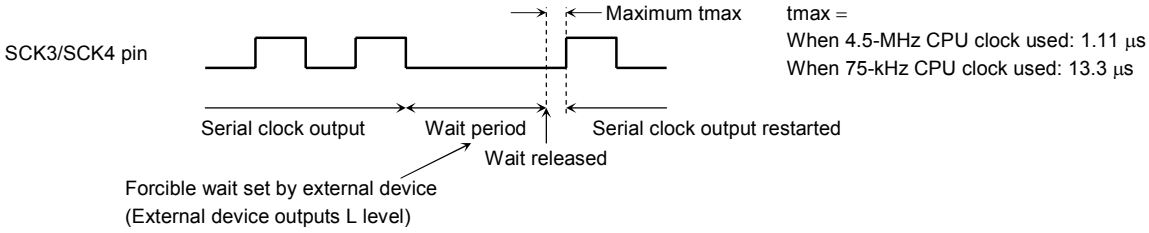
The SI3S bit is used to switch the SO3 pin input/output; the input/output switching is updated under the following conditions.

Edge	SCKINV	SI3S Bit Updating
0	1	After STA = 1 set, updates on serial clock (SCK3/SCK4) falling edge.
1	0	After STA = 1 set, updates on serial clock (SCK3/SCK4) rising edge.
0	0	Updates when STA = 1.
1	1	

9) Nch Bit

The Nch bit selects CMOS output or N-channel open drain output when the SO3/SO4 and SCK3/SCK4 pins are set to output. Setting the Nch bit to 0 sets CMOS output; setting Nch to 1 sets N-channel open drain output. When N-channel open drain is set, the serial clock operation wait function and the serial data output monitor function operate (see the section on the SO-NG F/F).

The serial clock wait function pauses the serial clock output when TC9325FG is set as a master (serial clock output set) and the serial output clock is set to forcible wait by an external device (which sets the serial clock to L).



10) BUSY Bit

The BUSY bit is used to reference the serial operation state.

When a serial operation starts (when the STA bit is set to 1 or the serial operation start conditions are satisfied), BUSY is set to 1. Before attempting to reference serial data, first check that this bit is set to 0. The falling edge of the BUSY bit generates interrupt requests (on completion of a serial operation).

11) COUNT Bit

The COUNT bit is used to determine whether data have been sent or received in 4-bit units. When the number of shift operations is a multiple of 4, the COUNT bit outputs 0. When not a multiple of 4, the bit outputs 1. COUNT is reset to 0 whenever the F/F reset bit is set to 1.

12) SIO F/F Bit

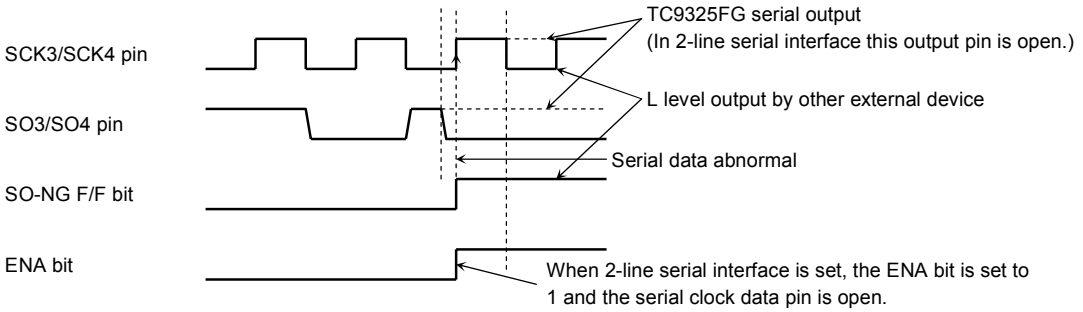
The SIO F/F bit is set to 1 when the SCK3/SCK4 pin starts a clock operation. When TC9325FG is set as a master (serial clock set to external input), this bit can be used to check whether a serial operation has started or is suspended. The SIO F/F bit is reset to 0 whenever the F/F reset bit is set to 1.

13) SO-NG F/F Bit

When serial data are output, this bit can be used to check whether the correct data have been output. When the Nch bit is set to 1 (N-channel open drain output), the SO-NG F/F bit is valid. When the SO-NG F/F bit is set to 0, the data output is normal; when the bit is set to 1, the data output is abnormal. When the data output is confirmed as abnormal with 2-line serial interface set, the ENA, SO3/SO4, and SCK3/SCK4 bits are all set to 1, the serial clock and serial data pins are open, and high impedance is set. This overrides the master restrictions when multiple masters are set and simultaneously outputting data. After this, serial operations continue until the completion of 8-bit data serial operations. Then, after checking that the serial operations have completed (BUSY3), the serial data can be referenced.

Even though the data output is judged abnormal with 3-line serial interface set, no setting of the ENA, SO3/SO4, and SCK3/SCK4 bits takes place and their status is unchanged. In this case, the SO-NG F/F bit is used to determine whether the data output is normal or abnormal.

The SO-GN F/F bit is reset to 0 whenever the F/F reset bit is set to 1.



14) STA Bit

This bit is used to start serial interface operations.

When 3-line serial interface is set, each setting of the STA bit to 1 starts a serial operation. Setting STA to 1 transfers serial output data to the shift register. When the serial clock is set to an internal clock (master), a serial clock is output. When the serial clock is set to an external clock (slave), the interface stands by for serial clock input.

When 2-line serial interface is set, inputting the start conditions to the SCK4 and SO4 pins automatically starts serial operations. When TC9325FG is set as the master, a serial clock (SCK4) is output for serial operations. When TC9325FG is a slave, an external serial clock is used for serial operations. When receiving or sending data equal to or larger than two bytes, setting STA to 1 on completion of serial operations on the first byte transfers the serial output data to the shift register and starts serial operations on the falling edge of the next serial clock.

15) ACK Bit

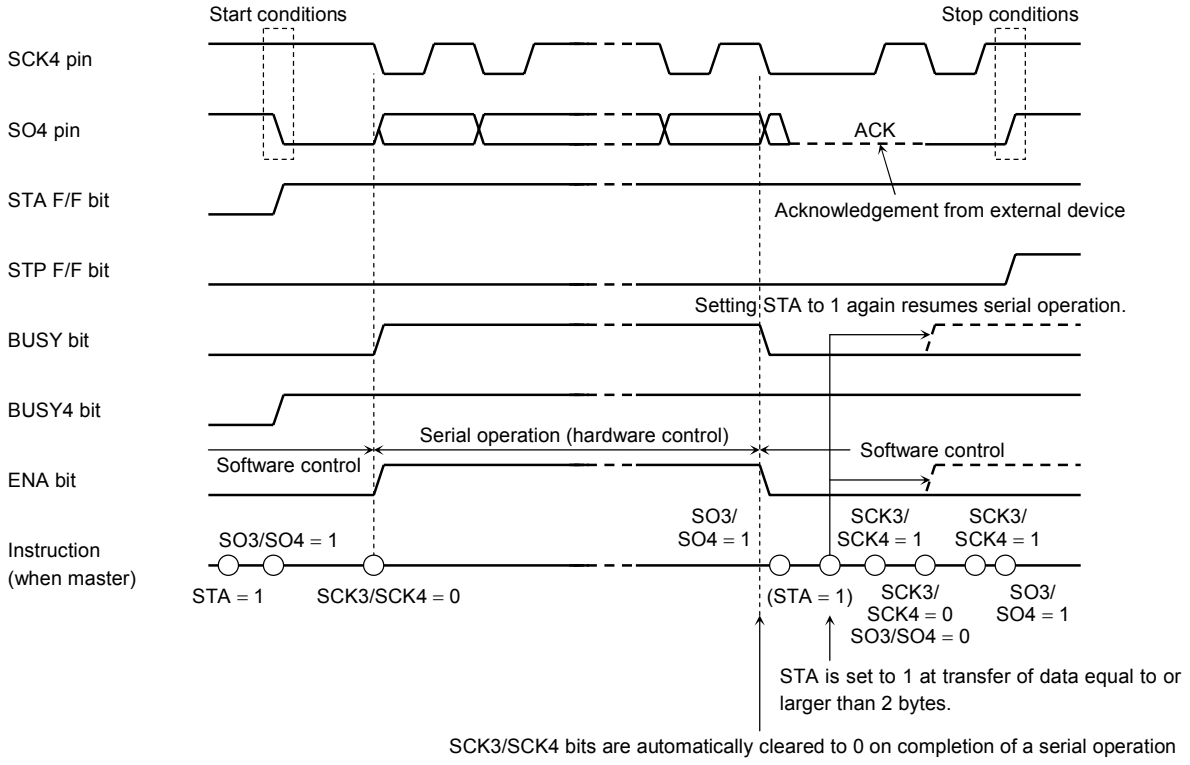
The ACK bit is the acknowledge bit. This bit is valid when 2-line serial interface is set. After inputting/outputting 8-bit serial data, the status of the SO4 pin is input to the ACK bit on the next rising edge. When 0 is input to ACK with STA already set to 1, the next serial operation begins. When 1 is input to ACK, any serial operations for which the STA bit is already set to 1 are cancelled.

ACK is reset to 0 whenever the F/F reset bit is set to 1.

16) STA F/F, STP F/F, BUSY4 Bits

These bits are used to detect the 2-line serial interface start and stop conditions and are valid when 2-line serial interface is set. When the 2-line serial interface start conditions are detected, the STA F/F and BUSY4 bits are set to 1. When the 2-line serial interface stop conditions are detected, the STP F/F bit is set to 1 and the BUSY4 bit is reset to 0. The STA F/F and STP F/F bits are reset to 0 whenever the F/F reset bit is set to 1.

The 2-line serial interface operation status can be detected by checking these bits.



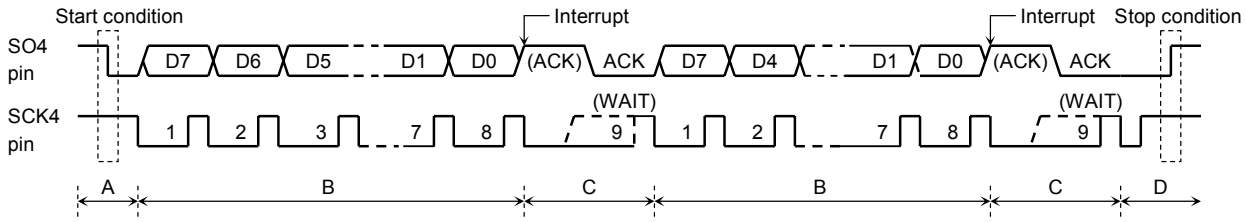
Example of Two-Line Serial Interface Operation

17) STP Bit

The STP bit is used to forcibly terminate serial operations still in progress and to cancel the start of a serial operation. At this time the bit is set to 1.

With 2-line serial interface set, when STP is set to 1 to terminate a serial operation in progress, the serial operation terminates at the time the setting is executed.

With 3-line serial interface set, when STP is set to 1 to terminate a serial operation in progress, the serial operation is terminated on the falling edge of the serial clock. Also, STP can be used to cancel the commencement of a serial operation where STA is already set to 1.

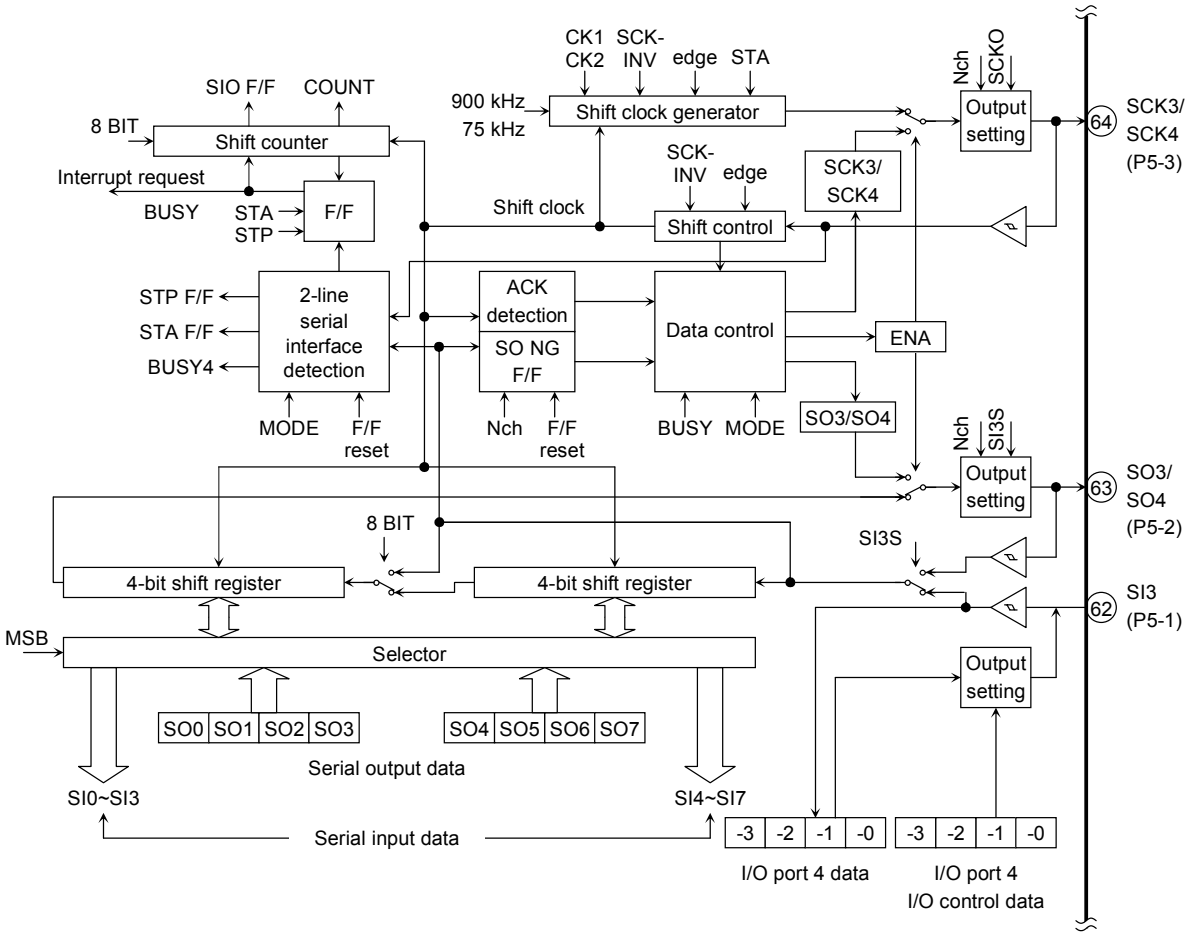


2-Line Serial Interface Timing Example

Setting mode conditions	First set up the following operating conditions • SIO_{on} = 1: Enables serial interface. • EDGE = 0: Sets rising edge shift. • 8BIT = 1: Sets 8-bit operations. • MSB = 1: Sets input/output data from MSB • MOD = 1: Sets 2-line serial interface operations. • SCKO = 1: Sets serial clock output (master mode). • SCK-INV = 0: Sets positive logic output. • Nch = 1: Sets N-channel open drain output. • CK0/1: Sets by operating frequency. When outputting serial data, first set data to the serial output data port (ϕL2CA, ϕL2CB). If TC9325FG is the master, set SCKO = 1; if the slave, set SCKO = 0; if data output, set SO1 = 0; if data input, set SOI = 1.
Start conditions (Timing A)	If TC9325FG is the master, control the start conditions output by software. If the slave, set to wait after setting the start conditions. For software control when TC9325FG is the master, set the SO3/SO4 and SCK3/SCK4 bits to 1 to set software control (ENA = 1) (ϕL14P3 ← FH). Set bits SO3/SO4 to 0 (ϕL14P3 ← EH), then set the SCK3/SCK4 bits to 0 (ϕL14P3 ← CH) to output the start condition waveform. At that time, the serial operation automatically starts on the rising edge of the SCK4 pin, as when STA = 1 is set (no need to set STA = 1). If the serial data input/output (SOI) setting has been changed, the serial data input/output (SOI) is updated on the serial clock's falling edge. If TC9325FG is set as a slave, shift operations start automatically at the start conditions.
Serial operations (Timing B)	When serial operations start, the flags are set as follows: BUSY = 1: Serial operation in progress. BUSY4 = 1: Set to 1 at start condition. 2-line serial operation in progress. STA F/F = 1: Set to 1 at start condition. Detects 2-line serial operation start signal. SIO F/F = 1: Set to 1 on SCK4 pin rising edge (1). Detects serial operation clock. ENA = 0: Serial operation input/output state. In serial operations, the SO4 pin state is input to the serial interface on a rising edge; serial data are output on a falling edge. On the falling edges of the eight serial clocks, the following states are set automatically: BUSY = 0: Serial operations complete BUSY4 = 1: Two-line serial operation in progress. STA F/F: Flag held SIO F/F: Flag held ENA = 1: Under software control (SO3/SO4, SCK3/SCK4 bits output) SCK3/SCK4 = 0: SCK4 pin set to L and clock wait state set In addition, a serial interface interrupt is generated if the interrupt is enabled. When the TC9325FG is the master, even though an H level (pulled-up state) is output to the SCK4 pin during a serial operation, if the pin state is L (waiting for the clock from another device), the serial clock is halted until the clock of the other device is released. Even though an H level is output from the SDA pin during serial data output, if the pin state is L (simultaneous output detected on a multi-master system), the SO3/SO4, SCK3/SCK4, and ENA bits are automatically set to 1 and software control is set on the SCL clock rising edge, then the output is released (Hz). At that time, the SO-NG F/F bit is set to 1. To output an H level from the SO3/SO4 pin after the serial operation completes (set to 0 on the start condition), set the SO3/SO4 bit to 1 (ϕL14P3 ← 9H or 6H) during a serial operation. Where the stop conditions are satisfied during a serial operation, an interrupt is generated if enabled.

Acknowledge detection (Timing C)	Software is used to control the acknowledge detection and output. On completion of a serial operation, ENA = 1, SCK3/SCK4 = 0, the SCK4 pin is automatically set to L, and clock output from other devices is prohibited. This state allows the necessary processing, such as reading serial input data and setting the next data. When that processing is complete, set the necessary conditions, then set the STA bit to 1. Next, if the TC9325FG is the master, generate an acknowledge clock by software control. Use software control to set the following: Acknowledge output: SO3/SO4 = 0, SCK3/SCK4 = 0 (ϕL14P3 ← CH) → SCK3/SCK4 = 1 (ϕL14P3 ← EH) → SCK3/SCK4 = 0 (ϕL14P3 ← CH) Acknowledge input: SO3/SO4 = 1, SCK3/SCK4 = 0 (ϕL14P3 ← DH) → SCK3/SCK4 = 1 (ϕL14P3 ← FH) → SCK3/SCK4 = 0 (ϕL14P3 ← DH) These states are read to the ACK bit on the rising edge of the SCL pin clock. If the TC9325FG is the slave, set the following for during a clock wait state set by completion of a serial operation: Acknowledge output: SO3/SO4 = 0, SCK3/SCK4 = 1 (ϕL14P3 ← EH) Acknowledge input: SO3/SO4 = 1, SCK3/SCK4 = 1 (ϕL14P3 ← FH) These states are read to the ACK bit on the rising edge of the SCL pin clock. On the falling edge of the acknowledge clock, the serial operation start (STA = 1) set prior to the reading of the acknowledge is validated and the serial operation commences.
Stop condition (Timing D)	If the TC9325FG is the master, set the output of the stop conditions by software control. If the slave, set the stop conditions, then set to wait state. Set the following software control when the TC9325FG is the master: SO3/SO4, SCK3/SCK4 bits = 0 (ϕL14P3 ← CH), SCK3/SCK4 bits = 1 (ϕL14P3 ← EH), then set the SO3/SO4 bits to 1 (ϕL14P3 ← FH). If TC9325FG is the slave, the following flags detect the stop condition and terminate the operation. When the stop condition is detected, the flags are: STP F/F = 1: Set to 1 by stop condition. Detects completion of 2-line serial operations. BUSY4 = 0: Reset to 0 by stop condition. 2-line serial operation complete. If completion is detected, the start of serial operations must be forcibly prevented. To do this, set the STP bit to 1 beforehand to terminate the operation.

7. Serial Interface Structure



The serial interface consists of a control circuit, shift registers, and I/O ports.

Note: The SI pin can also be used as I/O port 5 (P5-1).

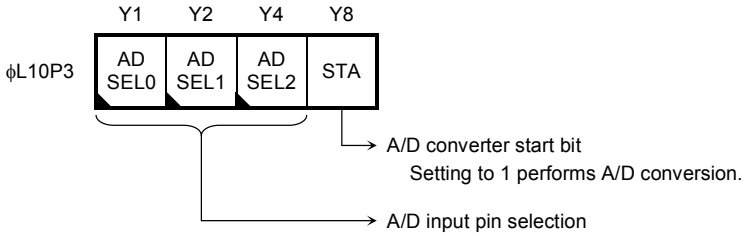
Note: The contents of the shift registers are loaded to data memory as the data and serial input data. Therefore, the data set as serial output data and the serial input data do not match.

Note: The serial input pins all incorporate Schmitt trigger circuits.

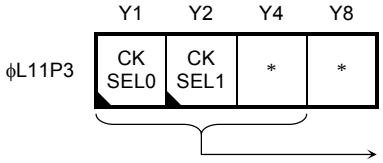
○ A/D Converter

The 8-channel, 8-bit resolution A/D converter is used for many purposes such as measuring voltages.

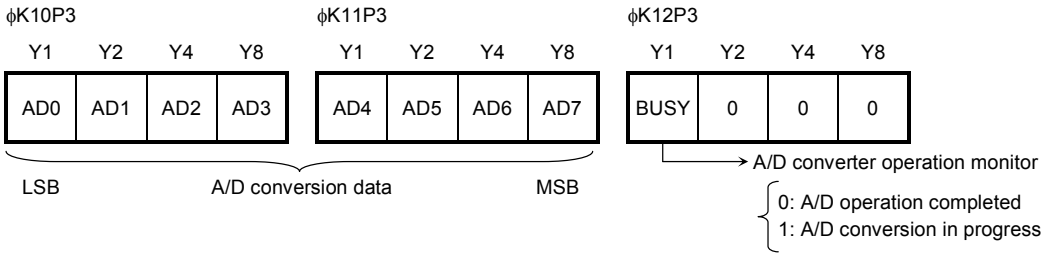
1. A/D Converter Control Port, Data Port



SEL0	SEL1	SEL2	A/D Input
0	0	0	ADIN1
1	0	0	ADIN2
0	1	0	ADIN3
1	1	0	ADIN4
0	0	1	ADIN5
1	0	1	ADIN6
0	1	1	ADIN7
1	1	1	ADIN8



SEL0	SEL1	4.5 MHz Selected	75 kHz Selected
0	0	900 kHz	75 kHz
1	0	100 kHz	Prohibited
0	1	50 kHz	Prohibited
1	1	900 kHz	75 kHz



The A/D converter uses 8-bit resolution, successive comparison conversion. The internal power supply (V_{DD}) is used as the AD conversion reference voltage. The A/D converter compares the voltage resulting from dividing the power supply by 256 with the A/D input voltage and outputs the comparison data to the A/D conversion data port. The A/D conversion input is multiplexed to eight channels of external input pins (pins ADIN1 to ADIN8) and selected by the AD SEL0 to SEL2 bits.

The A/D converter performs A/D conversion whenever the STA bit is set to 1. When the CPU clock is set to 4.5 MHz, the CK SEL1/2 bits can select the conversion clock from among 900-kHz, 100 kHz, and 50 kHz. When the CPU clock is set to 75 kHz, the conversion clock is selected as 75 kHz. The corresponding conversion times are: 23, 192, and 382 μs, and 294 μs. The BUSY bit can be referenced to check whether A/D conversion is complete. After A/D conversion is complete, the controller loads the A/D conversion data to data memory.

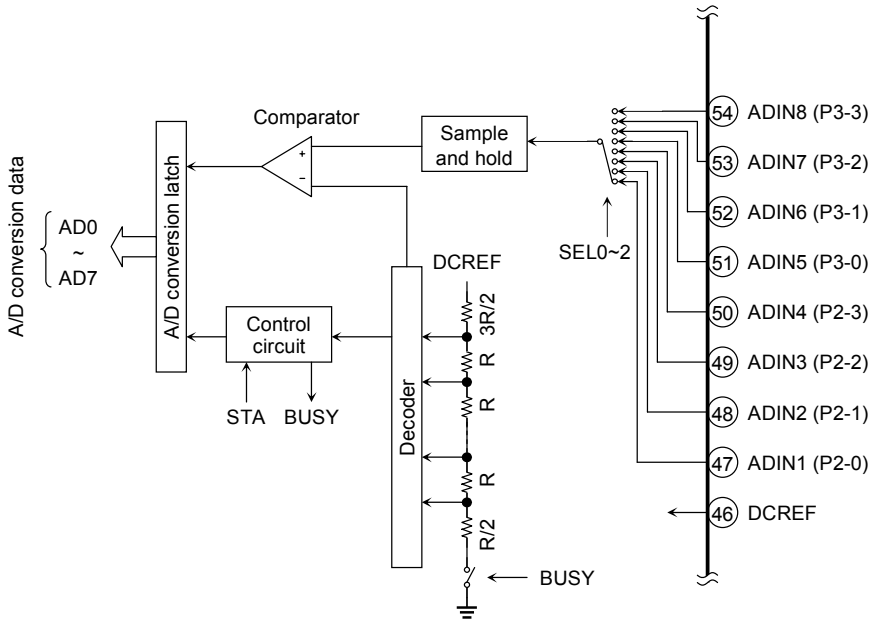
Use the following formula to calculate the A/D comparison result.

$$V_{DD} \times \frac{n-0.5}{256} (255 \geqq n \geqq 1) \leqq \text{A/D input voltage} \leqq V_{DD} \times \frac{n+0.5}{256} (254 \geqq n \geqq 0)$$

(where n is the [decimal] A/D conversion data value)

These control bits can be accessed by the OUT2 instruction with the operand [CN = 0H, 1H] and the IN2 instruction with the operand [CN = 0H to 2H] on I/O map page 3.

2. A/D Converter Circuit Structure



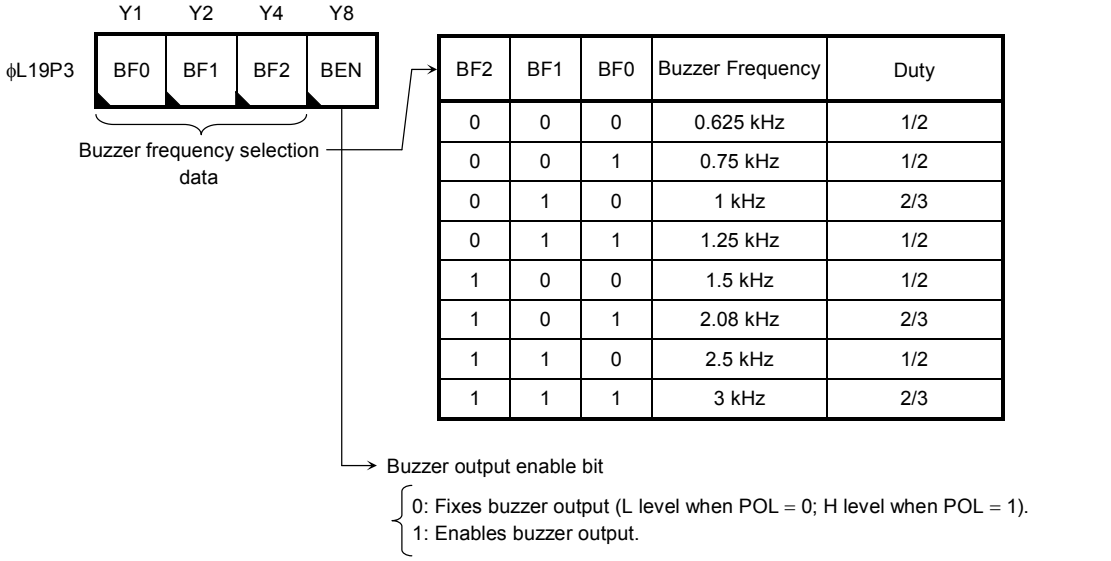
The A/D converter consists of a comparator, an A/D conversion latch, and a control circuit. Because the comparator block operates only when the BUSY bit is set to 1, the A/D converter consumes no current when not operating.

Note: Set to input ports the I/O ports corresponding to the A/D input pins used.

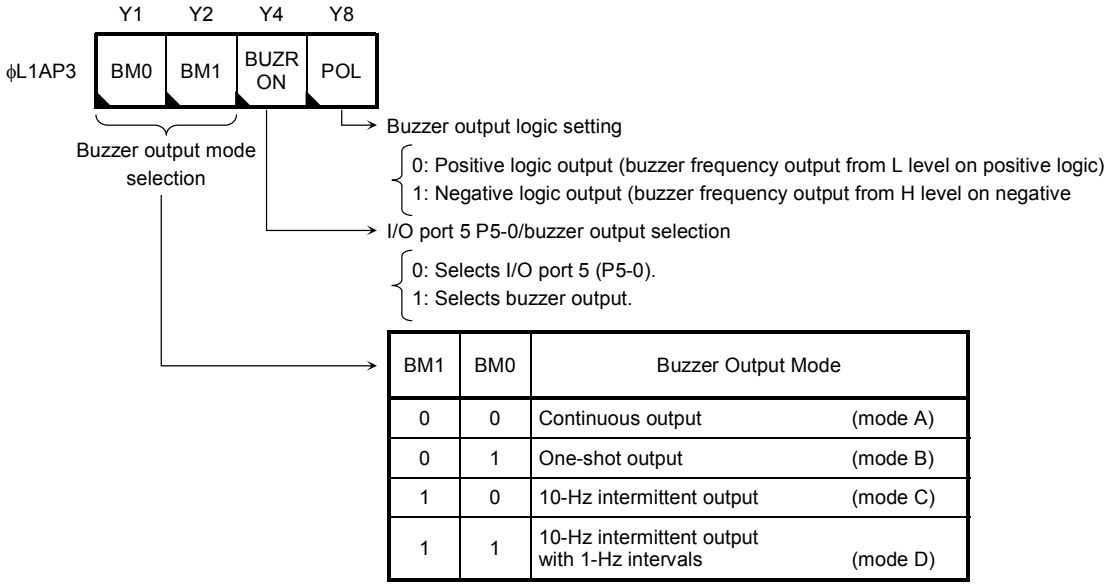
○ Buzzer Output

The buzzer output is used for such purposes as audible alarms or to issue audible confirmation for key-input or Tuning Scan mode. The buzzer frequency can be set from combinations of four output modes and eight frequencies.

1. Buzzer Control Port



BF2	BF1	BF0	Buzzer Frequency	Duty
0	0	0	0.625 kHz	1/2
0	0	1	0.75 kHz	1/2
0	1	0	1 kHz	2/3
0	1	1	1.25 kHz	1/2
1	0	0	1.5 kHz	1/2
1	0	1	2.08 kHz	2/3
1	1	0	2.5 kHz	1/2
1	1	1	3 kHz	2/3



BM1	BM0	Buzzer Output Mode	
0	0	Continuous output	(mode A)
0	1	One-shot output	(mode B)
1	0	10-Hz intermittent output	(mode C)
1	1	10-Hz intermittent output with 1-Hz intervals	(mode D)

The buzzer output uses the P5-0 I/O port. To switch the port over to buzzer output, set the BUZR ON bit to 1 and set the port to an output using the P5-0 I/O control port.

After setting the buzzer frequency, mode, and logic, setting the buzzer enable bit to 1 outputs the buzzer. When setting the buzzer conditions, set the buzzer enable bit to 0.

In continuous output (mode A), setting the buzzer enable bit to 1 outputs buzzer frequency continuously. Setting the bit to 0 terminates the buzzer output.

In one-shot output (mode B), a 50 ms sound is output every time the buzzer enable bit is set to 1. In this mode, setting the bit to 1 again during the buzzer output (50 ms) lengthens the buzzer output by 50 ms, to 100 ms. The buzzer output time can be easily adjusted. Setting the buzzer enable bit again during the 100 ms of buzzer output lengthens the output to 150 ms,

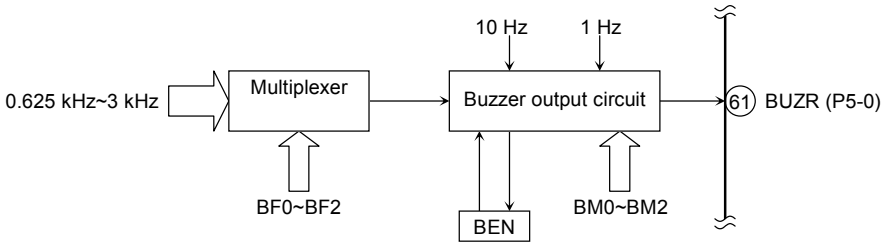
In 10-Hz intermittent output (mode C), setting the buzzer enable bit to 1 sets repetition of output for 50 ms then pause for 50 ms. Setting the bit to 0 terminates the buzzer output.

In 10 Hz intermittent output with 1 Hz intervals (mode D), setting the buzzer enable bit to 1 sets repetition of output for 50 ms then pause for 50 ms over a 500 ms period. Then, after a silent period of 500 ms the output/pause is repeated, and so on. Setting the bit to 0 terminates the buzzer output.

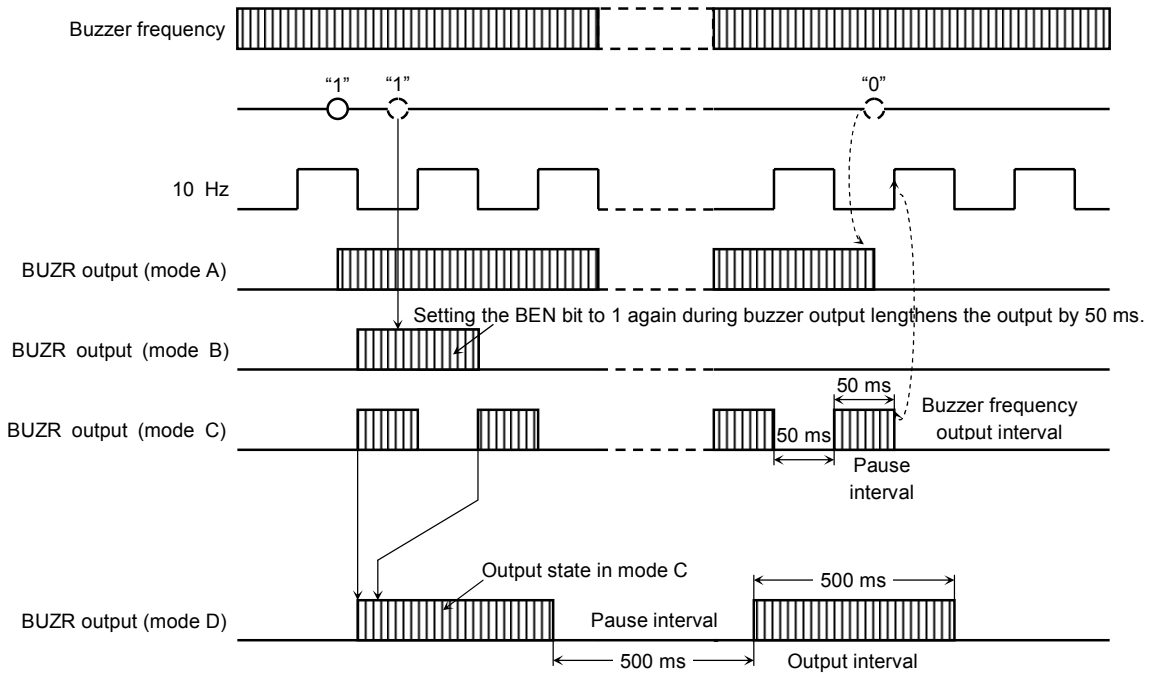
In modes B, C, and D, when the buzzer enable bit is set to 0 during buzzer output, the buzzer completes output of 50 ms before terminating. The contents of the timer port can be used to determine the buzzer output state. When the timer port 10 Hz bit is set to 0, the buzzer is output; when the bit is 1, the buzzer is paused.

Buzzer control is accessed using the OUT1 instruction with the [CN = 9N, AH] operand on I/O map page 3.

2. Buzzer Circuit Structure



3. Buzzer Output Timing

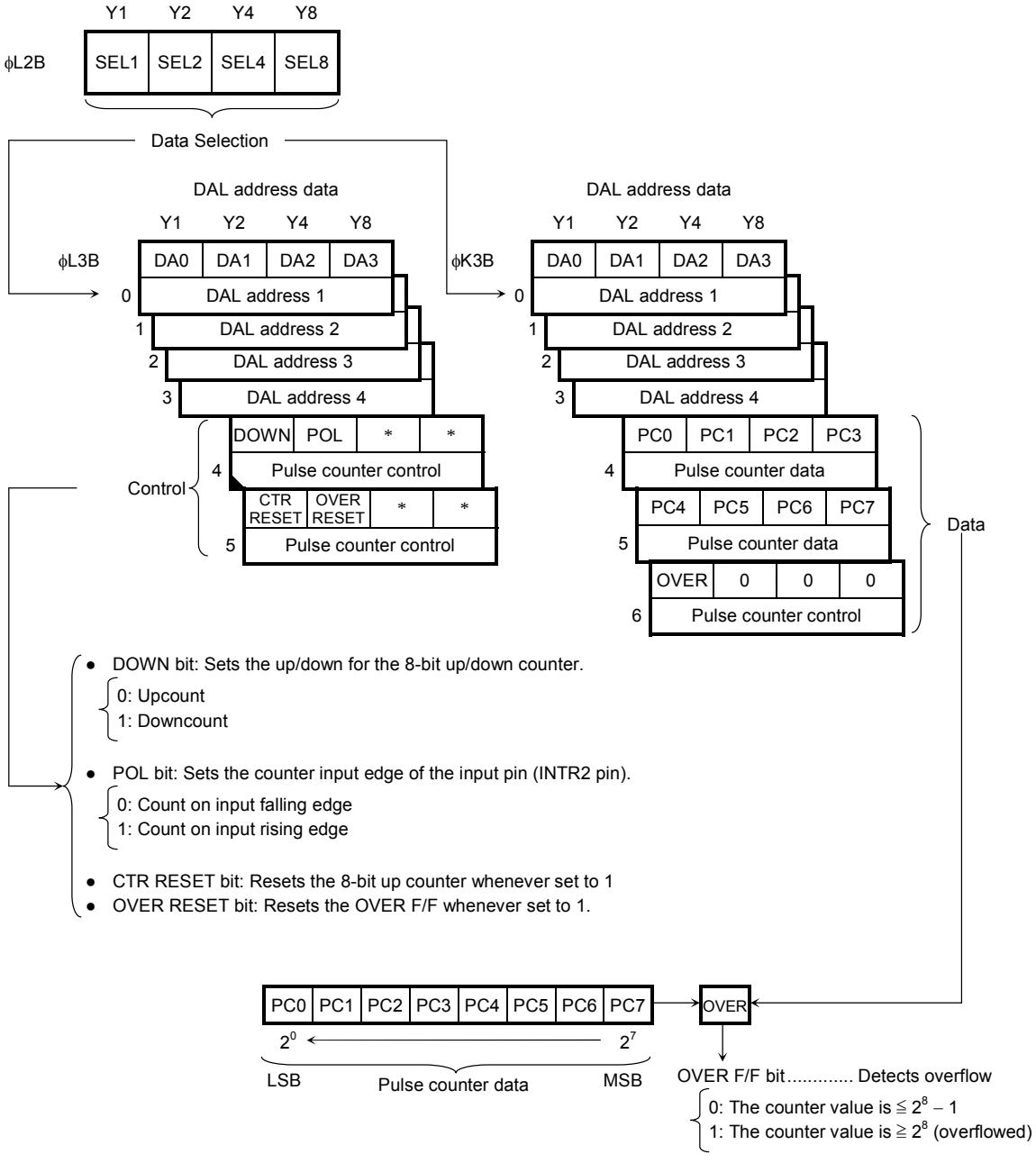


Note: When outputting the buzzer, set P4-0 to output state (set the I/O control port to 1).

○ **Pulse Counter**

The pulse counter is an 8-bit up/down counter. The pulse counter can detect the clock count during CMOS input using the INTR2 pin. This counter is useful for detecting the count when a tape is running.

1. Pulse Counter Control Port, Data Port



The pulse counter counts up the number of pulses input to the INTR2 pin.

The POL bit sets the count clock edge of the input pin. When POL is set to 0, the pulses are counted on the falling edge. When POL is set to 1, the pulses are counted on the rising edge. This bit is normally fixed.

The DOWN bit sets the up/down of the 8-bit counter. Setting DOWN to 0 specifies upcount; setting the bit to 1 specifies downcount. The bit can be freely switched between up and down counting. However, note that if a clock pulse is input while the bit is being switched, the count is cancelled.

When 2^8 or more pulses are input, the OVER F/F bit is set to 1. To count with 8 bits or higher, use OVER F/F to detect the overflows, adding or subtracting the number of overflows that occur on data memory. After an overflow is detected with OVER F/F, set the OVER RESET bit to 1 to reset OVER F/F.

The CTR RESET bit is only used to reset the 8-bit counter. Setting the bit to 1 resets the counter.

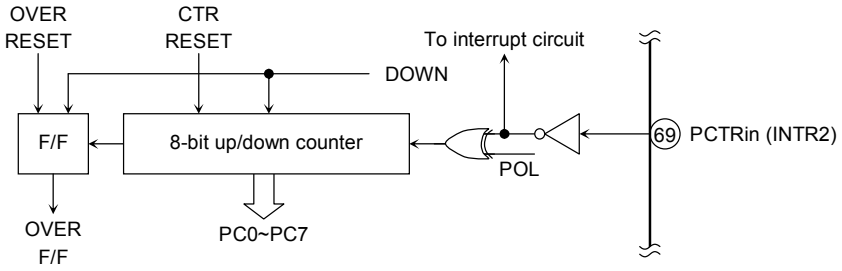
The counter data are loaded to data memory in binary format.

Pulse counter control and data loading are accessed by the OUT3/IN3 instruction with the operand [CN = BH]. These instructions are located in the DAL address register port. This port can be divided/indirectly specified and set using the data selection port (ϕL2B). Set the data of the desired port first, then access the data port later. The data selection port is incremented by 1 every time the DAL address port (ϕL3B, ϕK3B) is accessed. Accordingly, after setting the data selection port, the data can be repeatedly set.

Note: Switching the POL bit may input a clock pulse. After switching the bit, reset the counter data using the reset bit.

Note: The data selection port is automatically incremented by 1 at each access of ϕL2C, ϕL2D, ϕL2E, ϕL2F, ϕL3B, and ϕK3B.

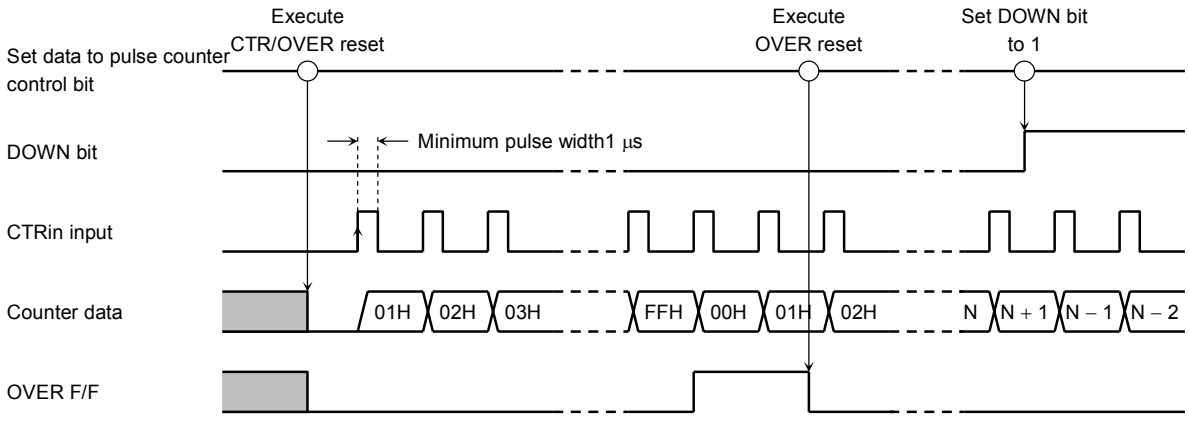
2. Pulse Counter Circuit Structure



Note: The pulse counter input is a Schmitt trigger input.

Note: The pulse counter can be used with an interrupt function (INTR2 pin input) at the same time.

3. Example of Pulse Counter Timing

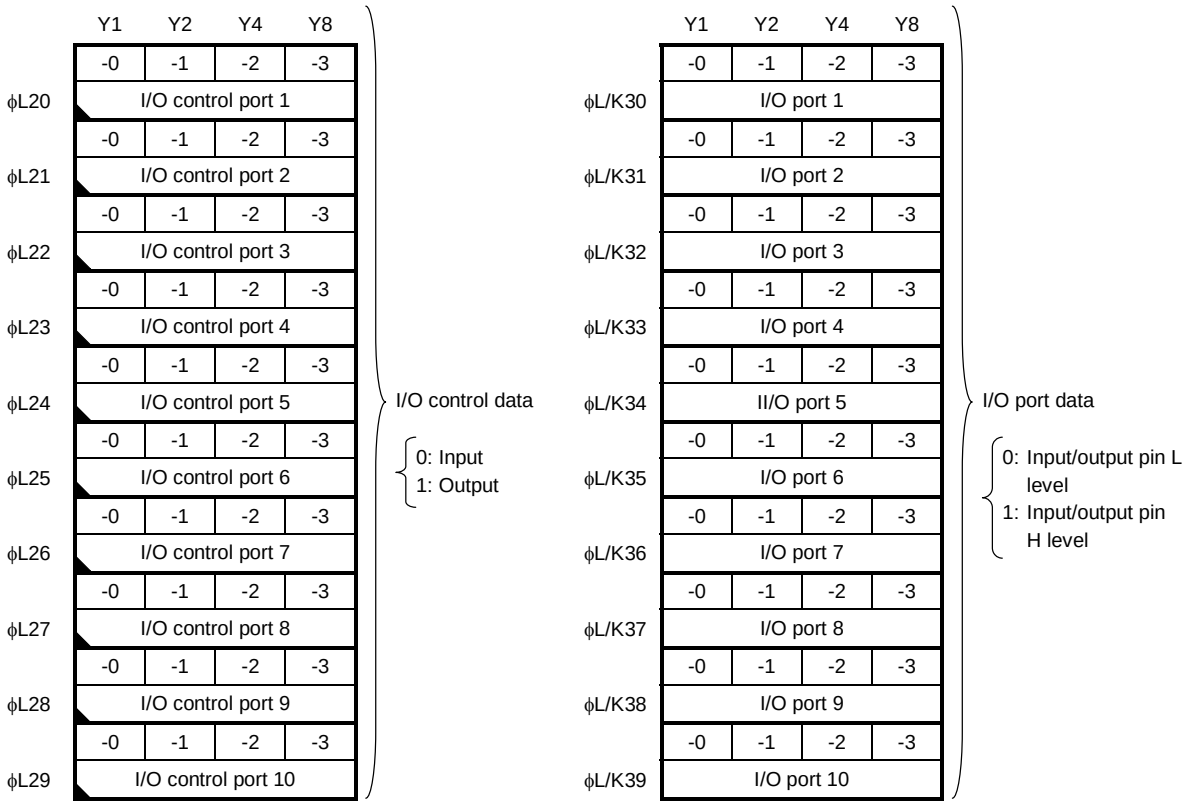


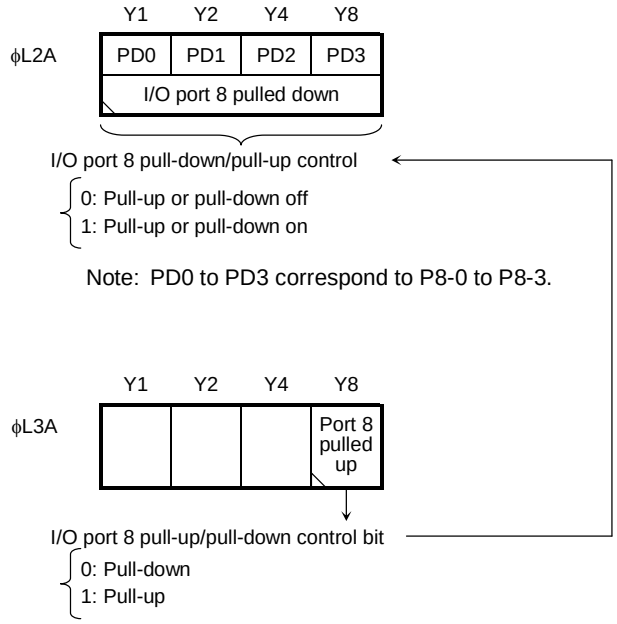
○ **Input/Output Ports (I/O Ports)**

The 40 I/O ports (derived from I/O P-1 to P-10) are used to input/output control signals. The following table shows the shared functions and the characteristics of each I/O port.

I/O Port		Shared/Additional Functions	Input	Output
I/O port 1		—	CMOS	CMOS
I/O port 2		8-bit AD converter analog input. The potential to DCREF can be inputted.		
I/O port 3				
I/O port 4	P4-0	—		
	P4-1~3	Serial interface 1/2	Schmitt trigger	
I/O port 5	P5-0	Buzzer output	CMOS	
	P5-1~3	Serial interface 3/4	Schmitt trigger	CMOS/ N-channel open drain
I/O port 6		—	CMOS	CMOS
I/O port 7				
I/O port 8		Either pulled up/pulled down can be set. Note that pulled up or pulled down must be set for all the bits		
I/O port 9		LCD driver segment output		
I/O port 10				

1. I/O Port Control, I/O Port Data





The contents of the I/O control data port set the I/O ports to input/output. To set a port to input, set the I/O control data port bit corresponding to that I/O port to 0. To set to output, set the I/O control data port bit corresponding to the I/O port to 1.

When an I/O port is set to output, the OUT3 instruction corresponding to the port controls the port's output state. The IN3 instruction reads the data currently being output into data memory. Because the data read by the IN3 instruction are used to read the pin state, these do not always match the data output by the OUT3 instruction.

When an I/O port is set to an input port, the IN3 instruction corresponding to that port is used to read the data being input to the port into data memory. At this time, the contents of the output latch do not affect the data.

When the state of an I/O port set to input changes, I/O port 8 cancels the execution of the WAIT or CKSTP instruction and restarts the CPU operation. When the I/O bit of the MUTE port is set to 1, a change in the input state likewise forcibly sets the MUTE bit to 1. In addition, the I/O port 8 pull-down control port can set the port to pull-up or pull-down state. Each pin can be pulled up or pulled down. When the port is set to 1, it can be pulled up or pulled down. The I/O port 8 pull-up/pull-down control bit switches the pull-up and pull-down states. When the control bit is set to 0 the port is pulled down. When set to 1 the port is pulled up.

The pull-up/pull-down settings are useful for a key matrix structure where an I/O port output is set as the key matrix output and (pulled-up or pulled-down) I/O port 8 is set as the input. A low-noise key matrix can be formed by the following method. If I/O port 8 is pulled down, detect key input by setting the key matrix output side to high impedance (input state), outputting/scanning an H level signal to the key input line, and reading the input state of I/O port 8. If I/O port 8 is pulled up, detect key input by outputting an L level signal to the key input line in the same way.

While the CKSTP or WAIT instruction is being executed, the key input can also be detected and the system can be restarted. If the restart is during execution of the CKSTP instruction, I/O port 1 is pulled up. Because all the I/O port outputs are set to L during Clock Stop mode, I/O port 8 waits in pulled-up state. Pressing key changes the I/O port 8 input and restarts the system. Be sure to remember that a 100-ms standby period follows the release of Clock Stop mode at this time. Because the release of the WAIT instruction holds the output state, the system can be restarted either by a pull-up or pull-down, and because there is no standby after the release of the WAIT instruction, a key input can be immediately detected or implemented. Current dissipation can be minimized by using both these backup modes together.

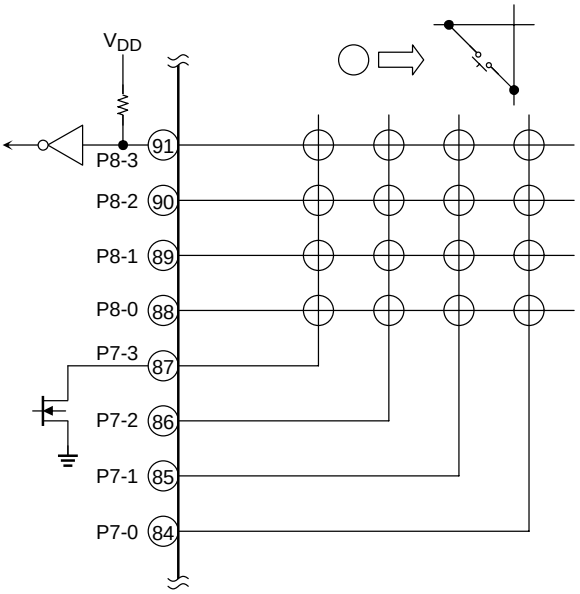
As the I/O port 8 input is the inverter input, I/O port 8 input cannot be used for methods involving intermediate potential. However, because other I/O ports input is on only when the input instruction is executed, inputting intermediate potential will not result in abnormal current dissipation. This allows such advantages as pull-ups with a lower potential than the V_{DD} potential and the use of three-value output.

I/O ports 2 and 3 are CMOS I/O ports, also used for 8-bit A/D converter input.

I/O ports 4 and 5 are CMOS I/O ports. Pin P5-0 is also used for the buzzer output. Pins P4-1 to 3 and P5-1 to 3 are also used as serial interface pins.

I/O ports 6 and 7 are CMOS I/O ports.

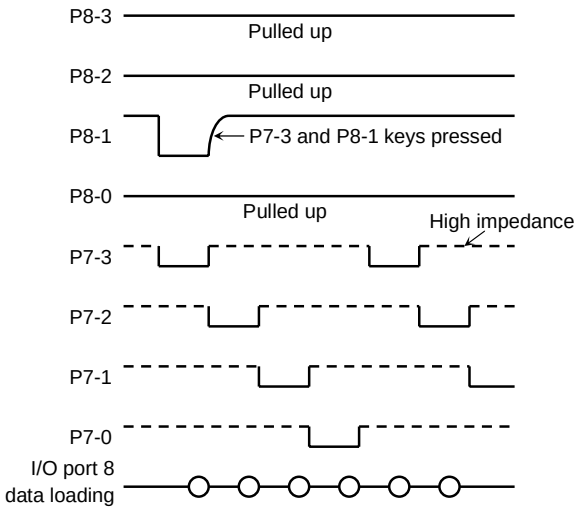
I/O ports 9 and 10 are CMOS I/O ports and are also used as the LCD driver. A reset sets these pins as I/O port input pins.



Example of Key Input Matrix Circuit Structure

The diagram on the left is an example of the structure of a key input matrix circuit. When no key is pressed, the ports are pulled up. Pressing a key inputs a source side (I/O port 9) L level signal. Be sure to keep in mind the time for the transition from L level to key input pull-up.

Setting all the key source-side ports to L during WAIT instruction execution releases the WAIT instruction whenever a key is pressed.



○ **Register Ports**

The G-register, the data register, and the DAL address register mentioned in the CPU description are treated as an internal port.

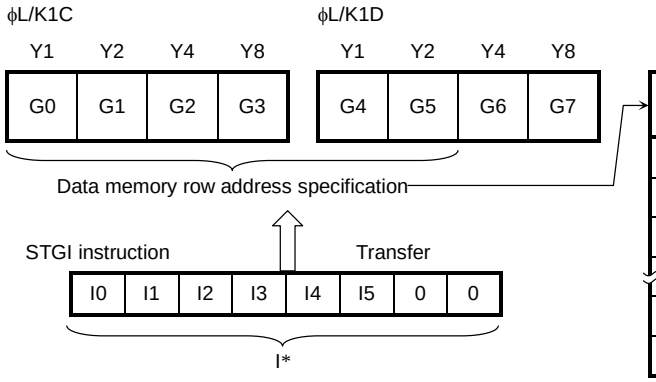
1. G-Register (ϕKL1C, ϕKL1D)

This register addresses the row address (DR = 04H to FFH) in data memory for the MVGD and MVGS instructions. This register is accessed by the OUT1/IN1 instruction with the operand [CN = CH to DH]. Using the STGI instruction, data can be set in the register with just one instruction.

Note: The register value is only valid for the MVGD or MVGS instructions. The register is ignored for other instructions. The MVGD and MVGS instructions have no effect on this register.

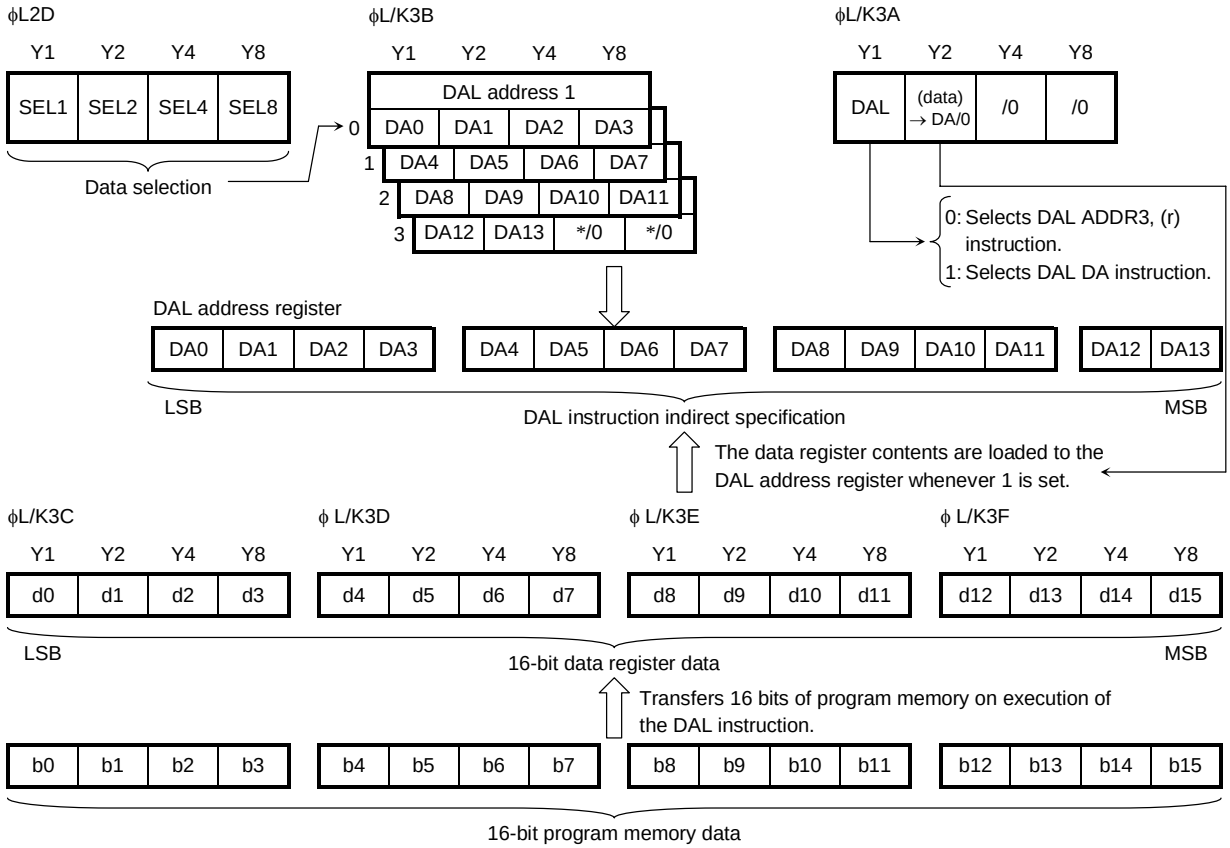
Note: Setting data 00H to FFH in the G-register allows all the data memory row addresses to be specified indirectly. (DR = 00H to FFH)

Note: This register can be both read and written. If necessary, at an interrupt, save and restore the register contents using data memory.



G7	G6	G5	G4	G3	G2	G1	G0	DR
0	0	0	0	0	1	0	0	04H
0	0	0	0	0	1	0	1	05H
0	0	0	0	0	1	1	0	06H
1	1	1	1	1	1	1	0	FEH
1	1	1	1	1	1	1	1	FFH

2. Data Register (ϕKL3C to ϕKL3F), DAL Address Register (ϕKL3B0 to ϕKL3B3), and Control Bits



The data register is a 16-bit register to load the program memory data when the DAL instruction is executed. The contents of the register are accessed in 4-bit units by the OUT1/IN1 instruction with the operand [CN = CH to FH]. This register can be used for such purposes as LCD segment decoding, radio band edge data, and coefficient data for binary-to-BCD conversion.

The DAL address register (DA) is a 14-bit register to indirectly specify program memory when the DAL instruction is executed. The DAL instruction has two operations, selected by the DAL bit. Setting DAL to 0 sets the program memory reference address to ADDR3 (6 bits) and the contents of the general register (r) in the operand. Setting DAL to 1 sets the reference address to the 14 bits of the DAL address register. Executing the DAL instruction with the DAL bit set to 0 sets the reference area to 0000H to 03FFH in program memory. However, executing the DAL instruction with the DAL bit set to 1 allows the whole program memory area (0000H to 3FFFH) to be referenced.

Setting the (DATA) → DA bit to 1 transfer the data register contents to the 14-bit DAL address register with one instruction.

The contents of the DAL address register can be accessed in 4-bit units by the OUT3/IN3 instruction with the operand [CN = BH]. The DAL address register port can be divided/indirectly specified and set by the data selection port (øL2B). First set the data for the port you wish to set, then access the corresponding data port. The data selection port is incremented by 1 every time that port (ϕL3B, ϕK3B) is accessed. Accordingly, after setting the data selection port, the port can be repeatedly accessed.

The DAL bit and (DATA) → DA bit can be accessed by the OUT3 instruction with the operand [CN = AH].

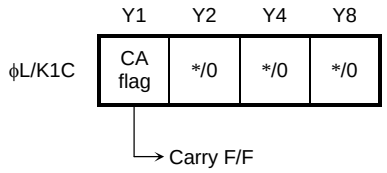
Note: The DAL address register is valid only at execution of the DAL instruction when the DAL bit is set to 1. The execution of other instructions has no effect on the register. The DAL instruction also does not affect the register.

Note: The data register and DAL address register can be read and written. If necessary, at an interrupt, save and restore its contents using data memory.

Note: Setting the (DATA) → DA bit to 0 performs no operation. When ϕK3A is accessed, only the DAL bit is read. (Other bits are 0.)

3. Carry F/F (Ca Flag, ϕKL1B)

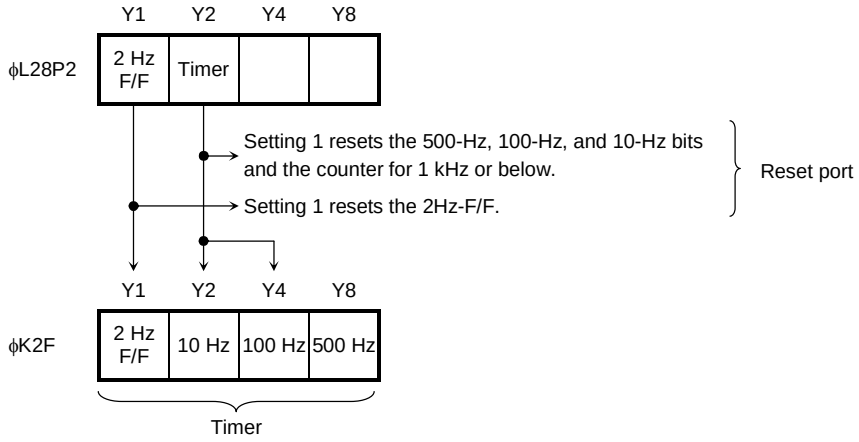
This F/F is set when a carry or borrow occurs as the result of an arithmetic instruction. The F/F is reset if a carry or borrow does not occur. The carrier F/F can be accessed by the OUT1/IN1 instruction with the operand [CN = BH]. Accordingly, the carry F/F can be easily saved and restored when an interrupt occurs. When saving, use the IN1 instruction to write the carry F/F to data memory. When restoring, use the OUT1 instruction to transfer the saved data from data memory to the carry F/F.



○ Timer Port

The timer has 500-Hz, 100-Hz, 10-Hz, and 2-Hz F/F bits. These are used for such purposes as clock operations or Tuning Scan mode counts.

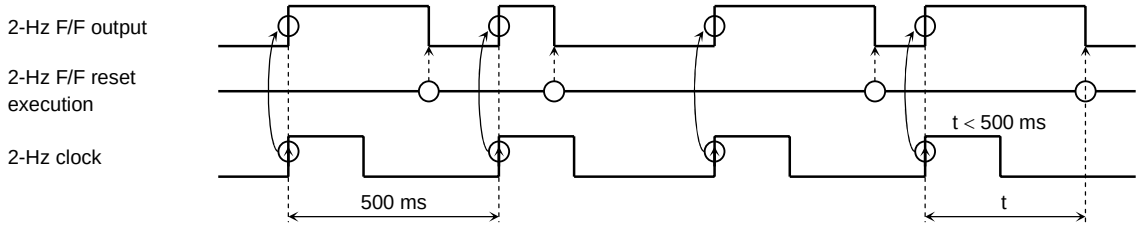
1. Timer Port



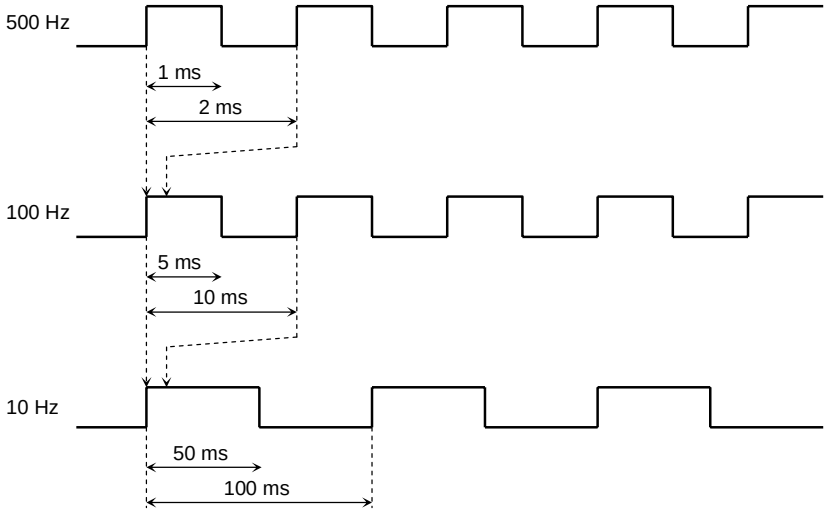
The timer port is accessed by the OUT2 instruction with the operand [CN = 8H] and the IN2 instruction with the operand [CN = FH] on IO map page 2.

2. Timer Port Timing

The 2-Hz timer F/F is set by the 2-Hz (500 ms) signal, and reset by setting the RESET port 2-Hz F/F to 1. This bit can normally be used for the clock count.
The 2-Hz timer F/F is only reset by the RESET port 2-Hz F/F. Therefore, if the F/F is not reset within 500 ms, the next count is missed and the correct time is not obtained.



The 10-Hz, 100-Hz, and 500-Hz timers are output to the 10-Hz, 100-Hz, and 500-Hz bits with a cycle of 100 ms, 10ms, and 2 ms, respectively, and a pulse duty of 50%. Whenever the RESET port timer bit is set to 1, counters below 1 kHz are reset.



○ Output Ports (Also Function as LCD Driver Pins)

The output port includes 30 CMOS output ports, which also function as the LCD driver. The LCD OFF bit is used to switch the port to an output port. Setting the LCD OFF bit to 1 sets the port to an output port. The data output to the output port can be accessed by the OUT2 instruction with the operand [CN = CH]. These data can be divided/indirectly specified and set using the data selection port (ϕL2B). First set the data for the segment data port you wish to set, then access the corresponding data port.

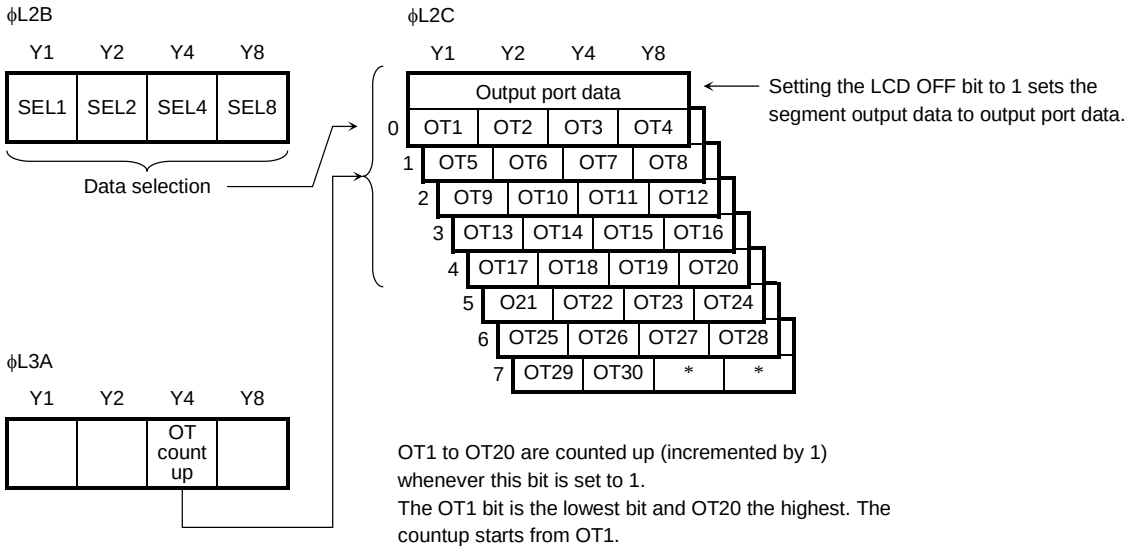
The data selection port is incremented by 1 every time a general-purpose output data port (ϕL2C) is accessed. Accordingly, after setting the data selection port, the data can be repeatedly set.

In OT1 to OT20, output data can be incremented by 1 in one instruction by using the OT count UP bit. Therefore, OT1 to OT20 can be used for the address signal output when using external memory.

Note: The data selection port is automatically incremented by 1 whenever ϕL2C, ϕL2D, ϕL2E, ϕL2F, ϕL3B, or ϕK3B on the I/O map are accessed.

Note: Setting the OT count UP bit to 0 sets no count up.

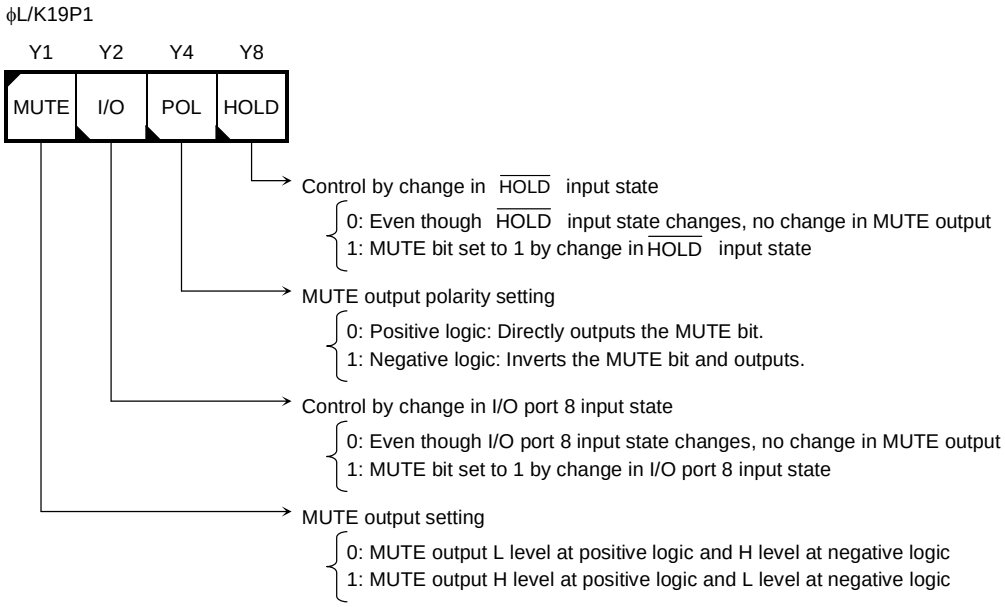
Note: See the LCD driver section.



○ **MUTE Output**

This is a 1-bit CMOS output port for muting control.

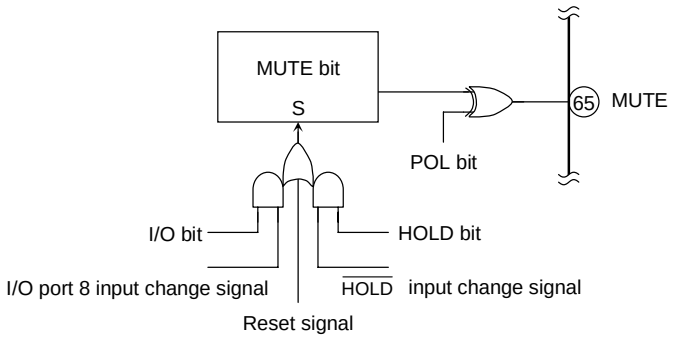
1. MUTE Port



The MUTE port is accessed by the OUT1/IN2 instruction with the operand [CN = 9H]. The MUTE output is used for muting control. At such times as switching bands and turning the radio off using the I/O port 8 and $\overline{HOLD}$ input, the MUTE bit can be set to 1 to prevent linear circuit switching noise. The I/O bit and HOLD bit control the MUTE bit.

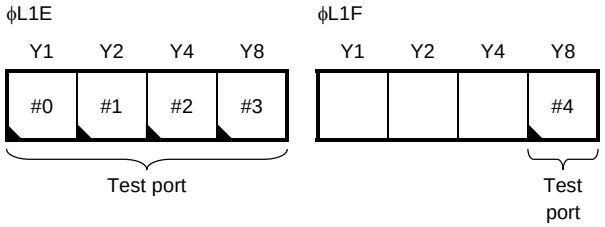
The POL bit sets the MUTE output logic. Set depending on your specifications.

2. MUTE Output Circuit Structure



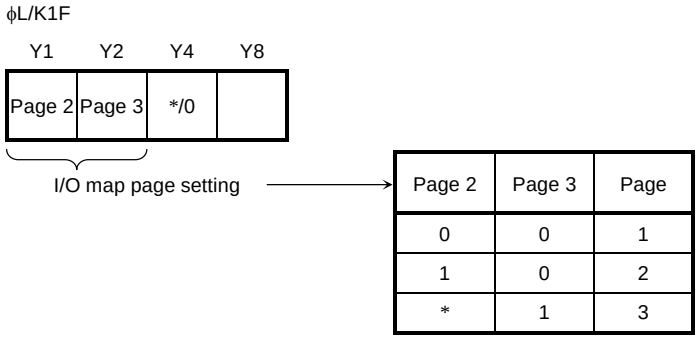
○ Test Ports

These are internal ports for testing the device's functions. The ports are accessed by the OUT1 instruction with the operand [CN = EH, FH]. The ports are normally set to 0.



○ Test Page

This port sets pages 1 to 3 of the I/O map. The port is accessed by the OUT1/IN1 instruction with the operand [CN = FH].



Page 2	Page 3	Page
0	0	1
1	0	2
*	1	3

○ Using as Emulator Chip

When an H level voltage is supplied to the TEST pin (Test mode), the device functions as an emulator chip. Three test modes are supported. A software development tool can be configured using two devices.

Connecting this software development tool and a tuner IC enables you to check radio operations while developing software.

For the development tool specifications, refer to the TC9325FG software development tool specification sheet.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage 1	V_{DD1}	−0.3~4.0	V
Power supply voltage 2	V_{DD2}	−0.3~6.0	V
Input voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power dissipation	P_D	400	mW
Operating temperature	T_{opr}	−40~85	°C
Storage temperature	T_{stg}	−65~150	°C

Electrical Characteristics (unless otherwise specified, Ta = –40~85°C, V_{DD} = 3.0~3.6 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD}	—	—	3.0	3.3	3.6	V
Memory hold voltage range	VHD	—	Crystal oscillation stopped (CKSTP instruction executed)	2.0	~	3.6	V
Operating power supply current	I_{DD1}	—	When PLL operating (VHF mode) and at FMin = 230 MHz input, Ta = 25°C, V_{DD} = 3.3 V	—	3.5	7.0	mA
	I_{DD2}	—	When CPU only operating (4.5-MHz clock operating, 75-kHz oscillation stopped PLL off, display lit), Ta = 25°C, V_{DD} = 3.3 V	—	1.0	2.0	
	I_{DD3}	—	When CPU only operating (75-kHz clock operating, 4.5-MHz oscillation stopped, PLL off, display lit), Ta = 25°C, V_{DD} = 3.3 V	—	0.25	0.50	
	I_{DD4}	—	In Hard Wait mode (4.5-MHz crystal only operating), Ta = 25°C, V_{DD} = 3.3 V	—	150	—	μA
	I_{DD5}	—	In Hard Wait mode (75-kHz crystal only operating), Ta = 25°C, V_{DD} = 3.3 V	—	100	—	
	I_{DD6}	—	When soft wait executed (PLL off, CPU operating intermittently on 4.5-MHz clock, display lit), Ta = 25°C, V_{DD} = 3.3 V	—	300	—	
	I_{DD7}	—	When soft wait executed (PLL off, CPU operating intermittently on 75-kHz clock, display lit), Ta = 25°C, V_{DD} = 3.3 V	—	250	—	
Memory hold current	IHD	—	Crystal oscillator stopped (CKSTP instruction executed)	—	0.1	10	μA
Crystal oscillator frequency	fXT1	—	Crystal oscillator 1 (X_{IN1}, X_{OUT1})	—	4.5	—	MHz
	fXT2	—	Crystal oscillator 2 (X_{IN2}, X_{OUT2})	—	75	—	kHz
Crystal oscillation startup time	tst	—	Crystal oscillator fXT2 = 75 kHz (X_{IN2}, X_{OUT2})	—	—	1.0	s
Low voltage detection voltage	VSTOP	—	(VCPU), STOP F/F bit detected	2.15	2.40	2.70	V

Programmable Counter and IF Counter Operating Frequency Ranges

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	fVHF	—	V_{IN} = 0.2 V_{p-p}	50	~	230	MHz
FMin (FM mode)	fFM1	—	V_{IN} = 0.1 V_{p-p}	50	~	140	
	fFM2	—	V_{IN} = 0.1 V_{p-p}	10	~	60	
AMin (HF mode)	fHF	—	V_{IN} = 0.1 V_{p-p}	1.0	~	30	
AMin (LF mode)	fLF	—	V_{IN} = 0.1 V_{p-p}	0.5	~	20	
IFIN1, IFIN2	fIF	—	V_{IN} = 0.1 V_{p-p}	0.3	~	20	

Programmable Counter and IF Counter Input Oscillation Ranges

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
FMin (VHF mode)	VVHF	—	fVHF	0.2	~	1.0	V_{p-p}
FMin (FM mode)	VFM	—	fFM1/fFM2	0.1	~	1.0	
AMin (HF mode)	VHF	—	fHF	0.1	~	1.0	
AMin (LF mode)	VLF	—	fLF	0.1	~	1.0	
IFIN1, IFIN2	VIF	—	fIF	0.1	~	1.0	

LCD Common Outputs/Segment Outputs (COM~COM4, S1~S22)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Bias output voltage	GND level	VBS1	—	V_{DD} = 3.3 V, no load	—	0.00	0.15	V
	1/3 V_{DD} level	VBS2	—	V_{DD} = 3.3 V, no load	0.95	1.10	1.25	
	1/2 V_{DD} level	VBS3	—	V_{DD} = 3.3 V, no load	1.50	1.65	1.80	
	2/3 V_{DD} level	VBS4	—	V_{DD} = 3.3 V, no load	2.05	2.20	2.35	
	V_{DD} level	VBS5	—	V_{DD} = 3.3 V, no load	3.15	3.30	—	

Output Ports and I/O Ports (OT1~OT30, P1-0~P10-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	IOH1	—	V_{DD} = 3.3 V, V_{OH} = V_{DD} − 0.3 V	−0.30	−0.80	—	mA
	Low level	IOL1	—	V_{DD} = 3.3 V, V_{OL} = 0.3 V, except for P5-1 to P5-3	0.30	0.80	—	
		IOL2	—	V_{DD2} = 3.3 V, V_{OL} = 0.3 V, P5-1~P5-3	1.50	4.00	—	
Input leakage current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V (P1-0~P10-3)	—	—	±1.0	μA
Input voltage	High level	V_{IH}	—	(P1-0~P10-3)	V_{DD} × 0.8	~	V_{DD}	V
	Low level	V_{IL}	—	(P1-0~P10-3)	0	~	V_{DD} × 0.2	
Input pulled-up/down resistor		RIN1	—	Ta = 25°C, When P8-0 to P8-3 pulled up/down	30	60	120	kΩ

MUTE, DO1, DO2 Output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	High level	IOH1	—	V_{DD} = 3.3 V, V_{OH} = V_{DD} − 0.3 V	−0.30	−0.80	—	mA
	Low level	IOL1	—	V_{DD} = 3.3 V, V_{OL} = 0.3 V	0.30	0.80	—	
Output off leakage current		ITL	—	V_{DD} = 3.3 V, VTLH = 3.3 V, VTLL = 0 V (DO1, DO2)	—	—	±100	nA

$\overline{\text{HOLD}}$, INTR1/2, IN1/2 Input Ports, $\overline{\text{RESET}}$ Input

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V	—	—	±1.0	μA
Output current	High level	V_{IH}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	Low level	V_{IL}	—	—	0	~	V_{DD} × 0.2	

AD Converter (ADIN1~ADIN8, DCREF)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	VAD	—	ADin1~ADin8	0	~	V_{DD}	V
Resolution	VRES	—	—	—	8	—	bit
Linear error	—	—	—	—	±0.5	±1.0	LSB
Conversion total error	—	—	—	—	±1.0	±2.0	
Analog input leakage	ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V, (ADin1~ADin8)	—	—	±1.0	μA
Reference voltage input current	IREF	—	Ta = 25°C, V_{DD} = 3.3 V, DCREF = 3.3 V (DCREF)	—	0.35	0.70	mA

Crystal Oscillators

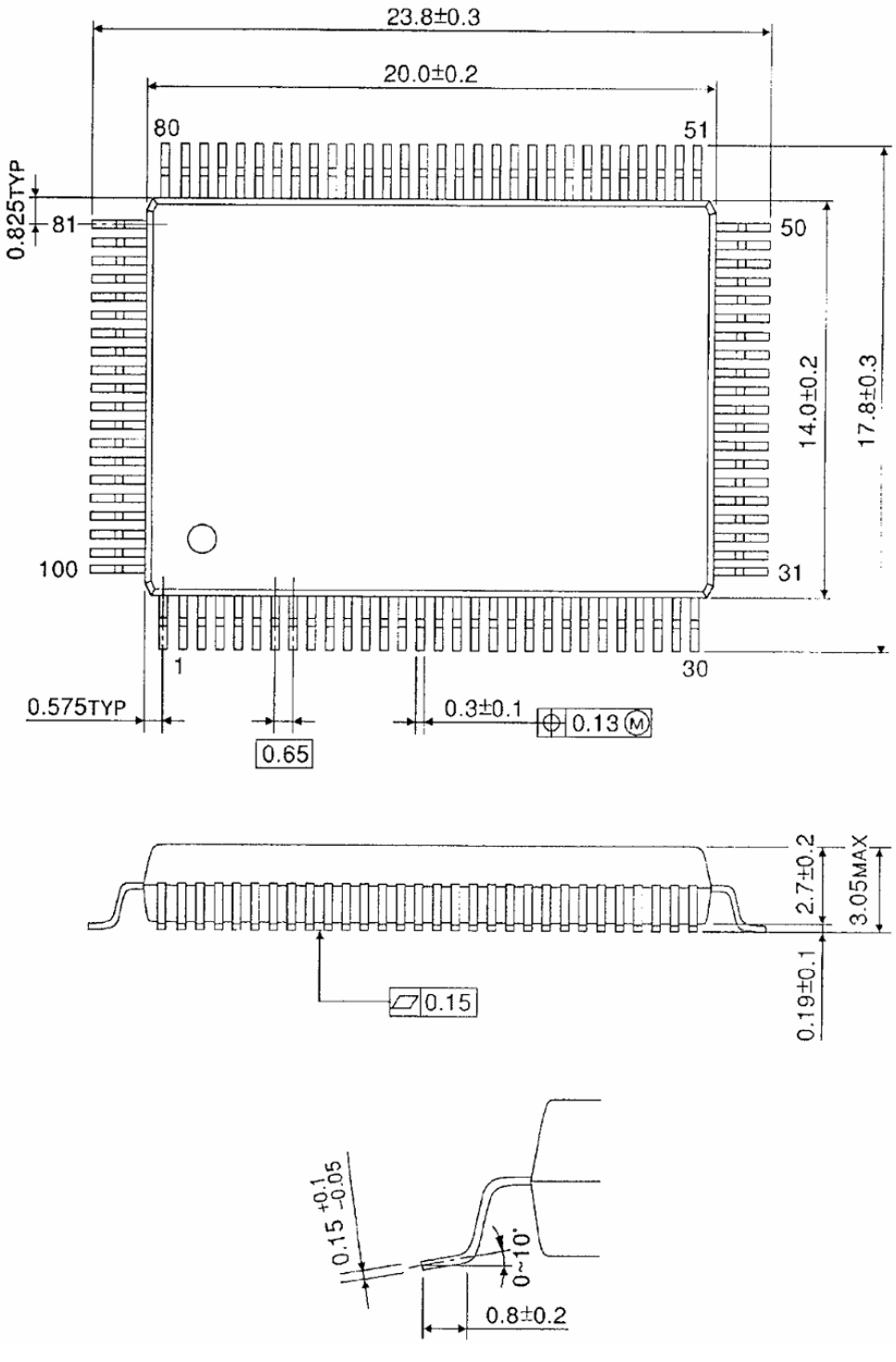
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
X_{IN1} amp feedback resistance	RfXT1	—	V_{DD} = 3.3 V, (X_{IN1}–X_{OUT1})	—	1.0	—	MΩ
X_{IN2} amp feedback resistance	RfXT2	—	V_{DD} = 3.3 V, (X_{IN2}–X_{OUT2})	—	10	—	
X_{OUT1} output resistance	ROUT1	—	Ta = 25°C, (X_{OUT1})	2.0	4.0	8.0	kΩ
X_{OUT2} output resistance	ROUT2	—	Ta = 25°C, (X_{OUT2})	2.5	5.0	10.0	

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pulled-down resistance	RIN2	—	Ta = 25°C, (TEST)	30	60	120	kΩ
Input amp feedback resistance	RfIN	—	Ta = 25°C, V_{DD} = 3.3 V (FMin, AMin, IFin1, IFin2)	0.5	1.0	2.0	

Package Dimensions

P-QFP100-1420-0.65 Q Unit : mm



Weight: 1.6 g (typ.)

Note: Lead type PD-Pff

RESTRICTIONS ON PRODUCT USE

030619EBA

- The information contained herein is subject to change without notice.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- TOSHIBA products should not be embedded to the downstream products which are prohibited to be produced and sold, under any law and regulations.