

NTD3055-150, NVD3055-150

MOSFET – Power, N-Channel, DPAK/IPAK 9.0 A, 60 V

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 10 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive ($t_p \leq 10 \text{ ms}$)	V_{GS} V_{GS}	± 20 ± 30	Vdc
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Continuous @ $T_A = 100^\circ\text{C}$ – Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_D I_D I_{DM}	9.0 3.0 27	Adc Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	28.8 0.19	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		2.1	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		1.5	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $L = 1.0 \text{ mH}$, $I_L(\text{pk}) = 7.75 \text{ A}$, $V_{DS} = 60 \text{ Vdc}$)	E_{AS}	30	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	5.2 71.4 100	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

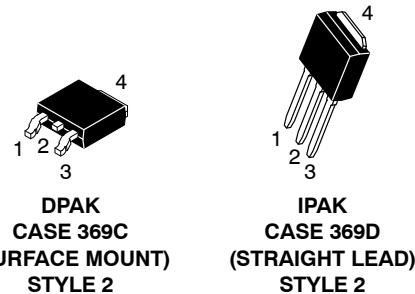
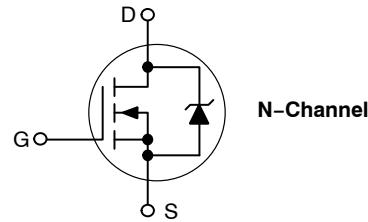
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



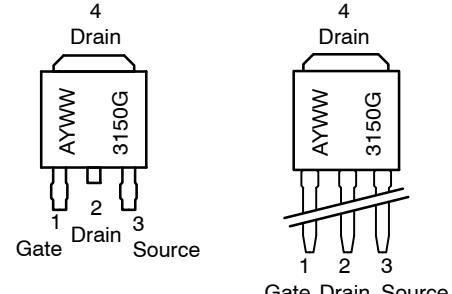
ON Semiconductor®

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9.0 AMPERES, 60 VOLTS
 $R_{DS(on)} = 122 \text{ m}\Omega$ (Typ)



MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location*
3150 = Device Code
Y = Year
WW = Work Week
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD3055-150, NVD3055-150

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0$ Vdc, $I_D = 250$ μAdc)	$V_{(\text{BR})\text{DSS}}$	60	—	—	Vdc
Temperature Coefficient (Positive)		—	70.2	—	$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 60$ Vdc, $V_{GS} = 0$ Vdc) ($V_{DS} = 60$ Vdc, $V_{GS} = 0$ Vdc, $T_J = 150^\circ\text{C}$)	I_{DSS}	—	—	1.0 10	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250$ μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(\text{th})}$	2.0 —	3.0 6.4	4.0 —	Vdc $\text{mV}/^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10$ Vdc, $I_D = 4.5$ Adc)	$R_{DS(\text{on})}$	—	122	150	$\text{m}\Omega$
Static Drain-to-Source On-Voltage (Note 3) ($V_{GS} = 10$ Vdc, $I_D = 9.0$ Adc) ($V_{GS} = 10$ Vdc, $I_D = 4.5$ Adc, $T_J = 150^\circ\text{C}$)	$V_{DS(\text{on})}$	— —	1.4 1.1	1.9 —	Vdc
Forward Transconductance (Note 3) ($V_{DS} = 7.0$ Vdc, $I_D = 6.0$ Adc)	g_{FS}	—	5.4	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25$ Vdc, $V_{GS} = 0$ Vdc, $f = 1.0$ MHz)	C_{iss}	—	200	280	pF
Output Capacitance		C_{oss}	—	70	100	
Transfer Capacitance		C_{rss}	—	26	40	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{DD} = 48$ Vdc, $I_D = 9.0$ Adc, $V_{GS} = 10$ Vdc, $R_G = 9.1$ Ω) (Note 3)	$t_{d(\text{on})}$	—	11.2	25	ns
Rise Time		t_r	—	37.1	80	
Turn-Off Delay Time		$t_{d(\text{off})}$	—	12.2	25	
Fall Time		t_f	—	23	50	
Gate Charge	$(V_{DS} = 48$ Vdc, $I_D = 9.0$ Adc, $V_{GS} = 10$ Vdc) (Note 3)	Q_T	—	7.1	15	nC
		Q_1	—	1.7	—	
		Q_2	—	3.5	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 9.0$ Adc, $V_{GS} = 0$ Vdc) (Note 3) ($I_S = 19$ Adc, $V_{GS} = 0$ Vdc, $T_J = 150^\circ\text{C}$)	V_{SD}	—	0.98 0.86	1.20 —	Vdc
Reverse Recovery Time	$(I_S = 9.0$ Adc, $V_{GS} = 0$ Vdc, $dI_S/dt = 100$ A/ μs) (Note 3)	t_{rr}	—	28.9	—	ns
		t_a	—	21.6	—	
		t_b	—	7.3	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.036	—	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs , Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NTD3055-150, NVD3055-150

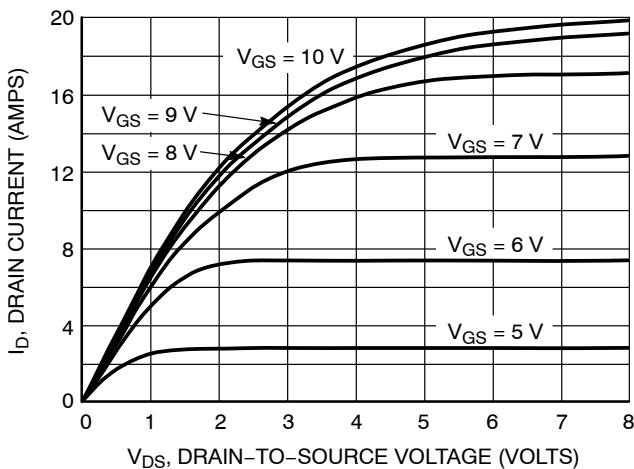


Figure 1. On-Region Characteristics

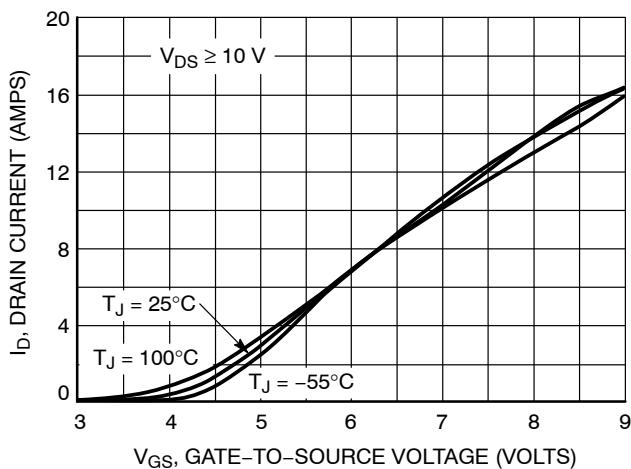


Figure 2. Transfer Characteristics

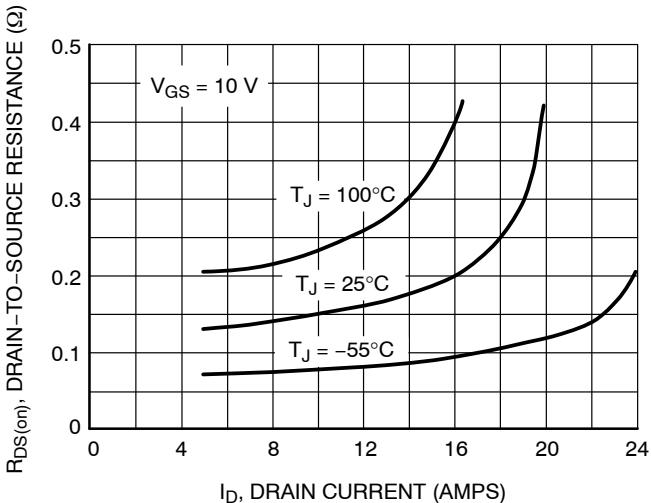


Figure 3. On-Resistance versus Gate-to-Source Voltage

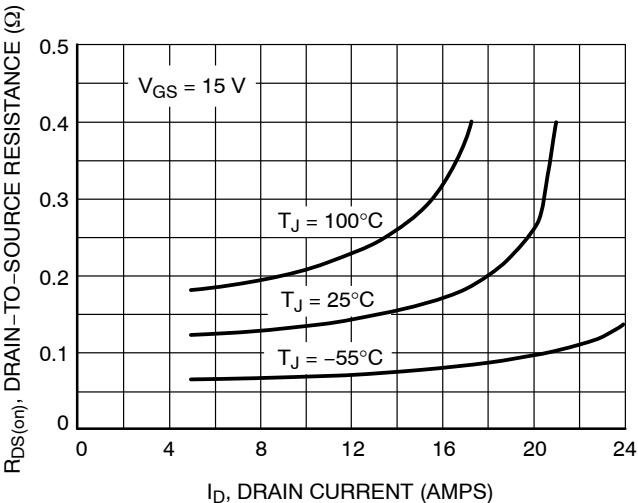


Figure 4. On-Resistance versus Drain Current and Gate Voltage

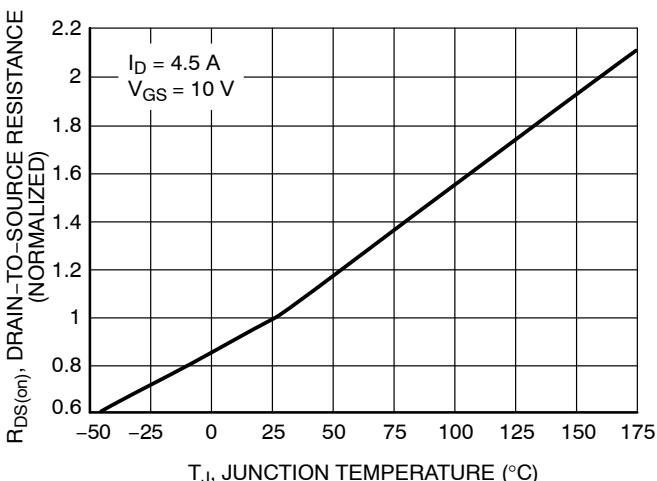


Figure 5. On-Resistance Variation with Temperature

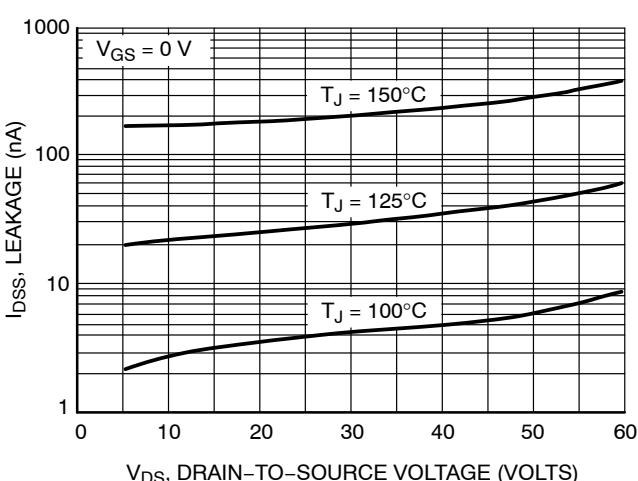


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD3055-150, NVD3055-150

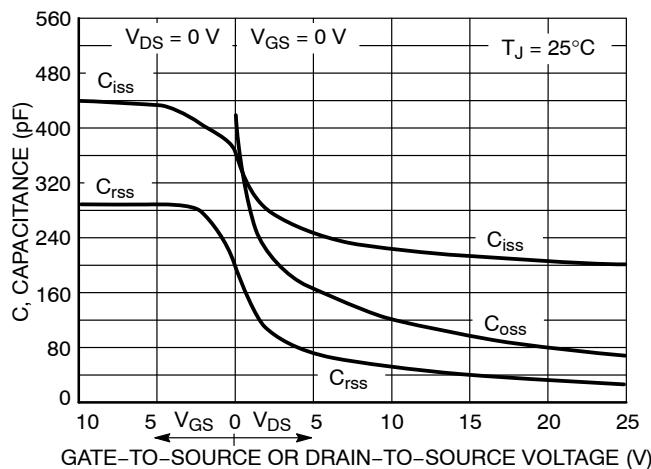


Figure 7. Capacitance Variation

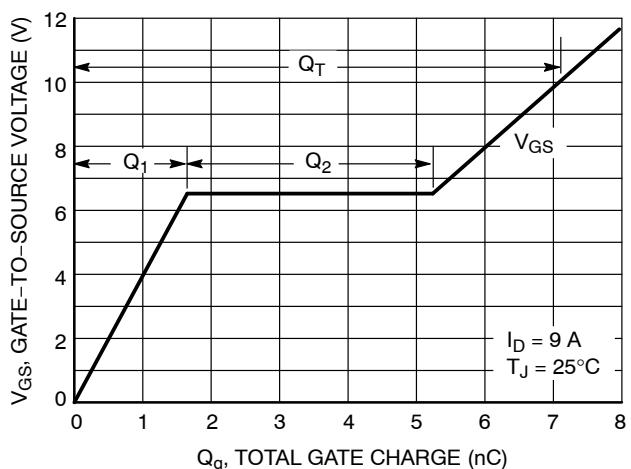


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

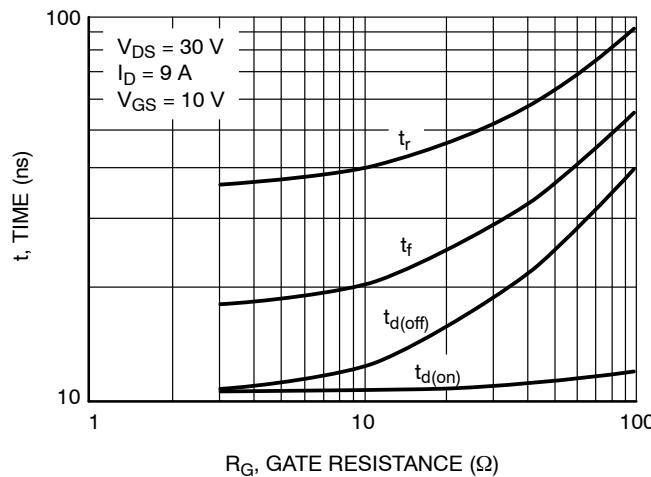


Figure 9. Resistive Switching Time Variation versus Gate Resistance

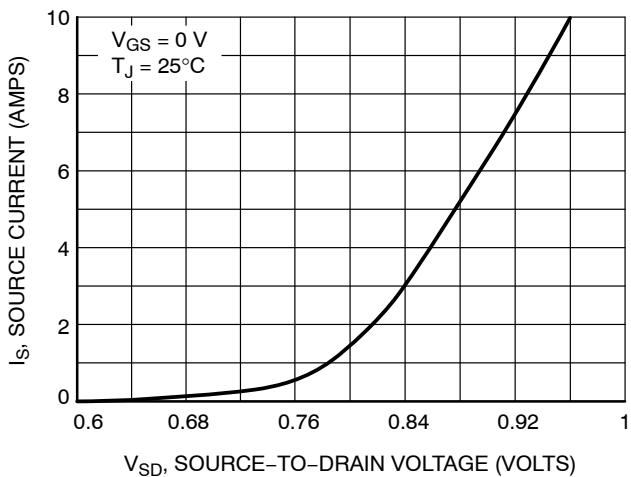


Figure 10. Diode Forward Voltage versus Current

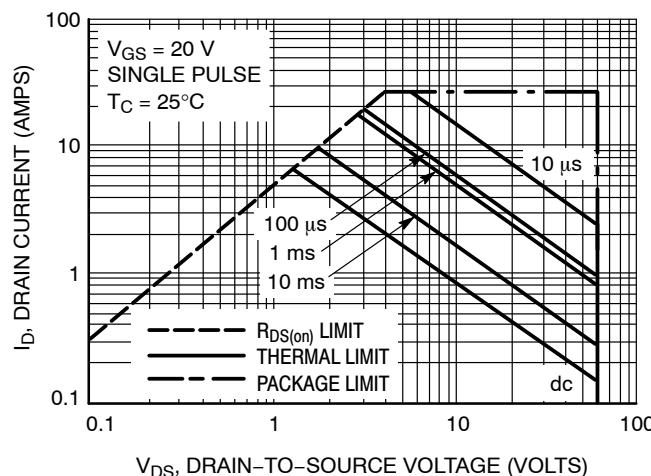


Figure 11. Maximum Rated Forward Biased Safe Operating Area

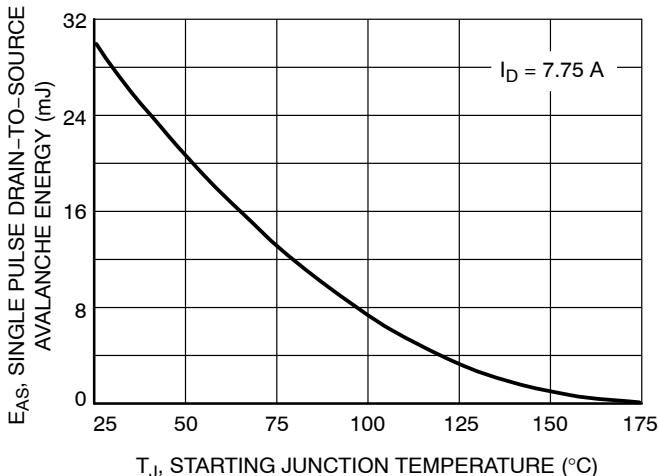


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

NTD3055-150, NVD3055-150

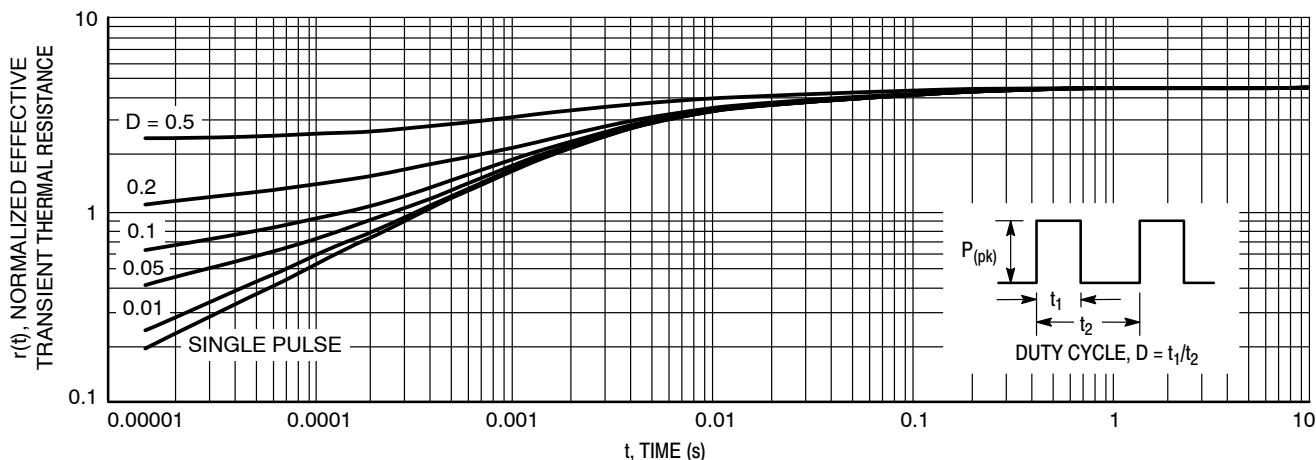


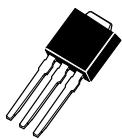
Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD3055-150G	DPAK (Pb-Free)	75 Units / Rail
NTD3055-150-1G	IPAK (Pb-Free)	75 Units / Rail
NTD3055-150T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD3055-150T4H	DPAK (Halide-Free)	2500 / Tape & Reel
NVD3055-150T4G*	DPAK (Pb-Free)	2500 / Tape & Reel
NVD3055-150T4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

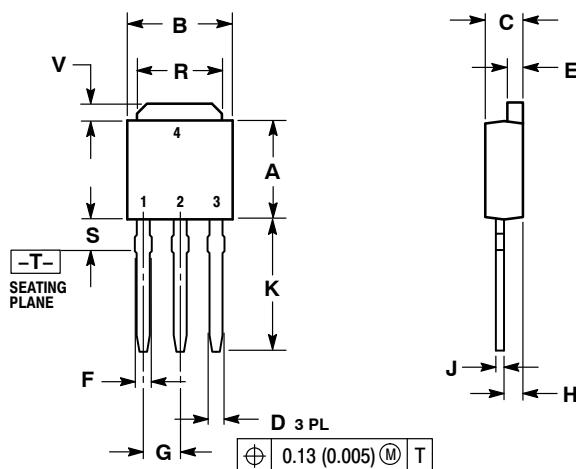


DPAK INSERTION MOUNT

CASE 369
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



NOTES:

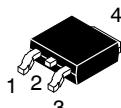
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2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

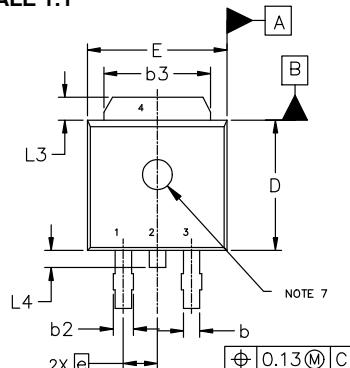
STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE	STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2
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DESCRIPTION:	DPAK INSERTION MOUNT	PAGE 1 OF 1

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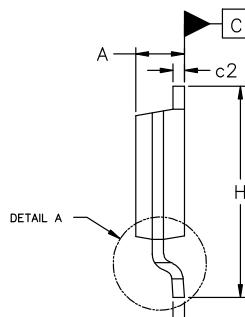
SCALE 1:1



TOP VIEW

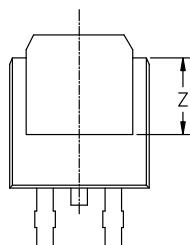
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE H

DATE 15 JUL 2025

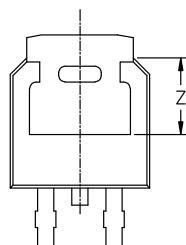
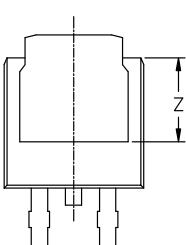
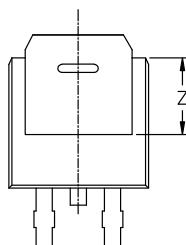
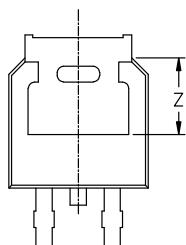


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29	BSC	
H	9.40	9.91	10.41
L	1.40	10.10	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



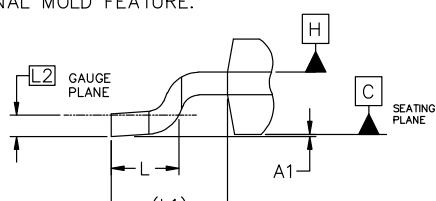
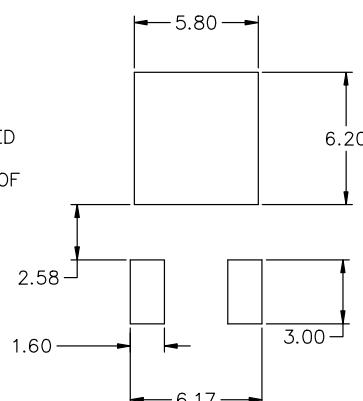
BOTTOM VIEW



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DETAIL A
ROTATED 90° CW

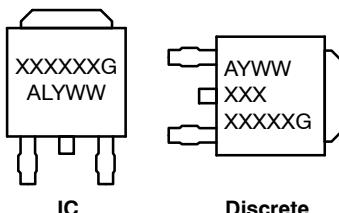
RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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