

TC74HC173AP, TC74HC173AF

Quad D-Type Register (3-state)

The TC74HC173A is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists a 4-bit register consisting of D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CK) and a common clear input (CLR).

Signals applied to the data inputs (D1~D4) are stored in the respective flip-flops on the positive going transition of CK when clock control inputs (G1, G2) are held low.

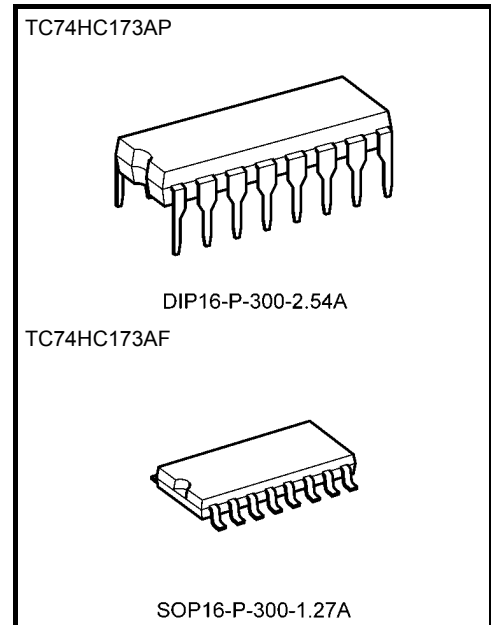
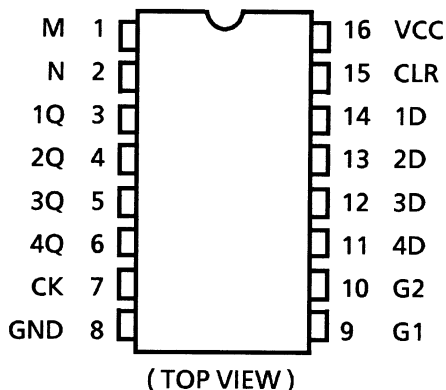
The clear function is asynchronous to CK and active on a high level. The stored data are enabled to each outputs when output control inputs (M, N) are held low, else the outputs are high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 47 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6 \text{ mA}$ (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (\text{opr}) = 2 \sim 6 \text{ V}$
- Pin and function compatible with 74LS173

Pin Assignment

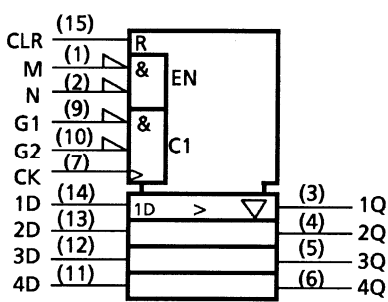


Weight

DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

IEC Logic Symbol



Truth Table

CLR	CK	Data Inable		Dn	Outputs Control		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L		X	X	X	L	L	Q0
L		H	X	X	L	L	Q0
L		X	H	X	L	L	Q0
L		L	L	H	L	L	H
L		L	L	L	L	L	L

X: Don't care

Z: High impedance

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	−0.5~7	V
DC input voltage	V _{IN}	−0.5~V _{CC} + 0.5	V
DC output voltage	V _{OUT}	−0.5~V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±35	mA
DC V _{CC} /ground current	I _{CC}	±75	mA
Power dissipation	P _D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T _{stg}	−65~150	°C

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of $-10\text{ mW}/^\circ\text{C}$ shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2~6	V
Input voltage	V_{IN}	0~ V_{CC}	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	t_r, t_f	0~1000 ($V_{CC} = 2.0$ V) 0~500 ($V_{CC} = 4.5$ V) 0~400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
High-level input voltage	VIH	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	V	
Low-level input voltage	VIL	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High-level output voltage	VOH	VIN = VIH or VIL	IOH = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			IOH = -6 mA	4.5	4.18	4.31	—	4.13	—	
IOH = -7.8 mA	6.0	5.68	5.80	—	5.63	—	—			
Low-level output voltage	VOL	VIN = VIH or VIL	IOL = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			IOL = 6 mA	4.5	—	0.17	0.26	—	0.33	
IOL = 7.8 mA	6.0	—	0.18	0.26	—	0.33	—			
3-state output off-state current	IOZ	VIN = VIH or VIL VOUT = VCC or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current	IIN	VIN = VCC or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	ICC	VIN = VCC or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	t_W (L) t_W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width (CLR)	t_W (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (G1, G2)	t_s	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (D)	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time (G1, G2, D)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time (CLR)	t_{rem}	—	2.0	—	5	5	ns
			4.5	—	5	5	
			6.0	—	5	5	
Clock frequency	f	—	2.0	—	9	7	ns
			4.5	—	43	34	
			6.0	—	51	40	

AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			CL (pF)	VCC (V)	Min	Typ.	Max	Min	Max	
Output transition time	tTLH tTHL	—	50	2.0 4.5 6.0	— — —	20 6 5	60 12 10	— — —	75 15 13	ns
Propagation delay time (CK-Q)	tPLH tPHL	—	50	2.0	—	50	115	—	145	ns
				4.5	—	15	23	—	29	
				6.0	—	12	20	—	25	
			150	2.0	—	65	155	—	195	
				4.5	—	20	31	—	39	
				6.0	—	16	26	—	33	
Propagation delay time (CLR-Q)	tPHL	—	50	2.0	—	50	115	—	145	ns
				4.5	—	15	23	—	29	
				6.0	—	12	20	—	25	
			150	2.0	—	63	155	—	195	
				4.5	—	20	31	—	39	
				6.0	—	16	26	—	33	
Output enable time	tPZL tPZH	RL = 1 kΩ	50	2.0	—	50	115	—	145	ns
				4.5	—	15	23	—	29	
				6.0	—	12	20	—	25	
			150	2.0	—	63	115	—	195	
				4.5	—	20	31	—	39	
				6.0	—	16	26	—	33	
Output disable time	tPLZ tPHZ	RL = 1 kΩ	50	2.0	—	36	135	—	170	ns
				4.5	—	17	27	—	34	
				6.0	—	15	23	—	29	
Maximum clock frequency	fmax	—	50	2.0	9	20	—	7	—	MHz
				4.5	43	67	—	34	—	
				6.0	51	84	—	40	—	
Input capacitance	CIN	—			—	5	10	—	10	pF
Output capacitance	COUT	—			—	10	—	—	—	pF
Power dissipation capacitance	CPD (Note)	—			—	45	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/4 \text{ (per flip flop)}$$

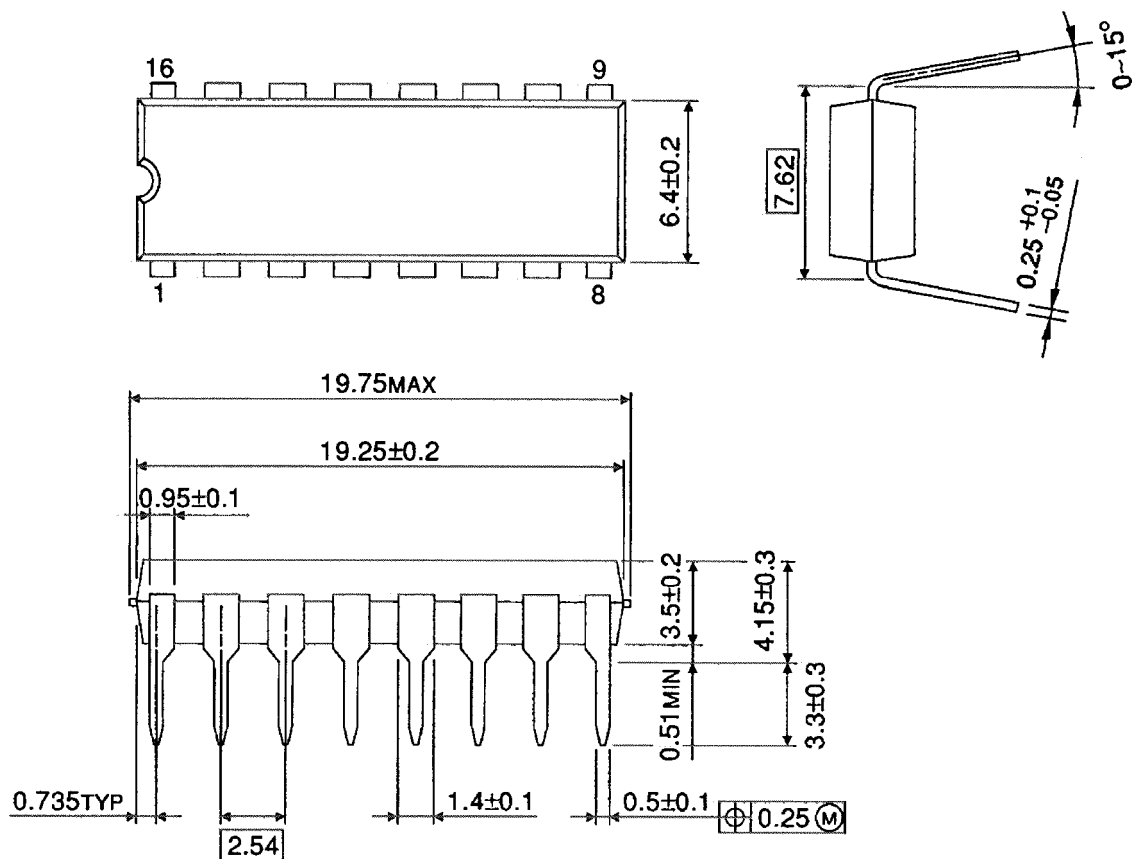
And the total C_{PD} when n pcs of flip flop operate be gained by the following equation:

$$C_{\text{PD (total)}} = 28 + 17 \cdot n$$

Package Dimensions

DIP16-P-300-2.54A

Unit : mm

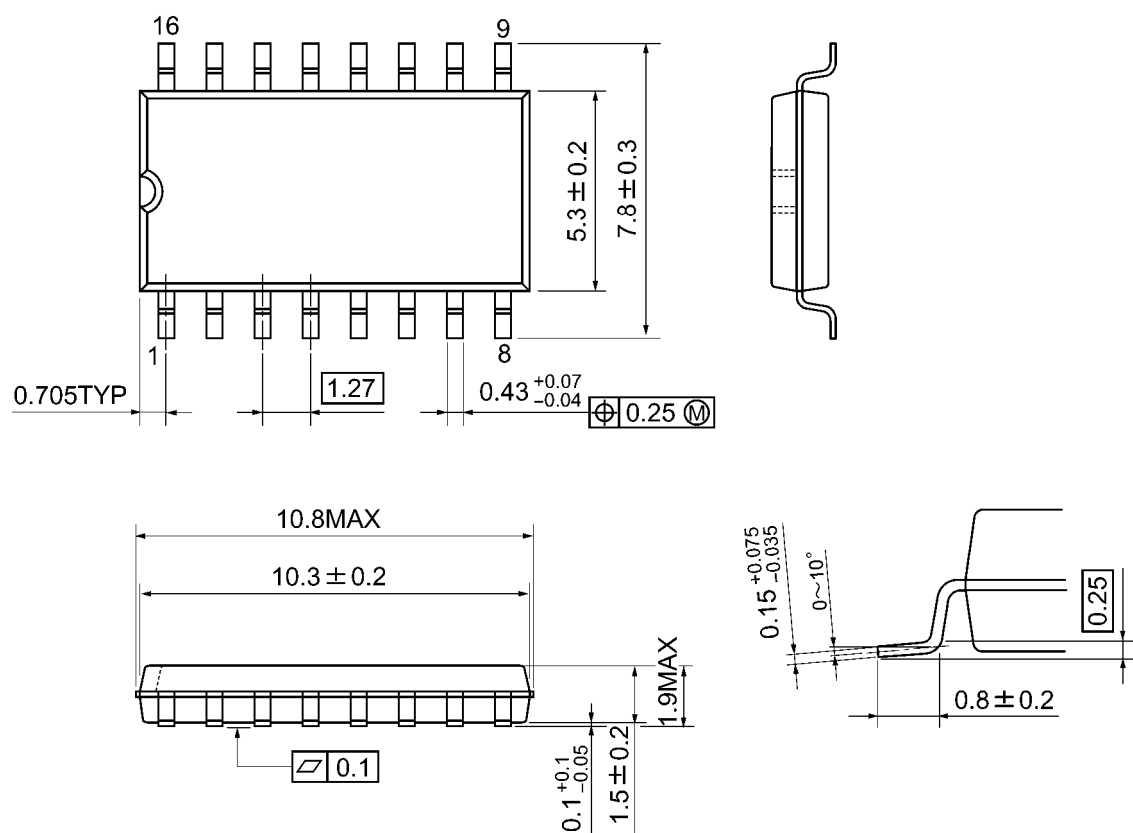


Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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