

# PH1225AL

## N-channel 25 V 1.2 mΩ logic level MOSFET in LFPAK

Rev. 01 — 14 October 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in LFPAK package qualified to 150 °C. This product is for computing use only

### 1.2 Features and benefits

- Advanced TrenchMOS provides low  $R_{DSon}$  and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- For computing use only

### 1.4 Quick reference data

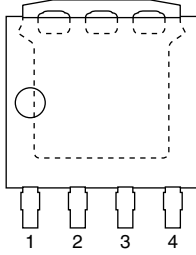
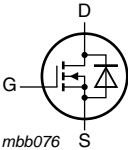
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	[1]	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	121	W
$T_j$	junction temperature		-55	-	150	°C
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	-	677	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ;	-	11.9	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 12\text{ V}$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	50.6	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 100\text{ °C}$ ; see <a href="#">Figure 11</a>	-	-	1.6	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 10</a>	-	0.9	1.2	mΩ

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	drain		
			<b>SOT1023 (LPAK2)</b>	

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
PH1225AL	LPAK2	Plastic single-ended surface-mounted package (LPAK2); 4 leads	SOT1023

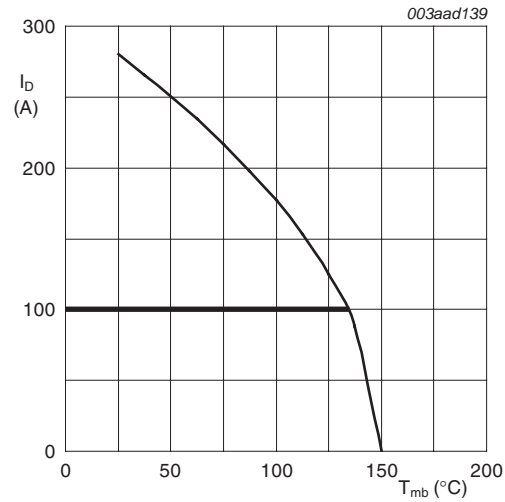
## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

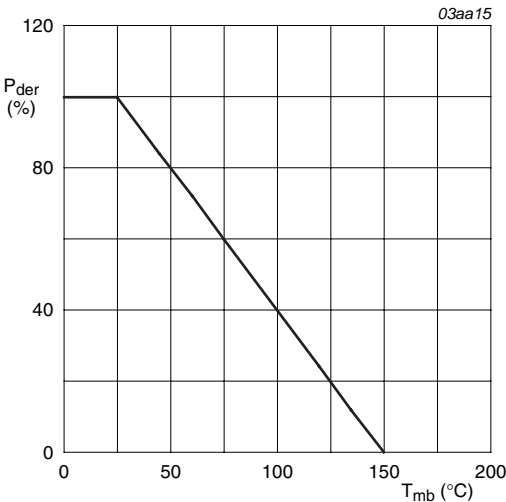
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	100	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	100	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	815	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	121	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$ ; <sup>[1]</sup>	-	100	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	815	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(initial)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	677	mJ

[1] Continuous current is limited by package.



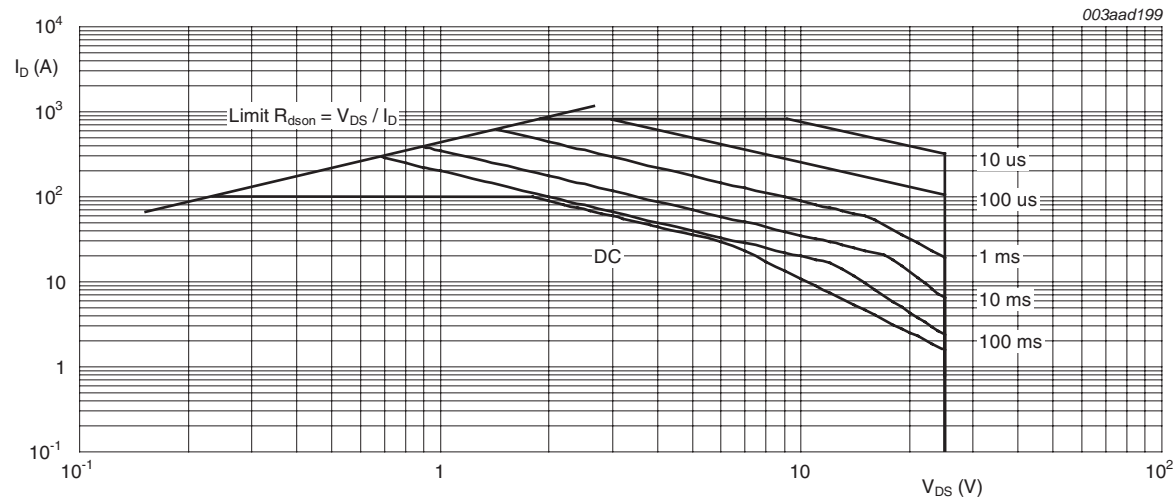
$V_{GS} \geq 5V(1)$  Capped at 100A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse Capped at 100A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.4	1	K/W

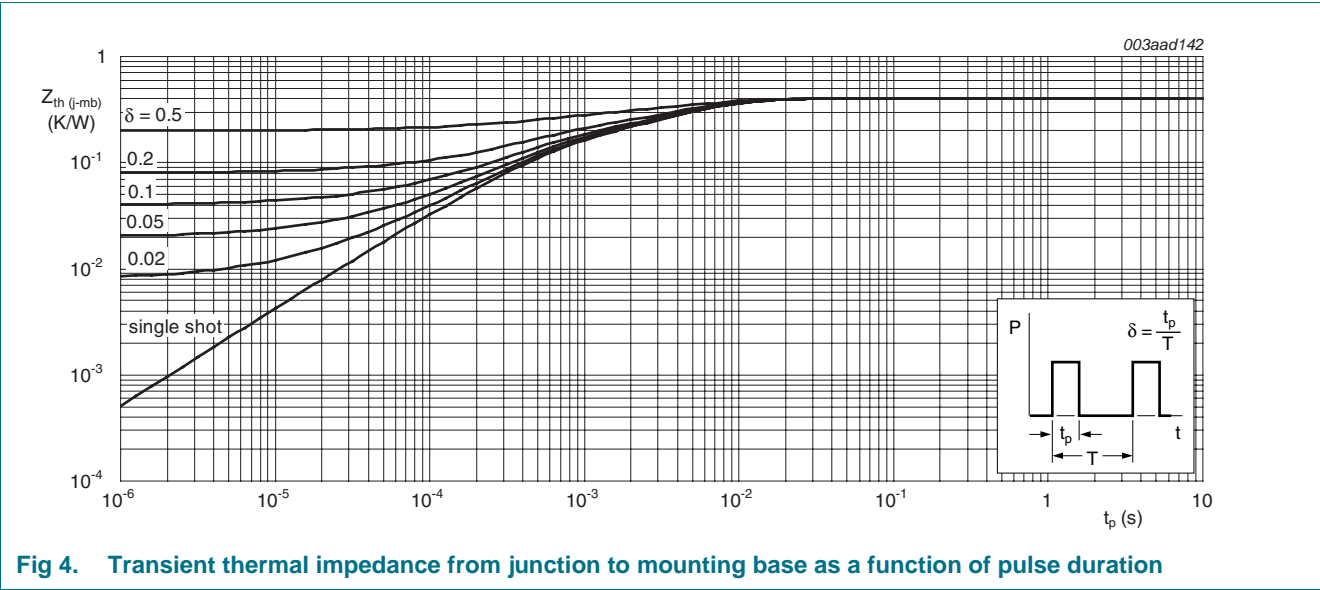


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	25	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = -55 ^\circ C$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 8</a> and <a href="#">9</a>	1.3	1.7	2.15	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 ^\circ C$ ; see <a href="#">Figure 9</a>	0.65	-	-	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 ^\circ C$ ; see <a href="#">Figure 9</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	1.5	$\mu A$
		$V_{DS} = 25 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 ^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 15 A$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 10</a>	-	1.2	1.85	mΩ
		$V_{GS} = 10 V$ ; $I_D = 15 A$ ; $T_j = 100 ^\circ C$ ; see <a href="#">Figure 11</a>	-	-	1.6	mΩ
		$V_{GS} = 10 V$ ; $I_D = 15 A$ ; $T_j = 150 ^\circ C$ ; see <a href="#">Figure 11</a>	-	-	2.1	mΩ
		$V_{GS} = 10 V$ ; $I_D = 15 A$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 10</a>	-	0.9	1.2	mΩ
$R_G$	gate resistance		-	0.94	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$ ; $V_{DS} = 12 V$ ; $V_{GS} = 10 V$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	105	-	nC
		$I_D = 25 A$ ; $V_{DS} = 12 V$ ; $V_{GS} = 4.5 V$ ; see <a href="#">Figure 12</a> and <a href="#">13</a>	-	50.6	-	nC
$Q_{GS}$	gate-source charge		-	19.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	8.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.5	-	nC
$Q_{GD}$	gate-drain charge		-	11.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 V$ ; see <a href="#">Figure 12</a>	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 12 V$ ; $V_{GS} = 0 V$ ; $f = 1 MHz$ ; $T_j = 25 ^\circ C$ ; see <a href="#">Figure 14</a>	-	6380	-	pF
$C_{oss}$	output capacitance		-	1640	-	pF
$C_{rss}$	reverse transfer capacitance		-	644	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12 V$ ; $R_L = 0.5 \Omega$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 5.6 \Omega$	-	69	-	ns
$t_r$	rise time		-	125	-	ns
$t_{d(off)}$	turn-off delay time		-	94	-	ns
$t_f$	fall time		-	56	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 15</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	52	-	ns
$Q_r$	recovered charge	$V_{DS} = 20\text{ V}$	-	66	-	nC

[1] Tested to JEDEC standards where applicable.

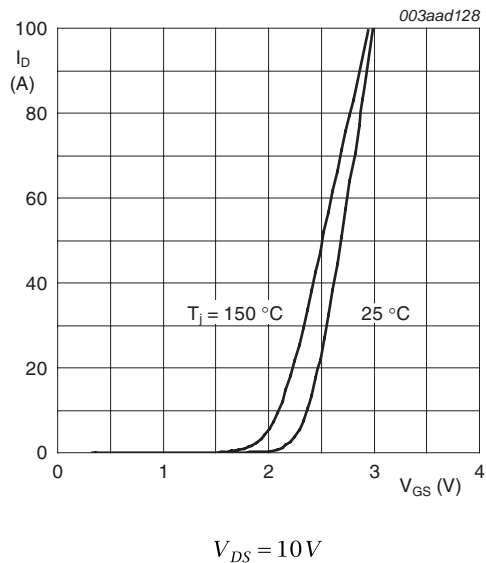


Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values

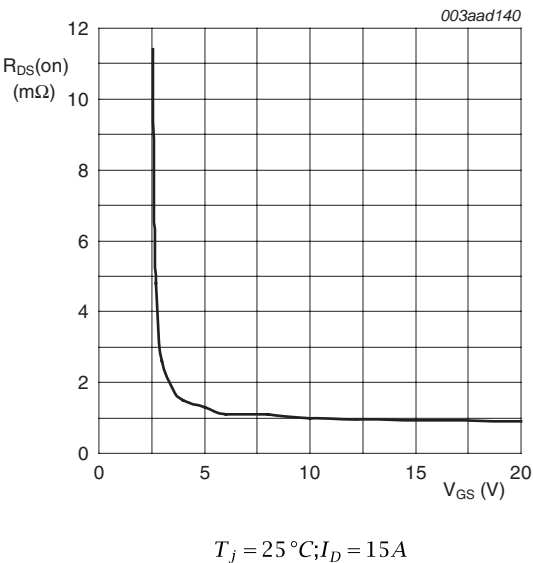


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

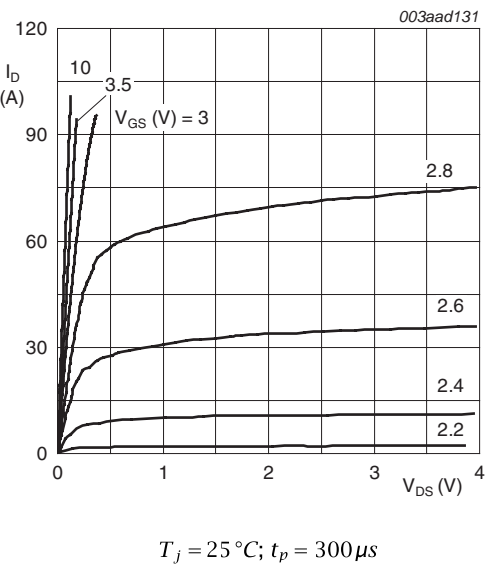


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

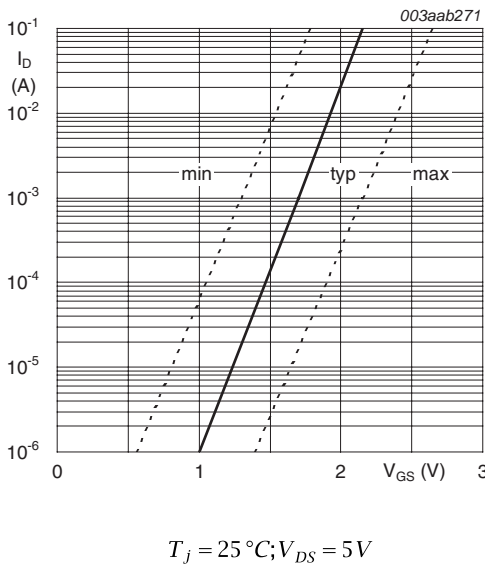
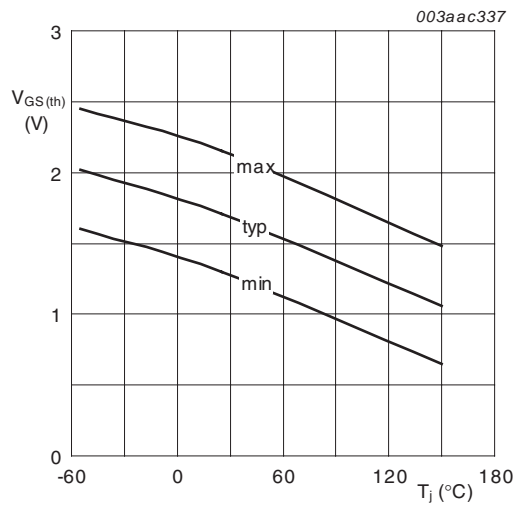
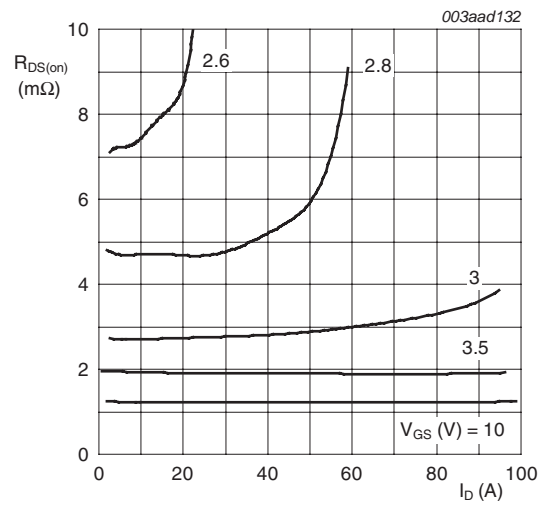


Fig 8. Sub-threshold drain current as a function of gate-source voltage



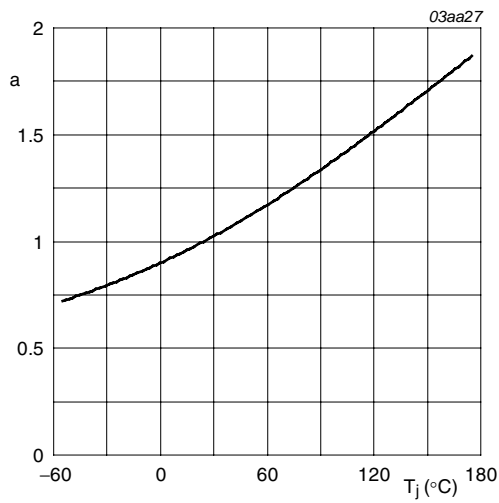
$$I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

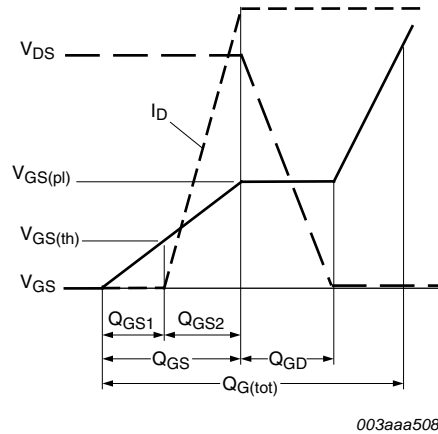
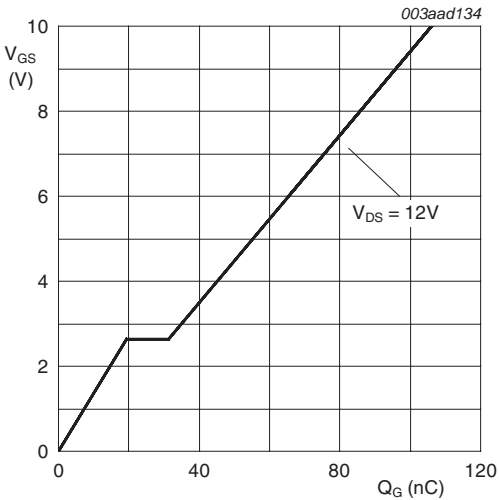
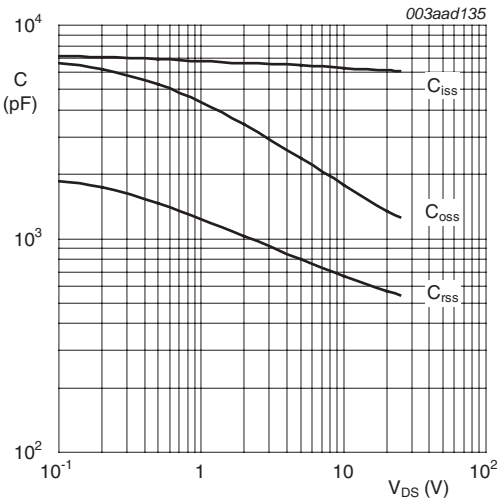


Fig 12. Gate charge waveform definitions



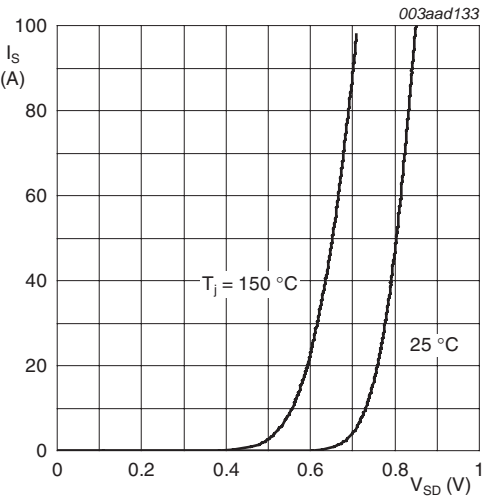
$T_j = 25\text{ }^{\circ}\text{C}; I_D = 10\text{ A}$

Fig 13. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



7. Package outline

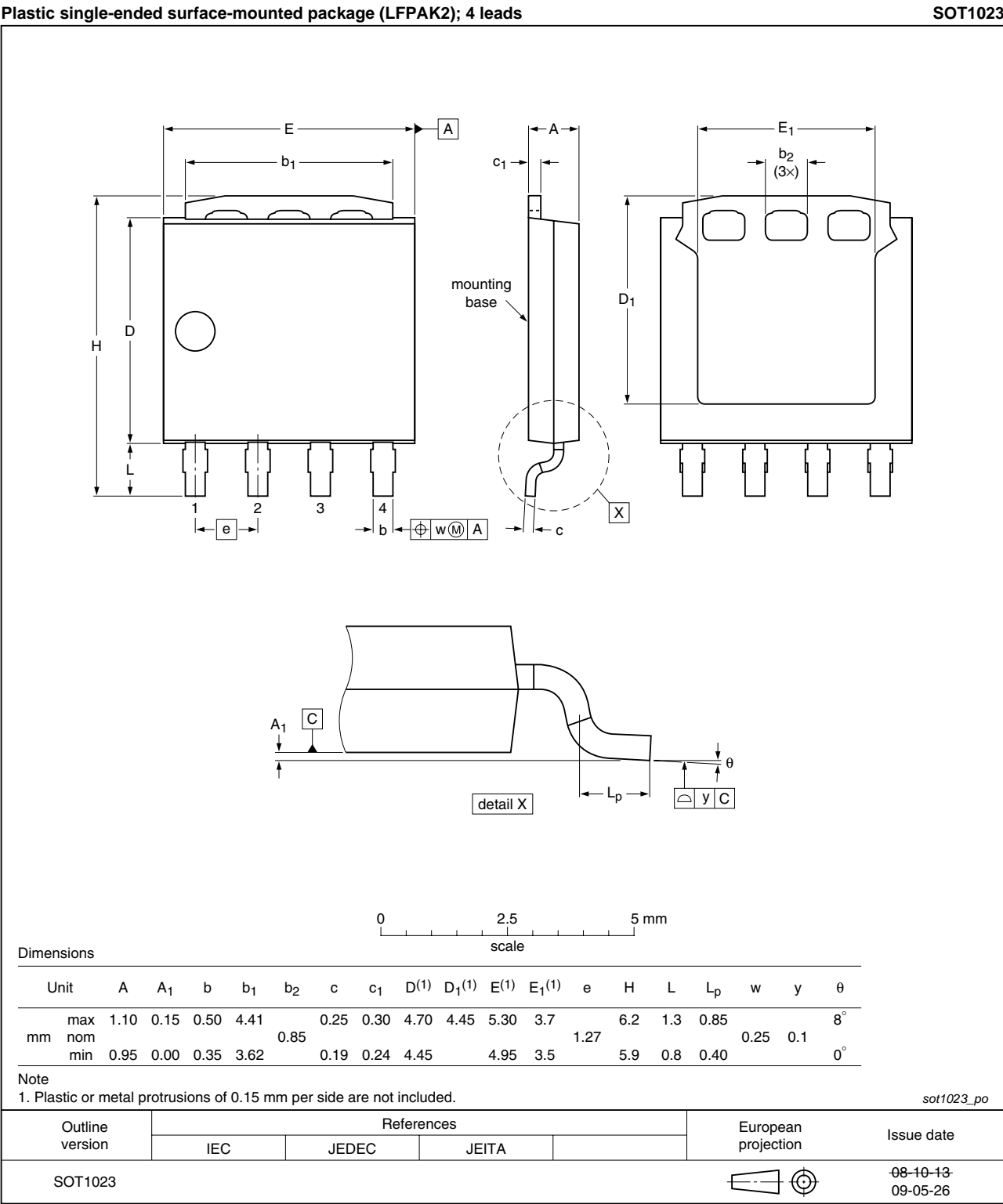


Fig 16. Package outline SOT1023 (LPAK2)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH1225AL_1	20091014	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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