MP28200

Ultra-Low 500nA I_q, High Efficiency, Wide Input 2V-5.5V, 1.5MHz, 200mA, Step-Down Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP28200 is a monolithic power-management unit containing 200mA, high-efficiency, step-down, switching converters. The nanoamp quiescent current provides extremely high efficiency when the load current is down in the µA range. With minimum input voltage as low as 2V, the MP28200 allows the system to operate directly from the battery.

The constant-on-time control scheme provides fast transient response, high light-load efficiency, and requires minimal capacitance. The regulation can be made tight by integrating an error amplifier to correct the output voltage.

The CTRL pins control the on/off and output voltage selection functions.

Fault protection features include under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown.

The MP28200 requires a minimal number of readily available, standard, external components and is available in a small QFN-12 (2mmx2mm) package.

FEATURES

- Ultra-Low I_q: 500nA
- Wide 2.0V to 5.5V Operating Input Range
- 7 Selectable Output Voltages
- Up to 200mA Output Current
- 1.5MHz Switching Frequency in Continuous Conduction Mode (CCM)
- 100% Duty Cycle in Dropout
- 0.25Ω and 0.25Ω Internal Power MOSFET Switches
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Protection (OTP)
- Available in a QFN-12 (2mmx2mm) Package

APPLICATIONS

- Wearables
- IOT
- Portable Instruments
- Battery-Powered Devices

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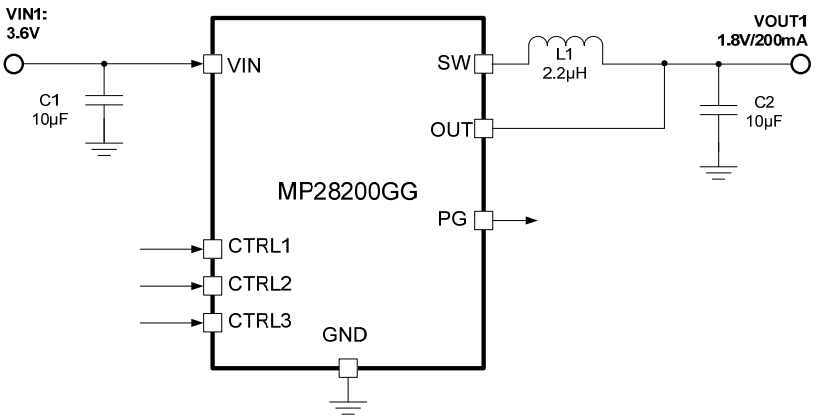
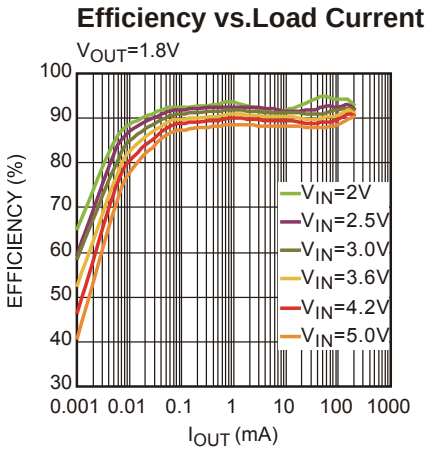
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP28200GG	QFN-12 (2mmx2mm)	*See Below*

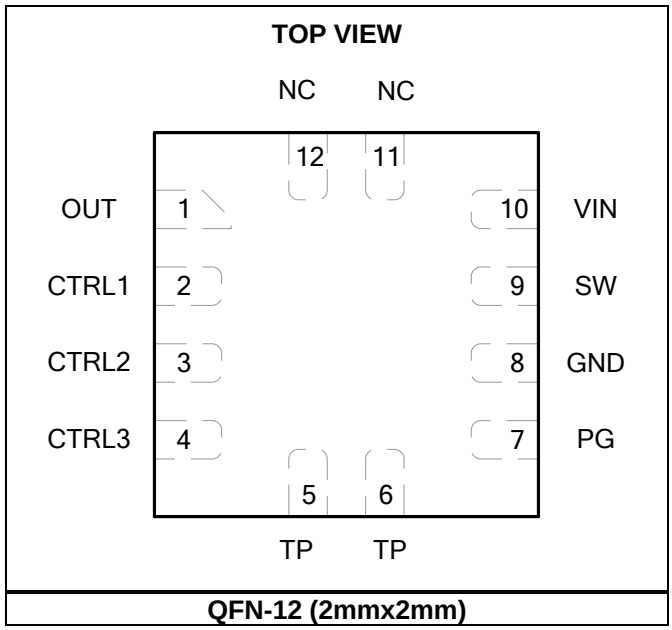
* For Tape & Reel, add suffix –Z (e.g. MP28200GG–Z)

TOP MARKING

FBY
LLL

FB: Product code of MP28200GG
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx2mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 6V
V_{SW} .....
-0.3V (-5V for <10ns) to
6V (8V for <10ns or 10V for <3ns)
All other pins .....-0.3V to 6V
Continuous power dissipation (T_A = +25°C)
.....1.6W (2)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN) .....2.0V to 5.5V
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mmx2mm)	80	16	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input voltage range (5)	V_{IN}		2.0		5.5	V
Under-voltage lockout threshold rising	$V_{IN\_UVLO\_R}$		1.65	1.8	1.95	V
Under-voltage lockout threshold hysteresis	$V_{IN\_UVLO\_H}$			150		mV
Supply current (shutdown)	$I_{SD\ 25}$	CTRL1/2/3 = 0V, or EN = 0		70		nA
Supply current (quiescent)	I_{Q_BUCK}	No load, CTRL4/5 = 0V, CTRL1/2/3 = H/L/H, OUT = 1.8V, not switching		500		nA
High-side switch on resistance	$R_{DSON\ H}$			0.25		Ω
Low-side switch on resistance	$R_{DSON\ L}$			0.25		Ω
Switch leakage current	I_{LK_SW}	CTRL1/2/3 = 0V, V_{IN} = 5.5V, V_{SW} = 0V and 5.5V, T_J = 25°C	-100	0	100	nA
High-side current limit	$I_{LIM\ H}$		430	550		mA
Low-side switch valley current (sourcing)	I_{LIMV_L}		250	350		mA
Low-side switch zero crossing current	I_{ZCD}		0	20		mA
On time	T_{ON}	V_{IN} = 3.6V, V_{OUT} = 1.8V	280	330	380	ns
Minimum on time	$T_{MIN\ ON}$			60		ns
Minimum off time	$T_{MIN\ OFF}$			100		ns
Maximum duty cycle (5)	D_{MAX}			100		%
Output voltage accuracy	V_{OUT}	CTRL1/2/3 = H/L/H, T_J = 25°C, I_{OUT} = 0.1A	1.782	1.800	1.818	V
		CTRL1/2/3 = H/L/H, T_J = -40°C to 85°C, I_{OUT} = 0.1A	1.773		1.827	
Line/load regulation (6)		From 2.5V to 5.5V, from 0A to 200mA	-1		1	%
Internal soft-start time	T_{SS}			0.5		ms
Discharge resistance during enable off	R_{DIS_OFF}			50		Ω
CTRL high logic	$CTRL_H$		1.2			V
CTRL low logic	$CTRL_L$				0.4	V
CTRL input current	I_{CTRL}	V_{CTRL} = 3.6V		1		nA
		V_{CTRL} = 0V		0		
		V_{EN} = 0V		0		
CTRL turn-on delay	T_D			300		µs
CTRL pull-down resistor	R_{PD}	Not present when CTRL is high to avoid I_Q impact		2		MΩ
Power good threshold	PG	FB with respect to the regulation		90		%

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ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 3.6V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power good hysteresis	PG_{Hys}			10		%
Power good delay	PG_{TD}			75		µs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good leakage current	I_{PGLK}	V_{PGBUS} = 1.8V			10	nA
Thermal shutdown (5)	T_{SD}			150		°C
Thermal hysteresis (5)	T_{SDHY}			30		°C

NOTES:

5) Guaranteed by design.
6) Application test.

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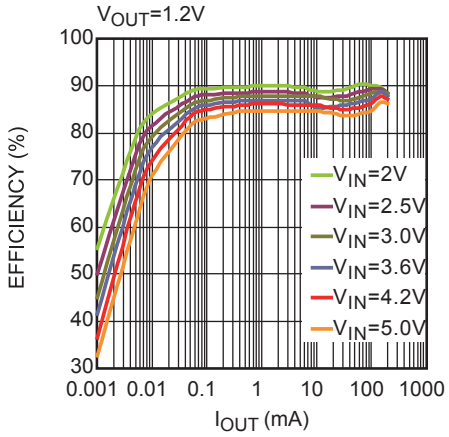
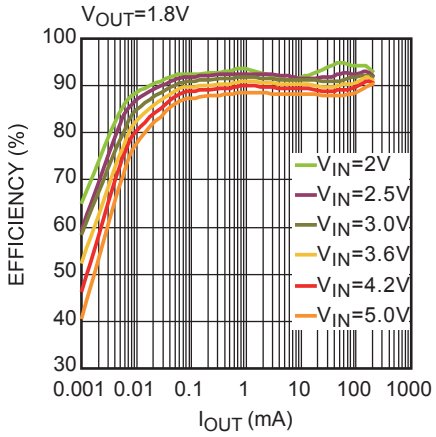
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = +25°C, unless otherwise noted.

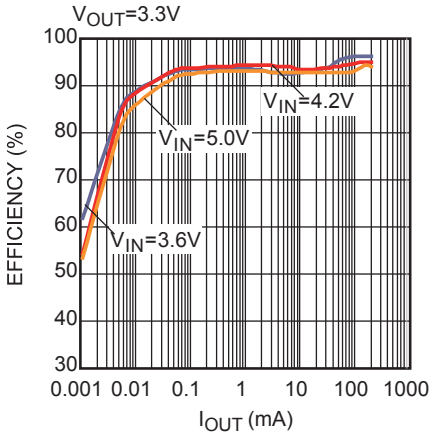
Efficiency vs.Load Current



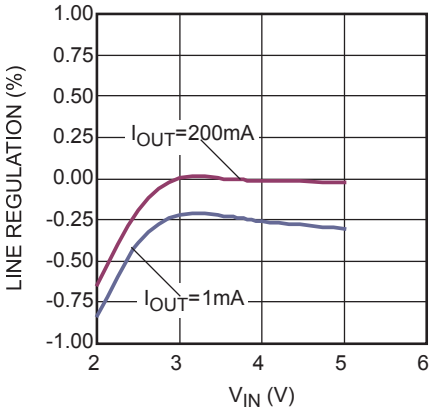
Efficiency vs.Load Current



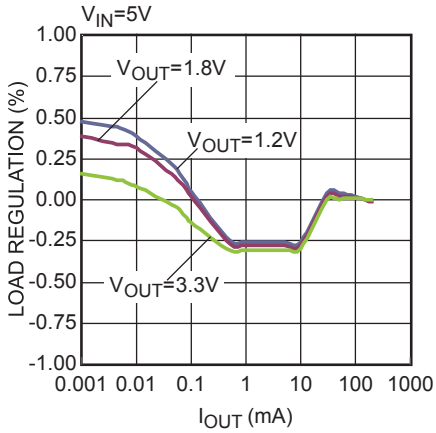
Efficiency vs.Load Current



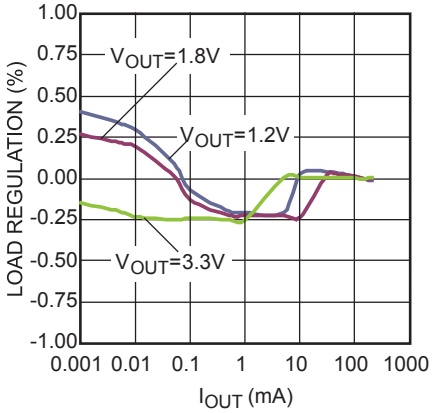
Line Regulation vs. Load Current



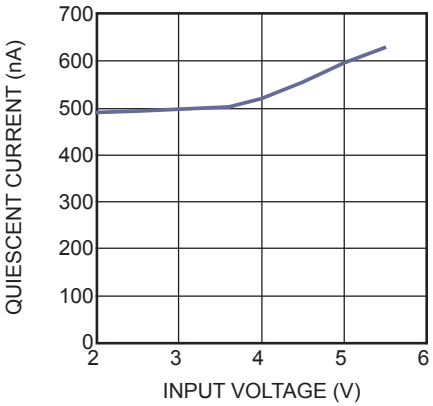
Load Regulation vs. Load Current



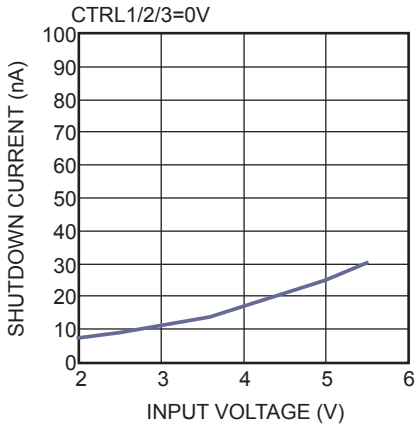
Load Regulation vs. Load Current



Buck Quiescent Current vs. Input Voltage



Buck Shutdown Current vs. Input Voltage



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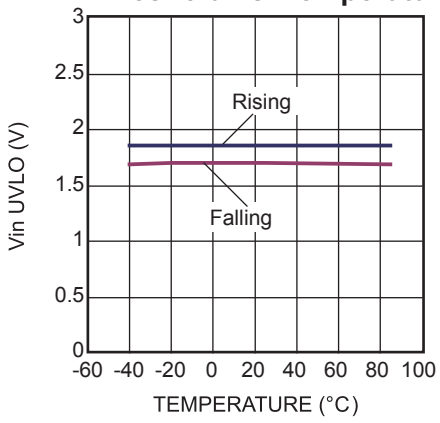
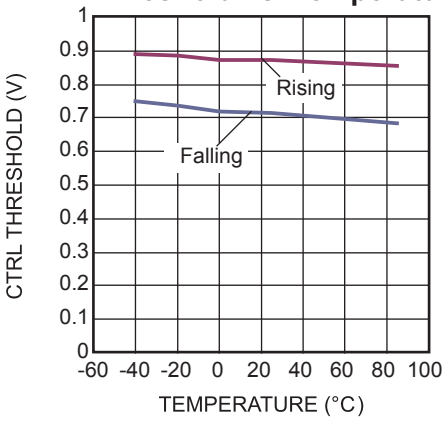
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = +25°C, unless otherwise noted.

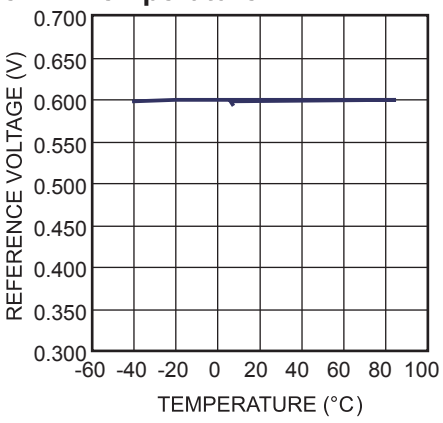
Buck VIN UVLO Rising Threshold vs. Temperature



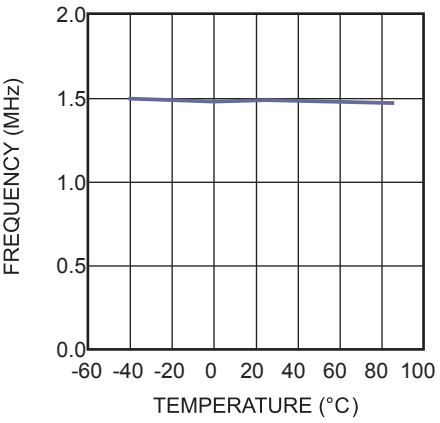
CTRL Rising and Falling Threshold vs. Temperature



Reference Voltage vs. Temperature

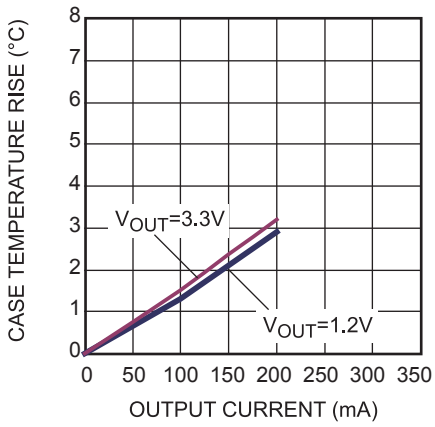


Frequency vs. Temperature



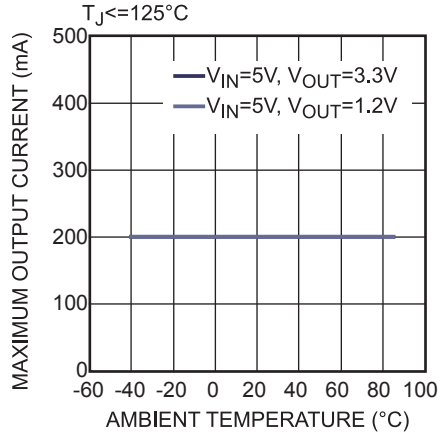
T_{RISING} vs. Output Current

V_{IN}=5V



Output Current Derating vs. Ambient Temperature

T_J<=125°C



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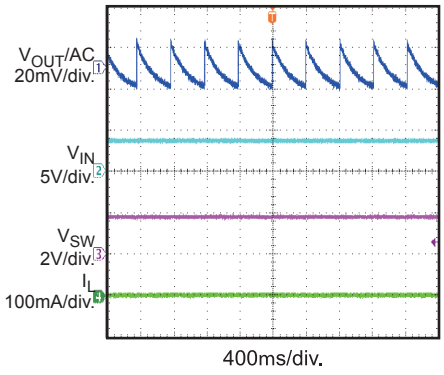
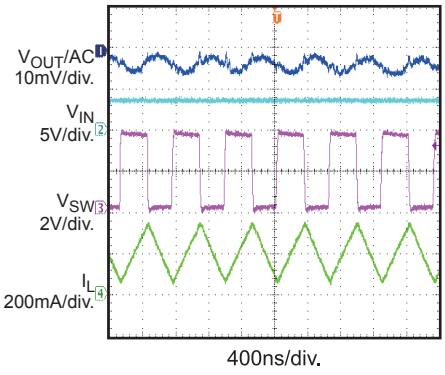
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = +25°C, unless otherwise noted.

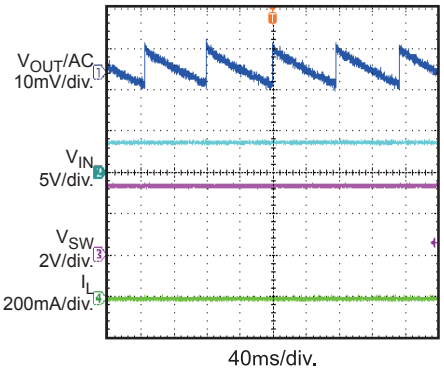
Steady State
I_{OUT} = 0A



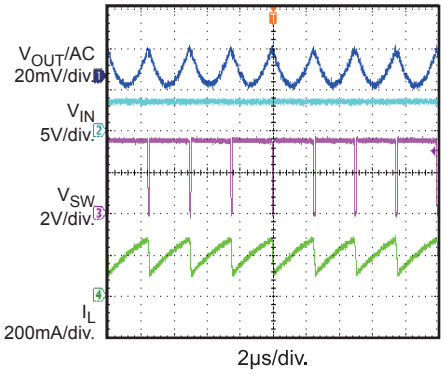
Steady State
I_{OUT} = 0.2A



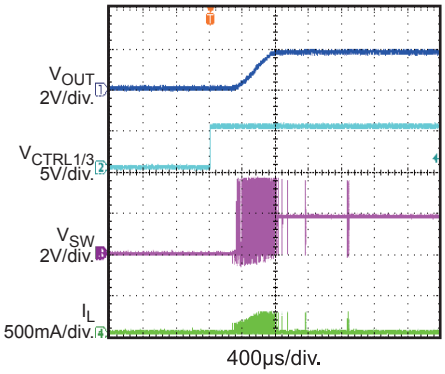
Steady State
V_{OUT} = 3.3V, I_{OUT} = 0A



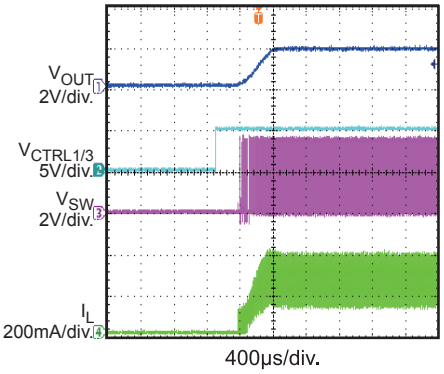
Steady State
V_{OUT} = 3.3V, I_{OUT} = 0.2A



CTRL On
I_{OUT} = 0A



CTRL On
I_{OUT} = 0.2A



CTRL Off
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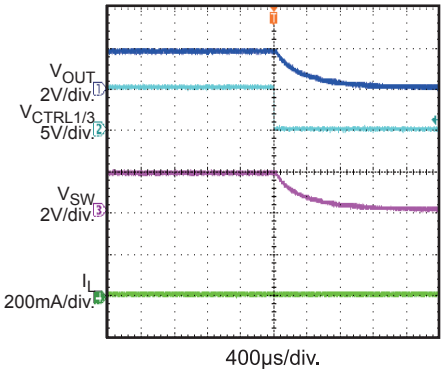

CTRL Off
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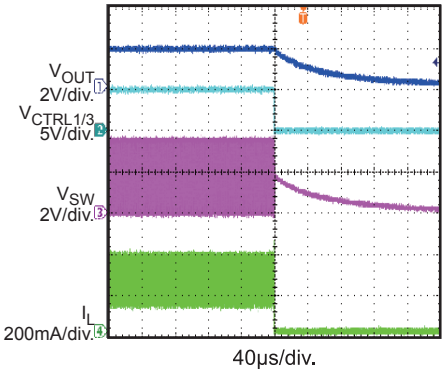

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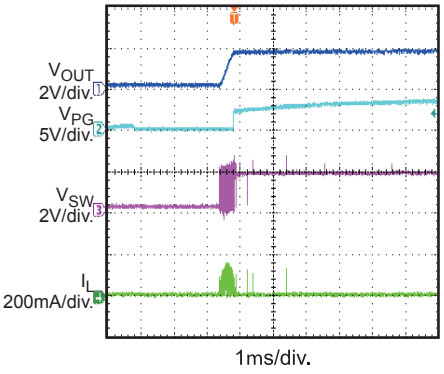

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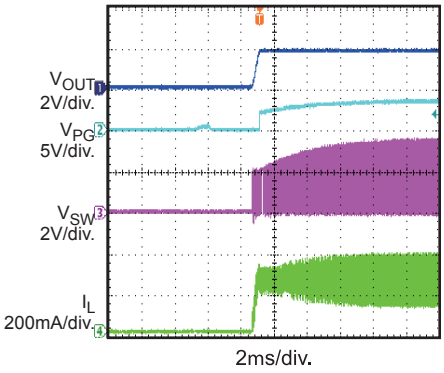
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 3.6V, V_{OUT} = 1.8V, L_1 = 2.2µH, C_{IN} = 10µF, C_{OUT} = 10µF, T_A = +25°C, unless otherwise noted.

PG On
I_{OUT} = 0.2A



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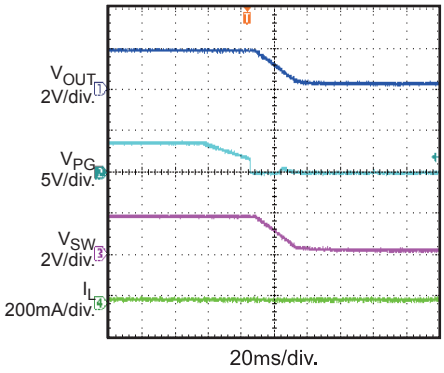

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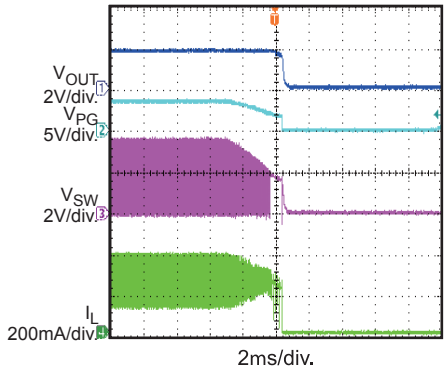
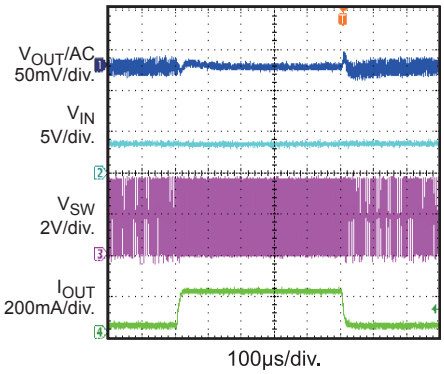
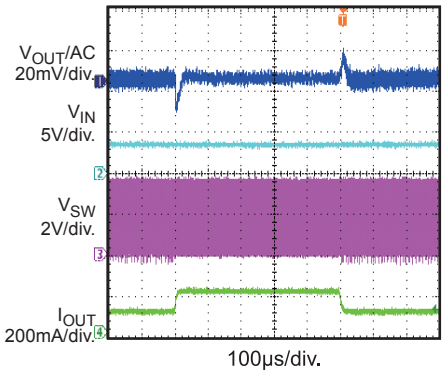


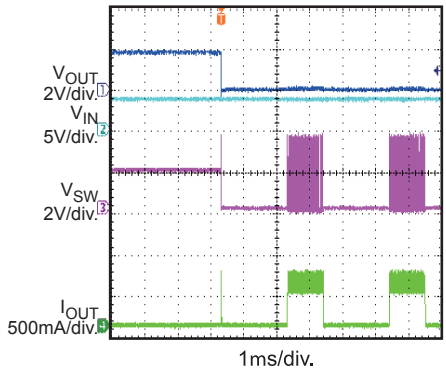
Load Transient
I_{OUT} = 30-200mA, 0.25A/µs



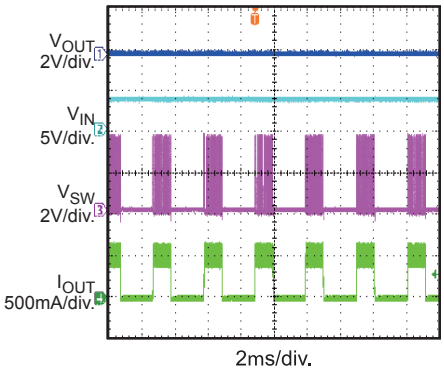
Load Transient
I_{OUT} = 100-200mA, 0.25A/µs



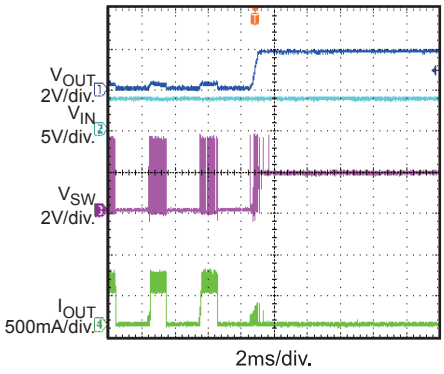
Short-Circuit Entry



Short-Circuit Steady



Short-Circuit Recovery



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PIN FUNCTIONS

Pin#	Name	Description
1	OUT	**Output voltage sensing of the step-down switcher.** Connect the load to OUT. An output capacitor is needed to decrease the output voltage ripple.
2	CTRL1	**Step-down switcher control signal.** Adjust the step-down switcher output voltage value dynamically. Do not float the CTRL pins during application. When used, ensure that the CTRL voltage is not lower than VIN. If unused, tie CTRL to GND. Refer to Table 1 on page 12 to set the buck output value.
3	CTRL2	
4	CTRL3	
5, 6	TP	**Internal test pin.** TP must be connected to GND.
7	PG	**Power good for the step-down switcher.** PG is an open-drain output.
8	GND	**Ground.**
9	SW	**Switch output for the step-down switcher.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
10	VIN	**Input supply voltage to the step-down switcher.** Place a small decoupling capacitor as close to VIN and GND as possible.
11, 12	NC	**Internal test pin.** NC must be left floating.

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BLOCK DIAGRAM

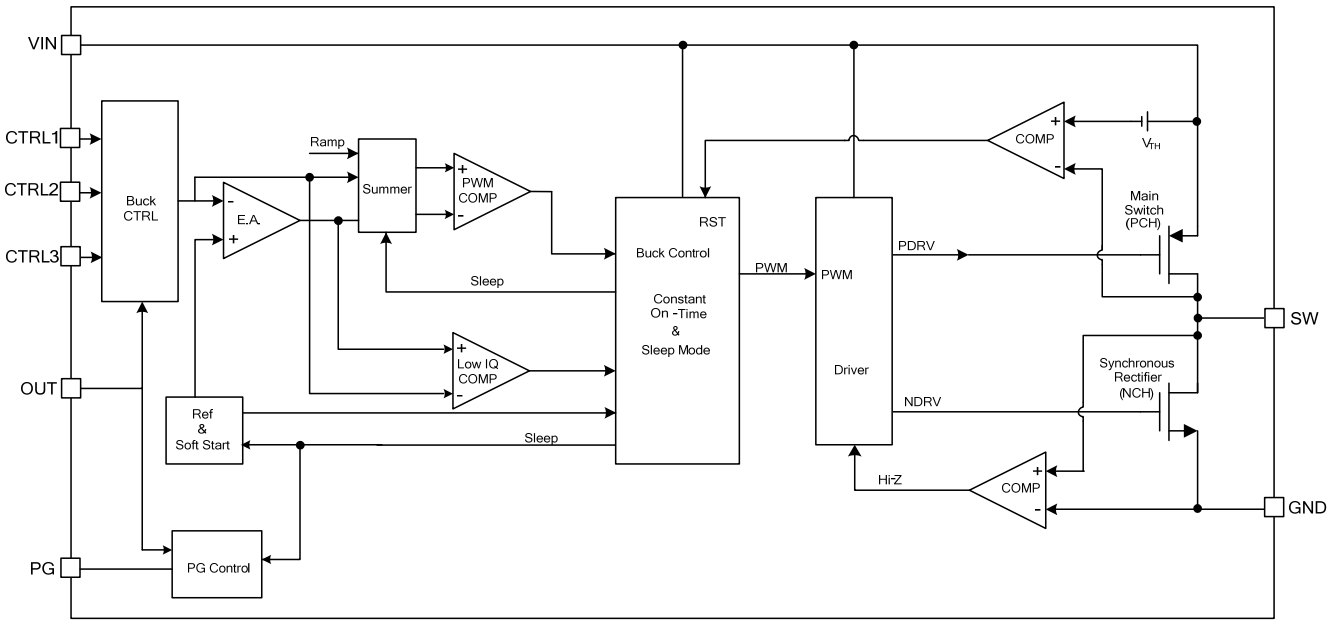

Figure 1: Functional Block Diagram

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OPERATION

The MP28200 has an ultra-low, quiescent current, step-down converter and low-dropout regulator. The step-down converter has 500nA of I_Q current, allowing the MP28200 to achieve extremely high efficiency at an ultra-low load current.

Constant-On-Time Control of the Buck

The MP28200 uses a constant-on-time control scheme to implement output voltage regulation. The one-shot on-timer is controlled by the input and output voltage conditions. At different input and output voltage conditions, the switching frequency is fairly the same stable, which helps with system design. The switching frequency is around 1.5MHz, typically.

With constant-on-time control, the output ripple is small, and the load transient response is fast. Constant-on-time control minimizes the need for input and output capacitors.

The MP28200 enters pulse-skip mode automatically when the low-side switch current reaches the zero ampere threshold. Pulse-skip mode helps improve light-load efficiency. The constant-on-time scheme provides a seamless transition from pulse-width modulation (PWM) mode to pulse-frequency modulation (PFM) mode and vice versa.

Light-Load Operation

When the load current decreases and the low-side switch current reaches the zero ampere threshold, both the high-side and low-side switches are turned off. Output energy is provided by the output capacitors during this period until the output voltage drops, reaches the regulation voltage, and triggers another on pulse.

Generally, the switching frequency in PFM mode depends on the load current. The switching frequency is lower when the load current is lighter. With PFM control at light-load mode plus the ultra-low quiescent operation current, the MP28200 can achieve the highest efficiency at an extremely low load. This helps extend the charge cycle of any battery-powered system.

When the buck works in light-load operation, it needs at least 5μs to exit light load. When a large, quick, and sharp load increase occurs in light-load mode, the output voltage drops during the exit transition.

Control (CTRL)

CTRL1/2/3 are used to control start-up and set the output voltages of the step-down regulator. When CTRL1/2/3 are low, the step-down switcher of the MP28200 is disabled. Once either one of CTRL1/2/3 are pulled high, the switcher is enabled. The output voltage is set depending on which CTRL pin is pulled high. The output voltage is programmable according to Table 1.

Table 1: CTRL vs. Output Voltages

CTRL3	CTRL2	CTRL1	OUT
0	0	0	Disabled
0	0	1	0.8V
0	1	0	1.0V
0	1	1	1.2V
1	0	0	1.5V
1	0	1	1.8V
1	1	0	2.5V
1	1	1	3.3V

The output voltage can be programmable during operation and supports dynamic output voltage scaling. CTRL cannot be floating. Any used CTRL voltage cannot be less than VIN, and any unused CTRL pin must be tied to GND.

Soft Start (SS)

When the converter is enabled, the internal reference is powered up. After a certain delay time, the device enters soft start (SS). The step-down switcher output voltage ramps up to the regulation voltage in about 0.5ms.

Power Good (PG) Indicators of the Buck

The MP28200 has an open-drain output power good (PG) indicator with a maximum $R_{DS(ON)}$ of less than 400Ω. PG requires an external pull-up resistor (100kΩ~500kΩ) for the power good indicator. This resistor can be pulled up to VIN or tied to CTRL if the CTRL voltages do not need to be adjusted dynamically.

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The PG comparator is active when the device is enabled. It is driven to a high impedance once the output voltage trips the PG threshold (90% of the regulation voltage, typically) and is pulled low once the output voltage falls below the PG hysteresis threshold (80% of the regulation voltage, typically). The output is also pulled low when the input voltage is lost or the part is disabled.

Output Discharge Function

The step-down regulator features the output discharge function once it is disabled. This feature prevents residual charge voltages on capacitors, which may impact a proper power-up of the system. When the input voltage is high and the related converters are disabled, the output discharge is active.

100% Duty Cycle Mode

When the input voltage reduces and is lower than the regulation output voltage, the output voltage drops, and the on time increases. Further reducing the input voltage drives the MP28200 into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the loading current times the $R_{DS(ON)}$ composed by the high-side switch and inductor.

Current Limit

The MP28200 has an internal current limit for the step-down converter.

The high-side switch current is monitored cycle-by-cycle and compares with the current-limit threshold. Once the current-limit comparator is triggered, the high-side switch is turned off and the low-side switch is turned on, reducing the inductor current. Until the low-side switch current is lower than the low-side current limit, the high-side switch is not allowed to turn on again.

Short Circuit and Recovery

If the output voltage of the buck converter is shorted to GND, the current limit is triggered. If the current limit is triggered every cycle for 200μs continuously, the MP28200 enters hiccup mode for the buck converter. The short-circuit condition can also be triggered when the output voltage is lower than 50% of the regulation output voltage and when the current limit is reached simultaneously. The buck disables the output power stage, discharges the output voltage, and then attempts to recover after a hiccup. If the short-circuit condition remains, the MP28200 repeats this operation until the short-circuit is removed and the output rises back to regulation levels.

Thermal Shutdown Circuit and Recovery

When the thermal shutdown signal is triggered, the MP28200 turns off and restarts when the temperature falls below the thermal hysteresis.

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APPLICATION INFORMATION

Inductor Selection

Most applications work best with a 1µH to 2.2µH inductor. Select an inductor with a DC resistance less than 200mΩ to optimize efficiency.

High-frequency, switch-mode power supplies with a magnetic device have strong electronic magnetic inference for the system. Any unshielded power inductor should be avoided since it has poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended for the application since they can decrease influence effectively. Table 2 lists some recommended inductors.

Table 2: Recommended Inductors

Inductance	Manufacturer P/N	Package	Manufacturer
2.2µH	DFE201612P-2R2M	2016	Tokyo
2.2µH	74479775222A	2012	Wurth

For most designs, the inductance value can be calculated with Equation (1):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (1)$$

Where ΔI_L is the inductor ripple current. Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (2):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (2)$$

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with a switching frequency impedance less than the input source impedance to prevent high-frequency switching current from passing to the input source. Use low ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

The input capacitor requires an adequate ripple current rating since it absorbs the input switching current.

Estimate the RMS current in the input capacitor with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case scenario occurs at VIN = $2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Output Capacitor Selection

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. For most applications, a 10µF capacitor is sufficient. Estimate the V_{OUT} ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

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PCB Layout Guidelines

Efficient PCB layout of the switching power supply and especially the high-switching frequency converter is critical for stable operation. If the layout is not carefully done, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 2 and follow the guidelines below.

1. Place the input capacitor as close to the IC pins as possible for the high-speed step-down regulator to provide clean control voltage for the chip.

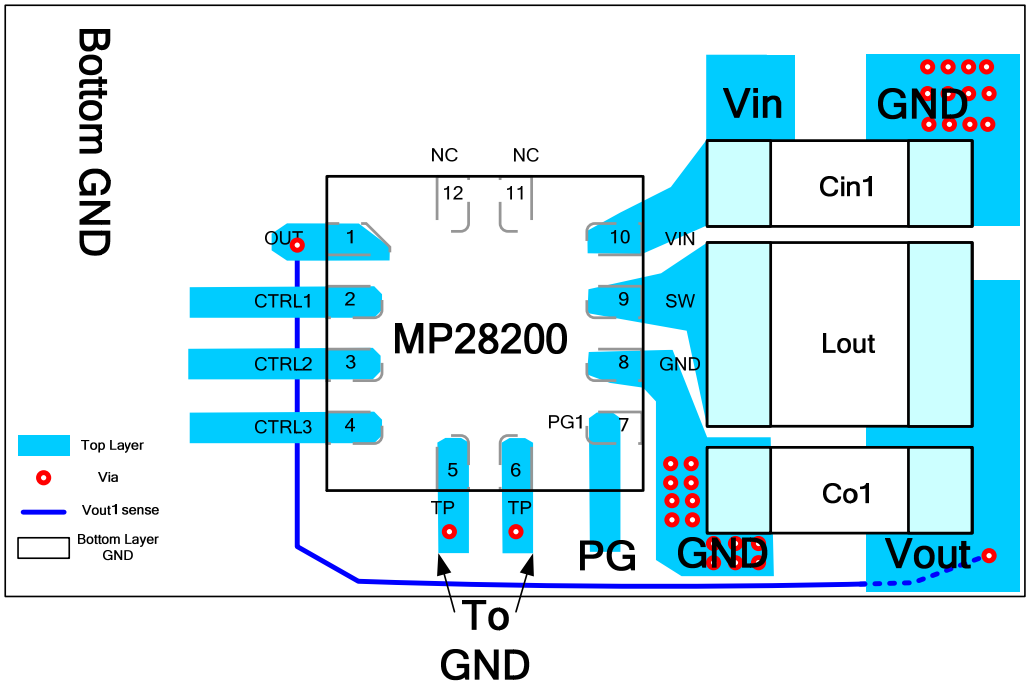

Figure 2: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

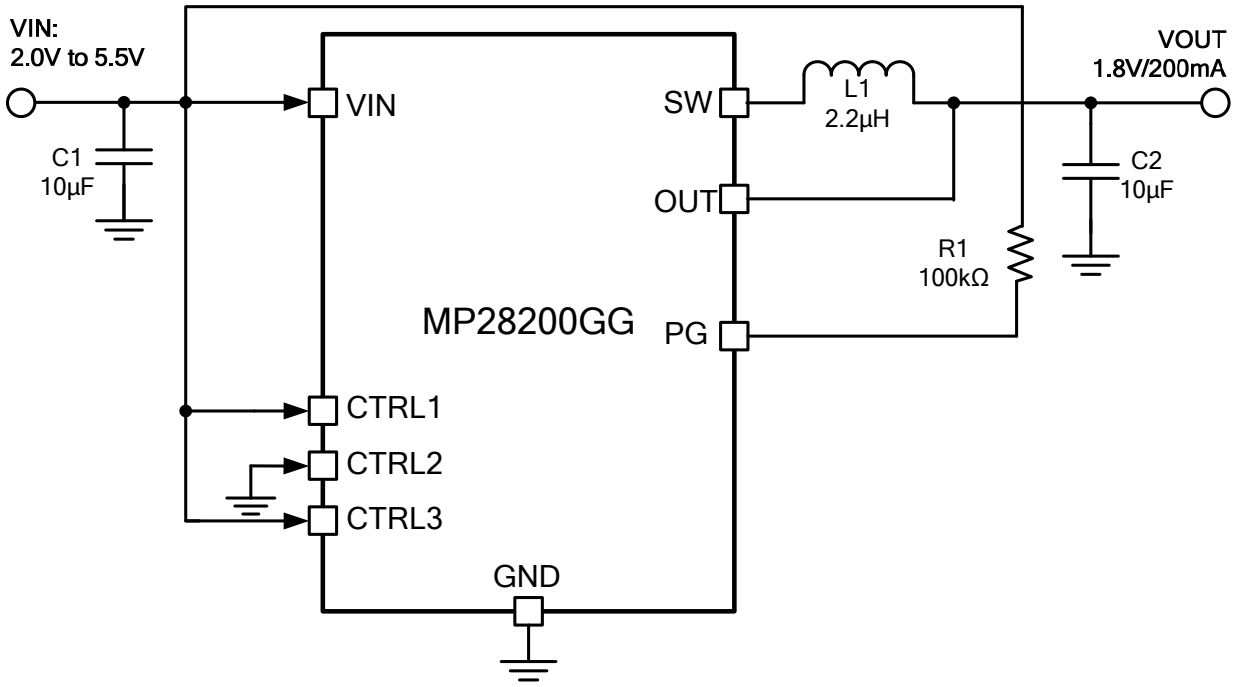

Figure 3: Typical Application Circuit for the MP28200GG

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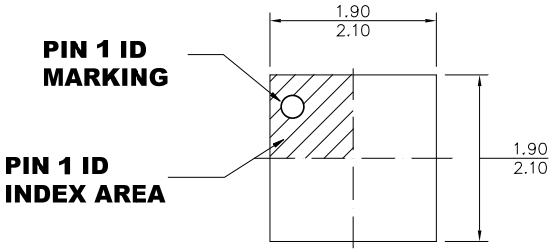
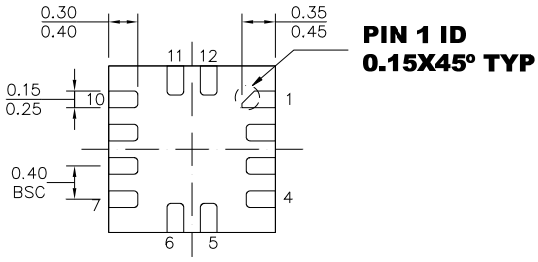
PACKAGE INFORMATION

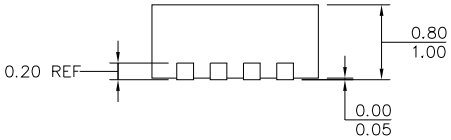
QFN-12 (2mmx2mm)



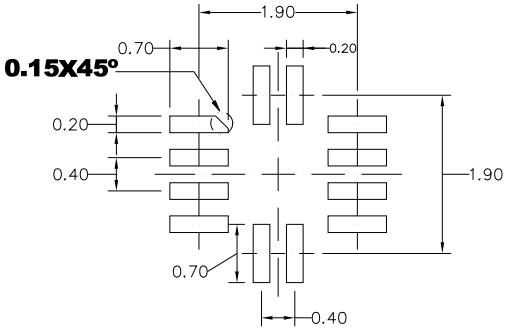
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

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2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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