



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5928	SSOP-24/QSOP-24	TLC5928DBQR	Tape and Reel, 2500
		TLC5928DBQ	Tube, 50
TLC5928	TSSOP-24	TLC5928PWR	Tape and Reel, 2000
		TLC5928PW	Tube, 60
TLC5928	HTSSOP-24 PowerPAD™	TLC5928PWPR	Tape and Reel, 2000
		TLC5928PWP	Tube, 60
TLC5928	QFN-24	TLC5928RGER	Tape and Reel, 3000
		TLC5928RGE	Tape and Reel, 250

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5928	UNIT
V _{CC}	Supply voltage: V _{CC}		–0.3 to +6.0	V
I _{OUT}	Output current (dc)	OUT0 to OUT15	40	mA
V _{IN}	Input voltage range		–0.3 to V _{CC} + 0.3	V
V _{OUT}	Output voltage range	SOUT	–0.3 to V _{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to +18	V
T _{J(MAX)}	Operating junction temperature		+150	°C
T _{STG}	Storage temperature range		–55 to +150	°C
ESD rating	Human body model (HBM)		2	kV
	Charged device model (CDM)		500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	OPERATING FACTOR ABOVE T _A = +25°C	T _A < +25°C POWER RATING	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
SSOP-24/QSOP-24	14.3 mW/°C	1782 mW	1140 mW	927 mW
TSSOP-24	9.6 mW/°C	1194 mW	764 mW	621 mW
HTSSOP-24 ⁽¹⁾	28.9 mW/°C	3611 mW	2311 mW	1878 mW
QFN-24 ⁽²⁾	24.8 mW/°C	3106 mW	1988 mW	1615 mW

- (1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see [SLMA002](#) (available for download at www.ti.com).
- (2) The package thermal impedance is calculated in accordance with JESD51-5.

RECOMMENDED OPERATING CONDITIONS

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5928			UNIT
			MIN	NOM	MAX	
DC Characteristics: V _{CC} = 3 V to 5.5 V						
V _{CC}	Supply voltage		3.0		5.5	V
V _O	Voltage applied to output	OUT0 to OUT15			17	V
V _{IH}	High-level input voltage		0.7 × V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage		GND		0.3 × V _{CC}	V
I _{OH}	High-level output current	SOUT			−1	mA
I _{OL}	Low-level output current	SOUT			1	mA
I _{OLC}	Constant output sink current	OUT0 to OUT15	2		35	mA
T _A	Operating free-air temperature range		−40		+85	°C
T _J	Operating junction temperature range		−40		+125	°C
AC Characteristics: V _{CC} = 3 V to 5.5 V						
f _{CLK} (SCLK)	Data shift clock frequency	SCLK			35	MHz
T _{WH0}	Pulse duration	SCLK	10			ns
T _{WL0}		SCLK	10			ns
T _{WH1}		LAT	20			ns
T _{WH2}		BLANK	20			ns
T _{WL2}		BLANK	20			ns
T _{SU0}		Setup time	SIN−SCLK↑	4		
T _{SU1}	LAT↑−SCLK↑		100			ns
T _{H0}	Hold time	SIN−SCLK↑	3			ns
T _{H1}		LAT↑−SCLK↑	10			ns

ELECTRICAL CHARACTERISTICS

At $V_{CC} = 3.0\text{ V}$ to 5.5 V and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values at $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5928			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -1\text{ mA}$ at SOUT	$V_{CC} - 0.4$		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL} = 1\text{ mA}$ at SOUT	0		0.4	V
I_{IN}	Input current	$V_{IN} = V_{CC}$ or GND at SIN, SCLK, LAT, and BLANK	-1		1	μA
I_{CC1}	Supply current (V_{CC})	SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 27\text{ k}\Omega$		1	2	mA
I_{CC2}		SIN/SCLK/LAT = low, BLANK = high, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 3\text{ k}\Omega$		4.5	8	mA
I_{CC3}		SIN/SCLK/LAT/BLANK = low, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 3\text{ k}\Omega$		7	18	mA
I_{CC4}		SIN/SCLK/LAT/BLANK = low, $V_{OUTn} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$		16	40	mA
I_{OLC}	Constant output current	All $OUTn = \text{ON}$, $V_{OUTn} = V_{OUTfix} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$ (see Figure 6), at OUT0 to OUT15	31	34	37	mA
I_{OLKG}	Output leakage current	All $OUTn$ for constant-current driver, all outputs off BLANK = high, $V_{OUTn} = V_{OUTfix} = 17\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$ (see Figure 6), at OUT0 to OUT15			0.1	μA
ΔI_{OLC}	Constant-current error (channel-to-channel) ⁽¹⁾	All $OUTn = \text{ON}$, $V_{OUTn} = V_{OUTfix} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15		± 1	± 3	%
ΔI_{OLC1}	Constant-current error (device-to-device) ⁽²⁾	All $OUTn = \text{ON}$, $V_{OUTn} = V_{OUTfix} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15		± 1	± 6	%
ΔI_{OLC2}	Line regulation ⁽³⁾	All $OUTn = \text{ON}$, $V_{OUTn} = V_{OUTfix} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$ at OUT0 to OUT15		± 0.5	± 1	%/V
ΔI_{OLC3}	Load regulation ⁽⁴⁾	All $OUTn = \text{ON}$, $V_{OUTn} = 1\text{ V}$ to 3 V , $V_{OUTfix} = 1\text{ V}$, $R_{IREF} = 1.5\text{ k}\Omega$, at OUT0 to OUT15		± 1	± 3	%/V
$T_{(PTW)}$	Pre-thermal warning threshold	Junction temperature ⁽⁵⁾	+125	+138	+150	$^\circ\text{C}$
V_{LOD}	LED open detection threshold	All $OUTn = \text{ON}$	0.25	0.30	0.35	V
V_{IREF}	Reference voltage output	$R_{IREF} = 1.5\text{ k}\Omega$	1.16	1.20	1.24	V

- (1) The deviation of each output from the average of OUT0–OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = \left[\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right] \times 100$$

- (2) The deviation of the OUT0–OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta (\%) = \left[\frac{\frac{(I_{OUT0} + I_{OUT1} + \dots + I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right] \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 42 \times \left[\frac{1.20}{R_{IREF}} \right]$$

- (3) Line regulation is calculated by this equation:

$$\Delta (\%/V) = \left[\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0\text{ V})} \right] \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

- (4) Load regulation is calculated by the equation:

$$\Delta (\%/V) = \left[\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right] \times \frac{100}{3\text{ V} - 1\text{ V}}$$

- (5) Not tested. Specified by design.

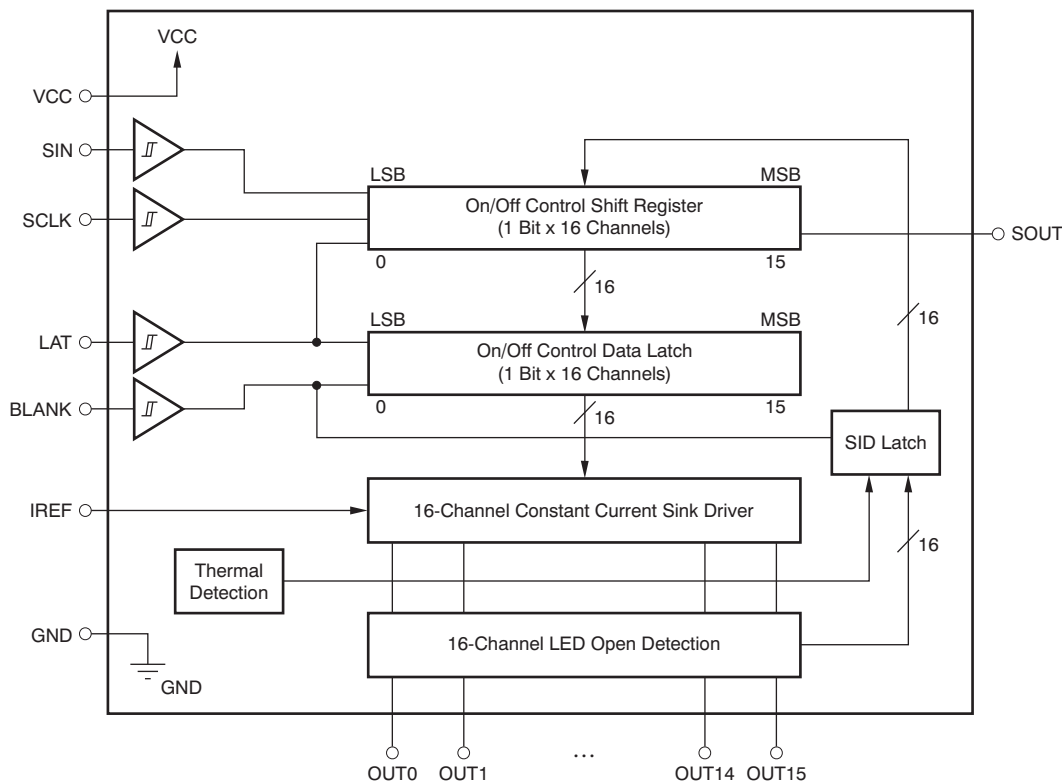
SWITCHING CHARACTERISTICS

At $V_{CC} = 3.0\text{ V}$ to 5.5 V , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $C_L = 15\text{ pF}$, $R_L = 130\ \Omega$, $R_{IREF} = 1.5\text{ k}\Omega$, and $V_{LED} = 5.5\text{ V}$. Typical values at $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5928			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 5)		5	15	ns
t_{R1}		OUTn (see Figure 4)		10	30	ns
t_{F0}	Fall time	SOUT (see Figure 5)		5	15	ns
t_{F1}		OUTn (see Figure 4)		10	30	ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT		8	20	ns
t_{D1}		LAT↑ or BLANK↓ to OUTn sink current on (see Figure 10)		12	30	ns
t_{D2}		LAT↑ or BLANK↑ to OUTn sink current off (see Figure 10)		12	30	ns
t_{ON_ERR}	Output on-time error ⁽¹⁾	On/off latch data = all '1', 20 ns BLANK low level one-shot pulse input (see Figure 4)	–8		+8	ns

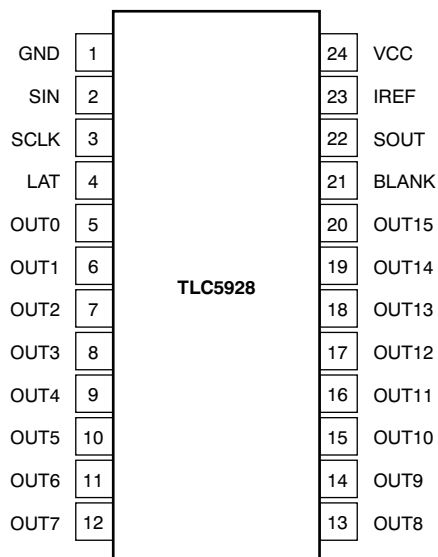
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: $t_{ON_ERR} (\text{ns}) = t_{OUT_ON} - \text{BLANK low level one-shot pulse width } (T_{WL2})$. t_{OUT_ON} indicates the actual on-time of the constant-current driver.

FUNCTIONAL BLOCK DIAGRAM

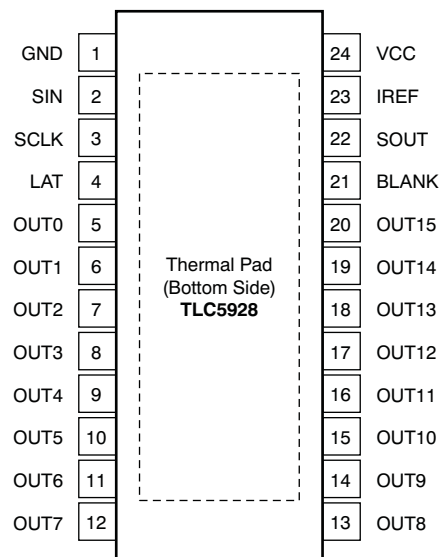


DEVICE INFORMATION

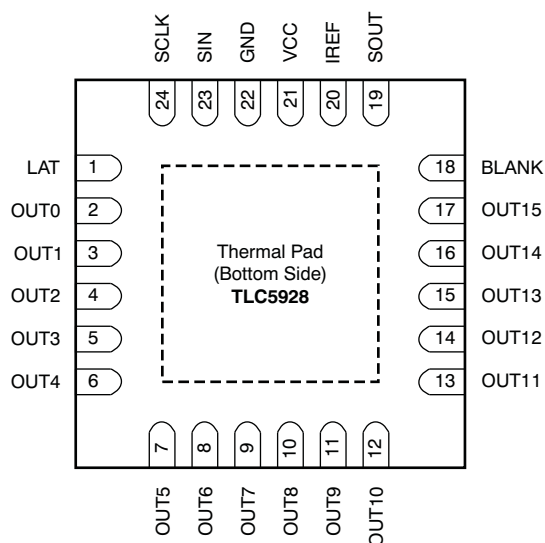
**SSOP-24/QSOP-24 AND TSSOP-24
DBQ AND PW PACKAGES
(TOP VIEW)**



**HTSSOP-24 PowerPAD
PWP PACKAGE
(TOP VIEW)**



**QFN-24
RGE PACKAGE
(TOP VIEW)**



NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	DBQ/PW/ PWP	RGE		
SIN	2	23	I	Serial data input for driver on/off control. When SIN = high level, data '1' are written into LSB of the on/off control shift register at the rising edge of SCLK.
SCLK	3	24	I	Serial data shift clock. Schmitt buffer input. All data in the on/off control shift register are shifted toward the MSB by 1-bit synchronization of SCLK. A rising edge on SCLK is allowed 100 ns after a rising edge of LAT.
LAT	4	1	I	Edge triggered latch. The data in the on/off control data shift register are transferred to the on/off control data latch at this rising edge. At the same time, the data in the on/off control shift register are replaced with LED open detection (LOD) and pre-thermal warning (PTW) data. LAT must be toggled only once after the shift data are updated to avoid the on/off control latch data being replaced with LOD and PTW data in the shift register.
BLANK	21	18	I	Blank, all outputs. When BLANK = high level, all constant-current outputs (OUT0–OUT15) are forced off. When BLANK = low level, all constant-current outputs are controlled by the on/off control data in the data latch. LOD and PTW data are latched into the SID data latch at the rising edge of BLANK and are present at the output of the SID data latch when BLANK is low.
IREF	23	20	I/O	Constant-current value setting, OUT0–OUT15 sink constant-current is set to desired value by connection to an external resistor between IREF and GND.
SOUT	22	19	O	Serial data output. This output is connected to the MSB of the on/off data shift register. SOUT data changes at the rising edge of SCLK.
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	O	Constant-current output
OUT2	7	4	O	Constant-current output
OUT3	8	5	O	Constant-current output
OUT4	9	6	O	Constant-current output
OUT5	10	7	O	Constant-current output
OUT6	11	8	O	Constant-current output
OUT7	12	9	O	Constant-current output
OUT8	13	10	O	Constant-current output
OUT9	14	11	O	Constant-current output
OUT10	15	12	O	Constant-current output
OUT11	16	13	O	Constant-current output
OUT12	17	14	O	Constant-current output
OUT13	18	15	O	Constant-current output
OUT14	19	16	O	Constant-current output
OUT15	20	17	O	Constant-current output
VCC	24	21	—	Power-supply voltage
GND	1	22	—	Power ground

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

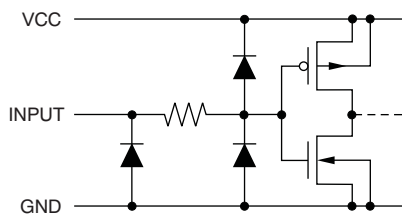


Figure 1. SIN, SCLK, LAT, BLANK

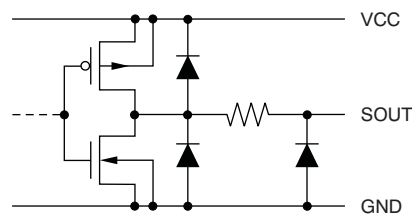


Figure 2. SOUT

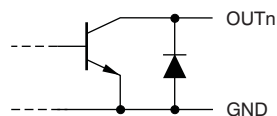
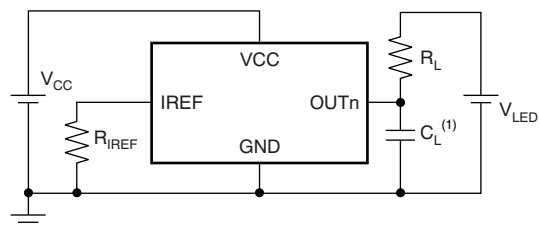


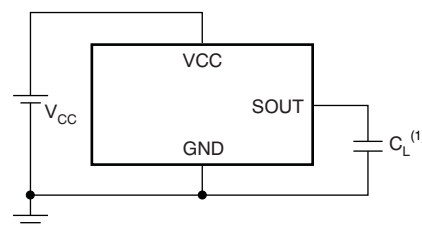
Figure 3. OUT0 Through OUT15

TEST CIRCUITS



(1) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

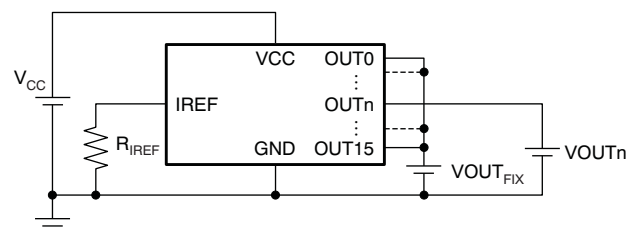
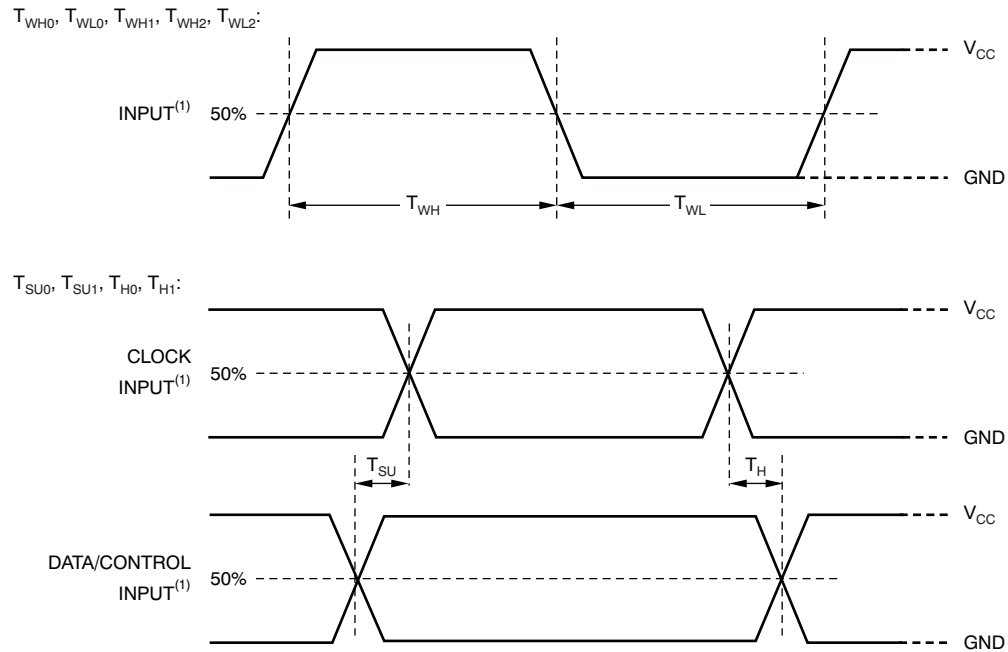


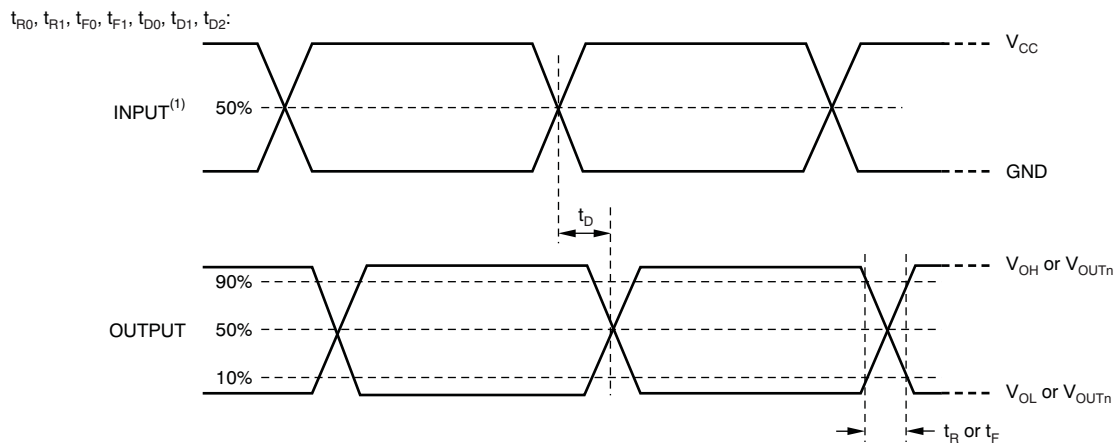
Figure 6. Constant-Current Test Circuit for OUTn

TIMING DIAGRAMS



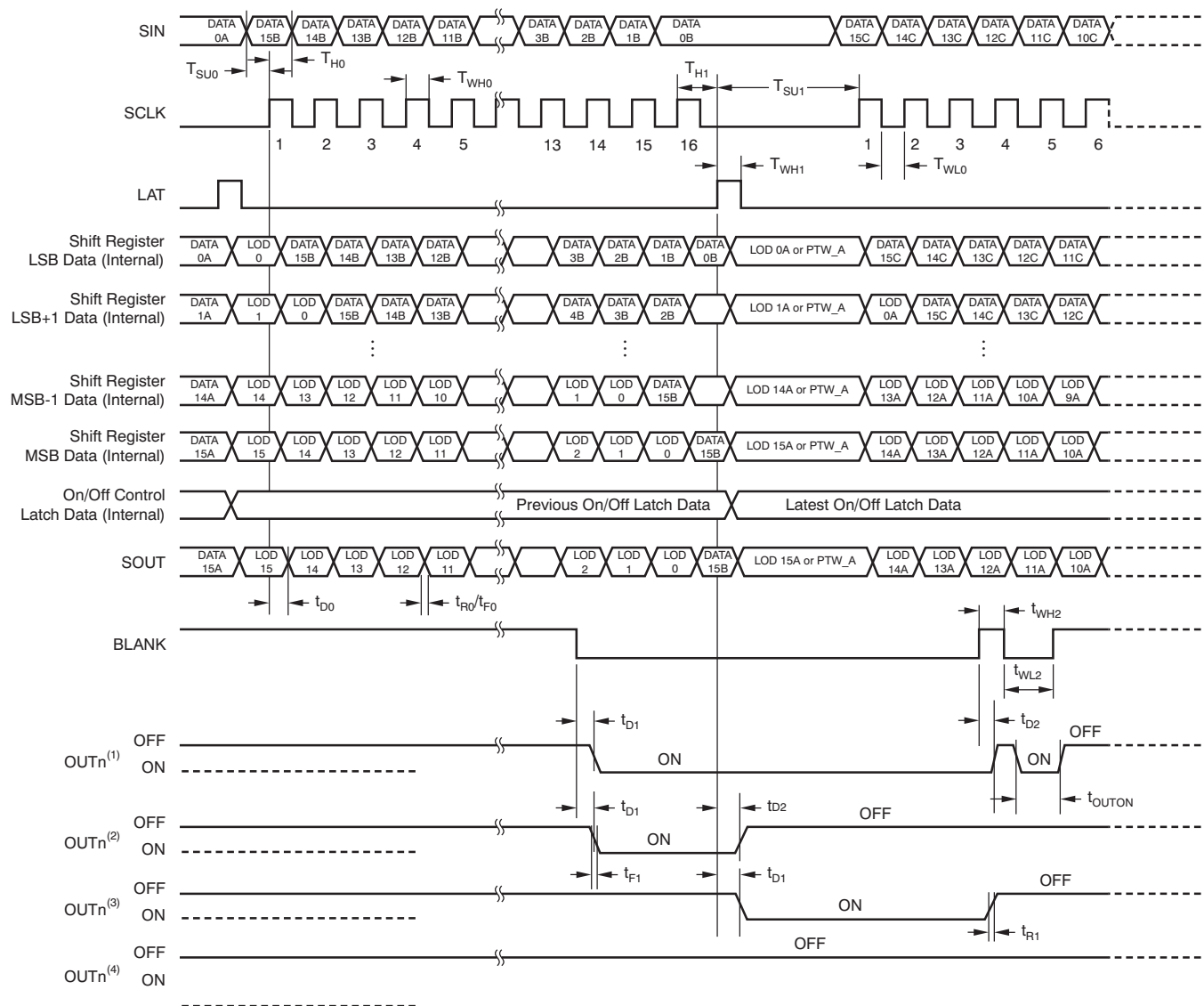
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing



- (1) On/off latched data are '1'.
- (2) On/off latched data are changed from '1' to '0' at the second LAT signal.
- (3) On/off latched data are changed from '0' to '1' at the second LAT signal.
- (4) On/off latched data are '0'.

Figure 9. Timing Diagram

TYPICAL CHARACTERISTICS

At $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

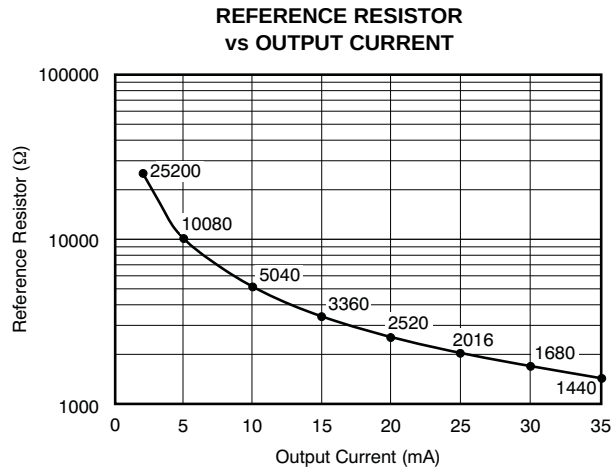


Figure 10.

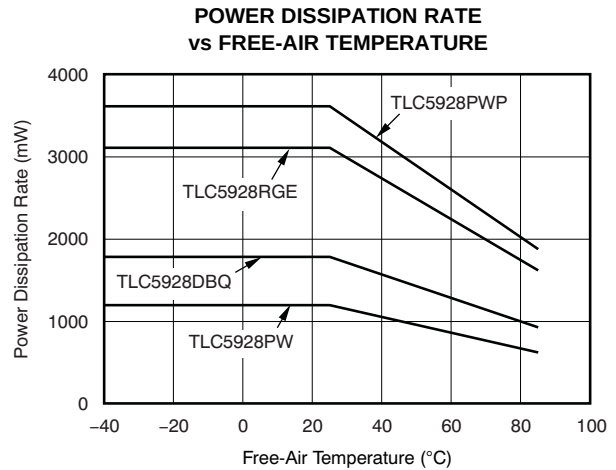


Figure 11.

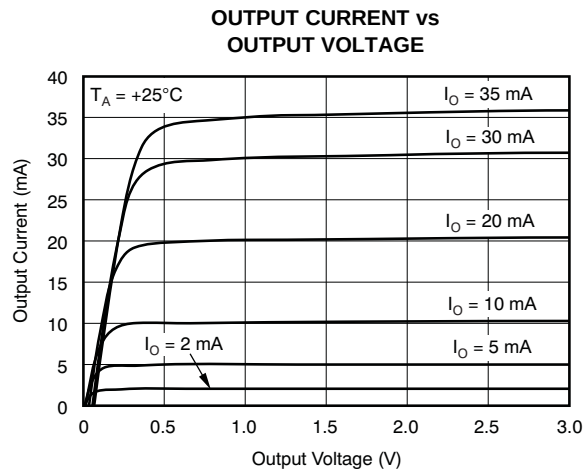


Figure 12.

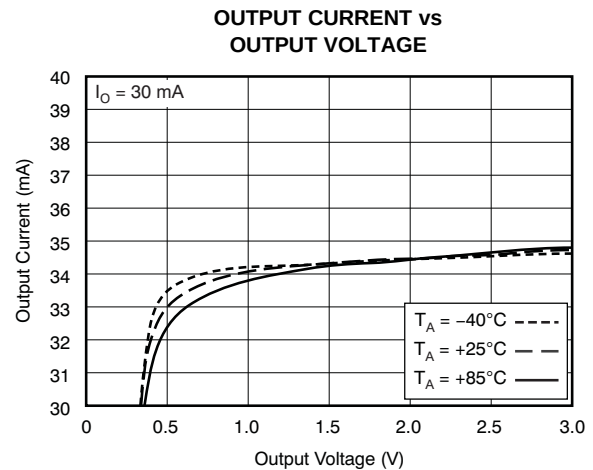


Figure 13.

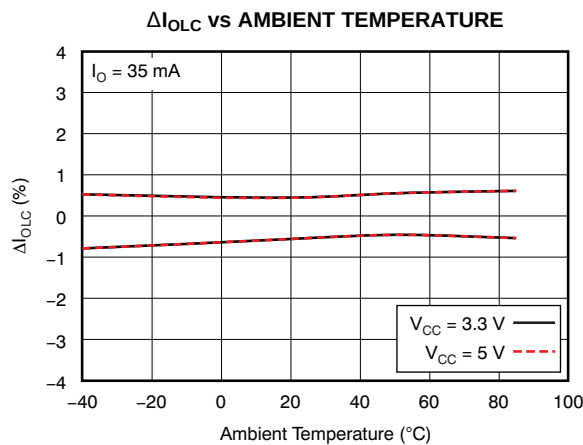


Figure 14.

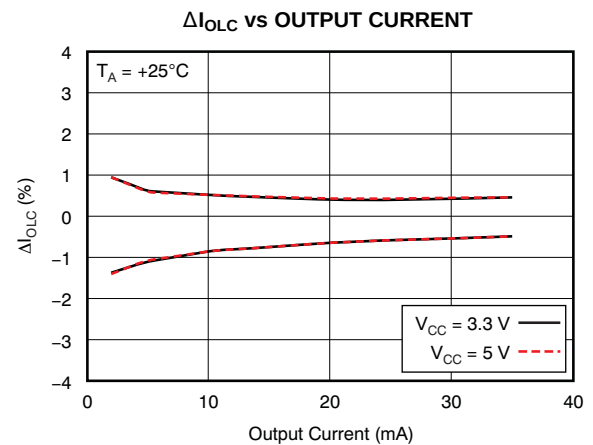


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At $V_{CC} = 3.3\text{ V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

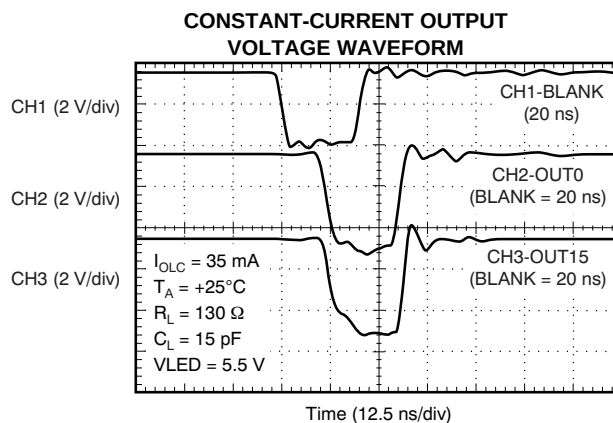


Figure 16.

DETAILED DESCRIPTION

SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by [Equation 1](#).

$$R_{IREF} (k\Omega) = \frac{V_{IREF} (V)}{I_{OLC} (mA)} \times 42$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V) (1)

I_{OLC} must be set in the range of 2 mA to 35 mA. The constant sink current characteristic for the external resistor value is shown in [Figure 10](#). [Table 1](#) describes the constant-current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLCMax} (mA, Typical)	R_{IREF} (k Ω)
35	1.44
30	1.68
25	2.02
20	2.52
15	3.36
10	5.04
5	10.1
2	25.2

CONSTANT-CURRENT DRIVER ON/OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on/off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in [Table 2](#).

Table 2. On/Off Control Data Truth Table

ON/OFF CONTROL LATCH DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the IC is initially powered on, the data in the on/off control shift register and data latch are not set to the respective default value. Therefore, the on/off control data must be written to the data latch before turning the constant-current output on. BLANK should be at a high level when powered on because the constant-current may be turned on as a result of random data in the on/off control latch.

The on/off data corresponding to any unconnected OUTn outputs should be set to '0' before turning on the remaining outputs. Otherwise, the supply current (I_{CC}) increases while the LEDs are on.

REGISTER CONFIGURATION

The TLC5928 has an on/off control data shift register and data latch. Both the on/off control shift register and latch are 16 bits long and are used to turn on/off the constant-current drivers. Figure 17 shows the shift register and latch configuration. The data at the SIN pin is shifted in to the LSB of the shift register at the rising edge of the SCLK pin; SOUT data change at the rising edge of SCLK. The timing diagram for data writing is shown in Figure 18. The driver on/off is controlled by the data in the on/off control data latch.

The on/off data are latched into the data latch by a rising edge of LAT after the data are written into the on/off control shift register by SIN and SCLK. At the same time, the data in the on/off control shift register are replaced with LED open detection (LOD) and pre-thermal warning (PTW) data. Therefore, LAT must be input only once after the on/off data update to avoid the on/off control data latch being replaced with LOD and PTW data in the shift register. When the IC is initially powered on, the data in the on/off control shift register and latch are not set to the default values; on/off control data must be written to the on/off control data latch before turning the constant-current output on. BLANK should be high when the IC is powered on because the constant-current may be turned on at that time as a result of random values in the on/off data latch. All constant-current outputs are forced off when BLANK is high.

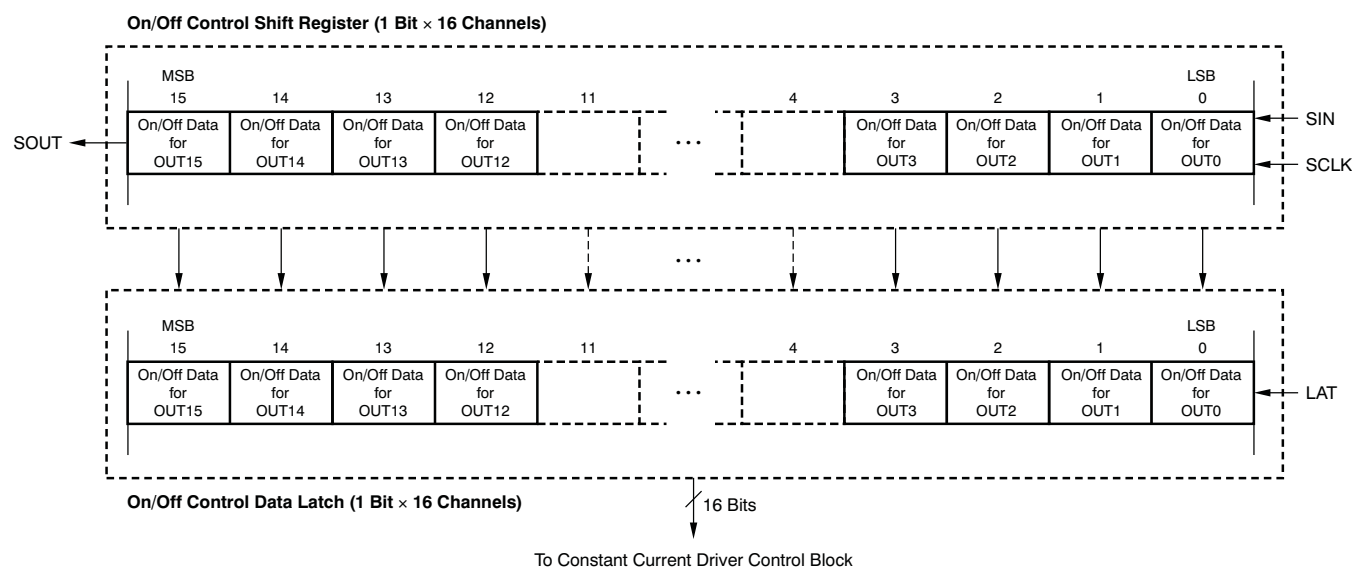
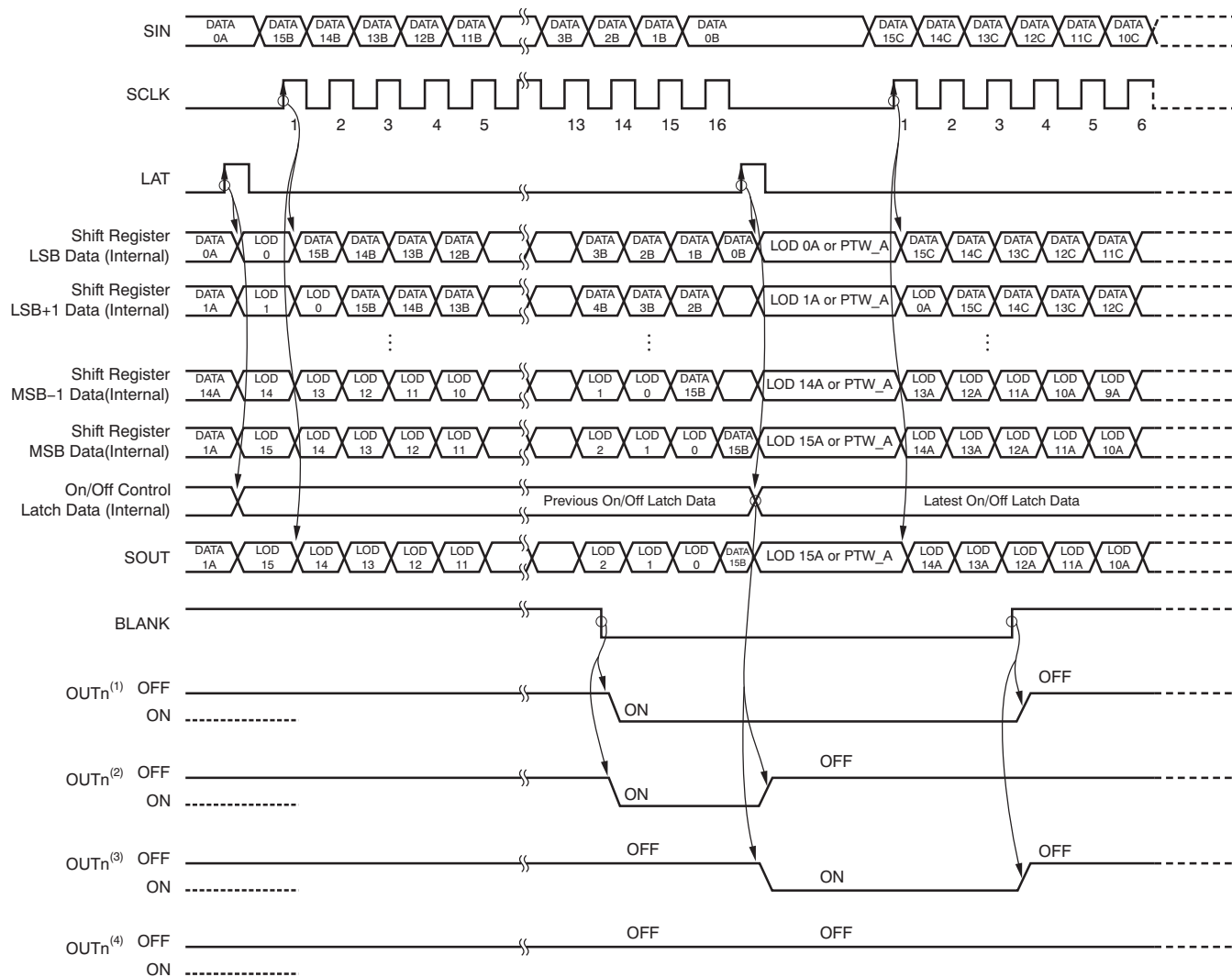


Figure 17. On/Off Control Shift Register and Latch Configuration



- (1) On/off latched data are '1'.
- (2) On/off latched data are changed from '1' to '0' at the second LAT signal.
- (3) On/off latched data are changed from '0' to '1' at the second LAT signal.
- (4) On/off latched data are '0'.

Figure 18. On/Off Control Operation

LED OPEN DETECTION (LOD) AND PRE-THERMAL WARNING (PTW)

The LED open detection (LOD) circuit checks the voltage of each active (that is, on) constant-current sink output (OUT0 through OUT15) to detect open LEDs and LEDs shorted to GND while BLANK is low. The LOD bits in the status information data register (SID) are set to '1' if the voltage of the corresponding OUTn pin is less than the LED open detection threshold ($V_{\text{LOD}} = 0.3 \text{ V}$, typ). The status information data can be read from the SOUT pin. To avoid false detection of open LEDs, the LED driver design must ensure that the constant-current sink output voltage is greater than 0.3 V when the outputs are on. Also, the output on-time must be 1 μs or greater to correctly read the valid LOD status.

The PTW function indicates that the IC junction temperature is too high. The PTW bit in the SID data is set to '1' while the IC junction temperature exceeds the temperature threshold ($T_{(\text{PTW})} = +138^\circ\text{C}$, typ). If the IC junction temperature decreases below the temperature of $T_{(\text{PTW})}$, the SID data are set depending on the LOD function. The constant-current outputs are not forced off during PTW conditions, so the controller should take appropriate action (such as reducing the duty cycle of effected channels).

The LOD and PTW data are latched into the SID latch with the rising edge of BLANK and do not change until BLANK goes low. The SID data latched in the latch are transferred into the on/off shift register with a rising edge of LAT. SID can be shifted out from SOUT with rising edges of SCLK. The data in the on/off control shift register are replaced with the LOD and PTW data at the rising edge of LAT. Therefore, LAT should be input only once after the shift data are updated to avoid the on/off control data latch information from being replaced with LOD and PTW data in the shift register. A timing diagram for LOD, PTW, and SID is shown in Figure 19.

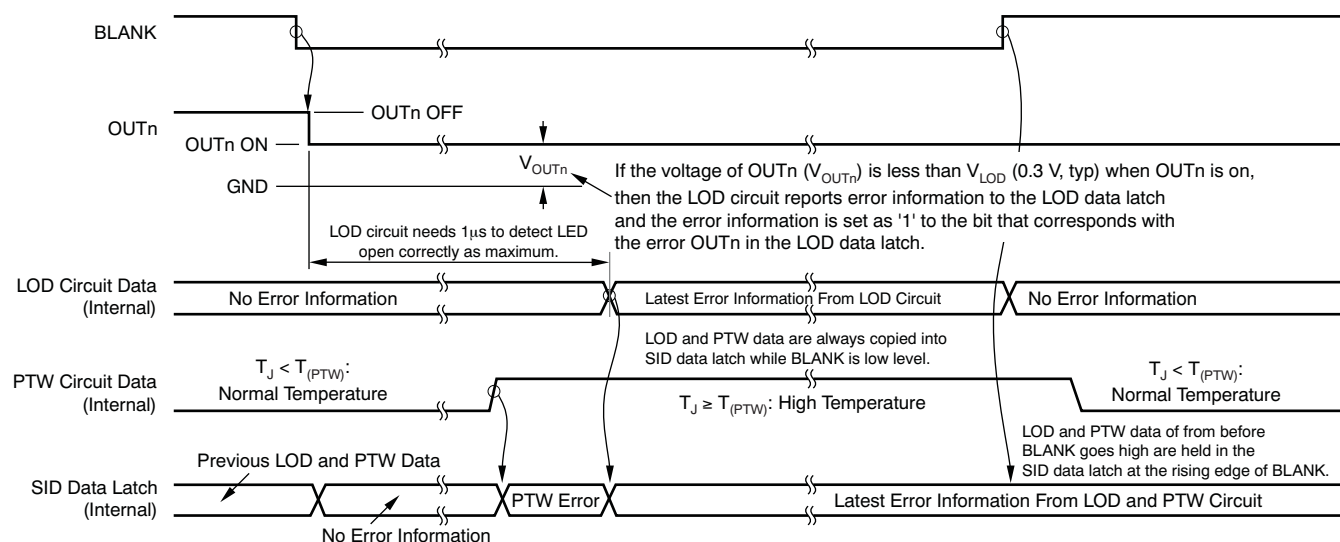


Figure 19. LOD/PTW/SID timing

STATUS INFORMATION DATA (SID)

The latched LED open detection (LOD) error and pre-thermal warning (PTW) in the SID data latch are shifted out onto the SOUT pin with each rising edge of SCLK. If a PTW is reported, all LOD error bits are set to '1'. The SID data are written over the data in the on/off control shift register at the rising edge of LAT. Therefore, the previous data in the on/off control shift register are lost when SID information is latched in. Figure 20 shows the SID bit assignments. See Figure 7 for the read timing of SID.

When the IC is powered on, the initial LOD data are invalid. Therefore, LOD data must be read after the rising edge of BLANK. Table 3 shows a truth table for LOD and PTW.

Table 3. LOD and PTW Truth Table

	CONDITION	SID DATA
LED open detection (LODn)	LED is connected ($V_{OUTn} > V_{LOD}$)	'0' (low level at SOUT)
	LED is opened or shorted to GND ($V_{OUTn} \leq V_{LOD}$ and output on)	'1' (high level at SOUT); set to the bit that has an LED error condition
Pre-thermal warning (PTW)	IC temperature is low (IC temperature $\leq T_{(PTW)}$)	Depend LED open error
	IC temperature is high (IC temperature $> T_{(PTW)}$)	All bits = '1' (high level at SOUT)

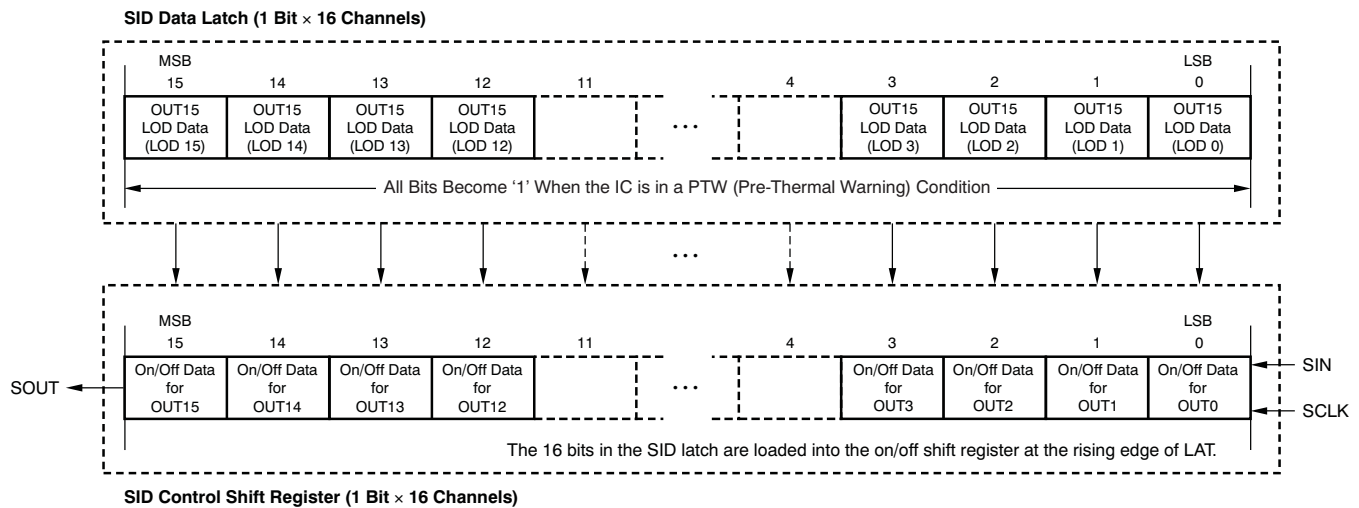


Figure 20. Status Information Data Configuration

LAYOUT CONSIDERATIONS

The output current transient time in the TLC5928 is very fast. In addition, all outputs turn on or off at the same time to minimize the output on-time error. This high current demand can cause GND to shift in the entire system, and lead to false triggering of signals. To overcome this issue, design all GND lines to be as wide and short as possible in order to reduce parasitic inductance and resistance.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2010) to Revision E

Page

- Added *Layout Considerations* section 17

Changes from Revision C (November 2008) to Revision D

Page

- Changed SO-24 to SSOP-24/QSOP-24 in Package/Ordering Information table 2
- Changed SO-24 to SSOP-24/QSOP-24 in Dissipation Ratings table 2
- Updated functional block diagram 5
- Changed SO-24 to SSOP-24/QSOP-24 in DBQ and PW Packages pinout 6
- Updated [Figure 9](#) 10
- Updated [Figure 18](#) 15

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5928DBQ	Active	Production	SSOP (DBQ) 24	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5928
TLC5928DBQ.B	Active	Production	SSOP (DBQ) 24	50 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5928
TLC5928DBQR	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5928
TLC5928DBQR.B	Active	Production	SSOP (DBQ) 24	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5928
TLC5928PW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5928
TLC5928PW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5928
TLC5928PWP	Active	Production	HTSSOP (PWP) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5928
TLC5928PWP.B	Active	Production	HTSSOP (PWP) 24	60 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5928
TLC5928PWPR	Active	Production	HTSSOP (PWP) 24	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5928
TLC5928PWPR.B	Active	Production	HTSSOP (PWP) 24	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PJ5928
TLC5928PWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5928
TLC5928PWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PJ5928
TLC5928RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928
TLC5928RGER.B	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928
TLC5928RGET	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928
TLC5928RGET.B	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928
TLC5928RGETG4	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928
TLC5928RGETG4.B	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 5928

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5928DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5928RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC5928RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC5928RGETG4	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5928DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC5928RGER	VQFN	RGE	24	3000	353.0	353.0	32.0
TLC5928RGET	VQFN	RGE	24	250	213.0	191.0	35.0
TLC5928RGETG4	VQFN	RGE	24	250	213.0	191.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC5928DBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32
TLC5928DBQ.B	DBQ	SSOP	24	50	506.6	8	3940	4.32
TLC5928PW	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5928PW.B	PW	TSSOP	24	60	530	10.2	3600	3.5
TLC5928PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TLC5928PWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

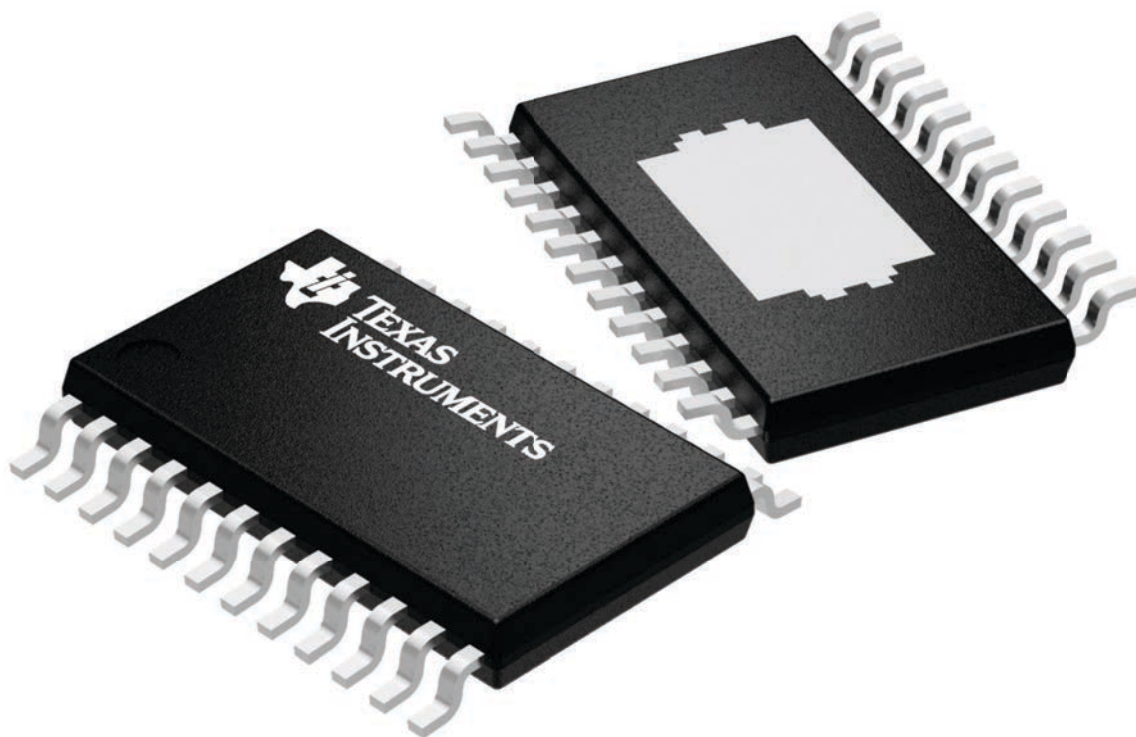
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

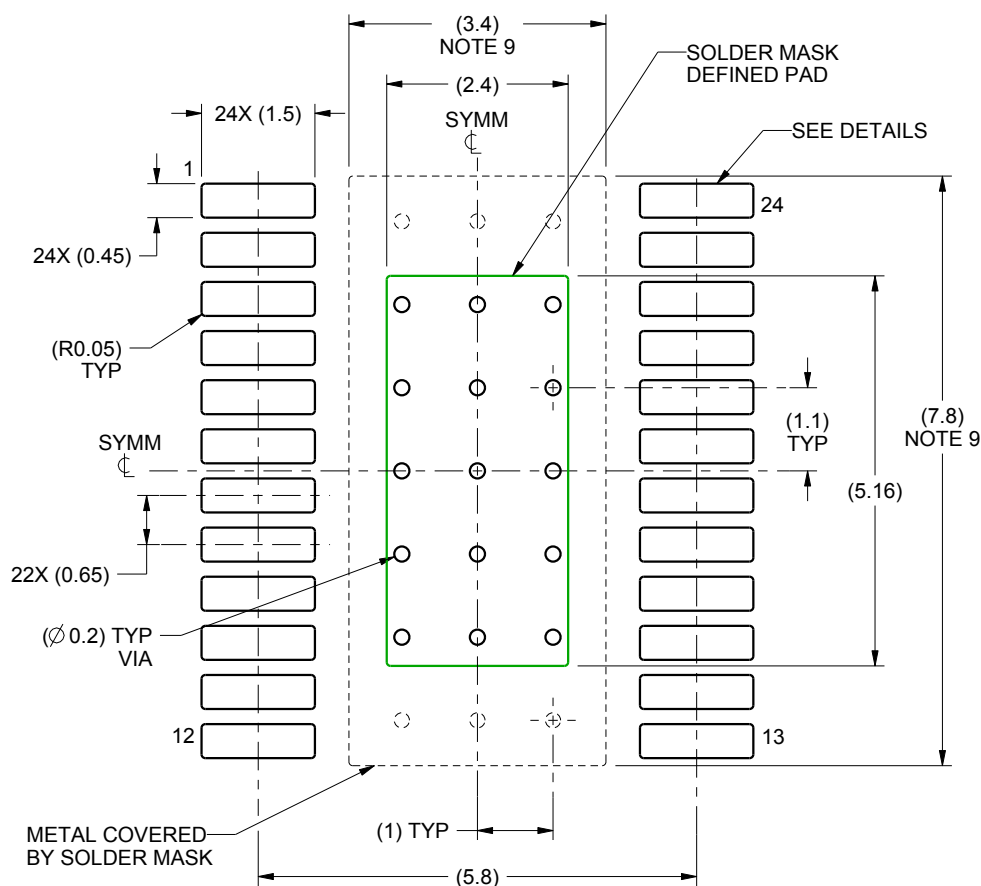
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.

EXAMPLE BOARD LAYOUT

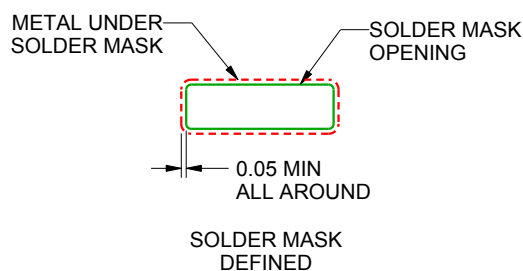
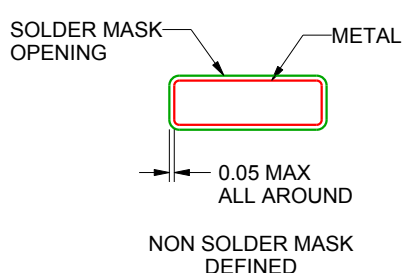
PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-24

4222709/A 02/2016

NOTES: (continued)

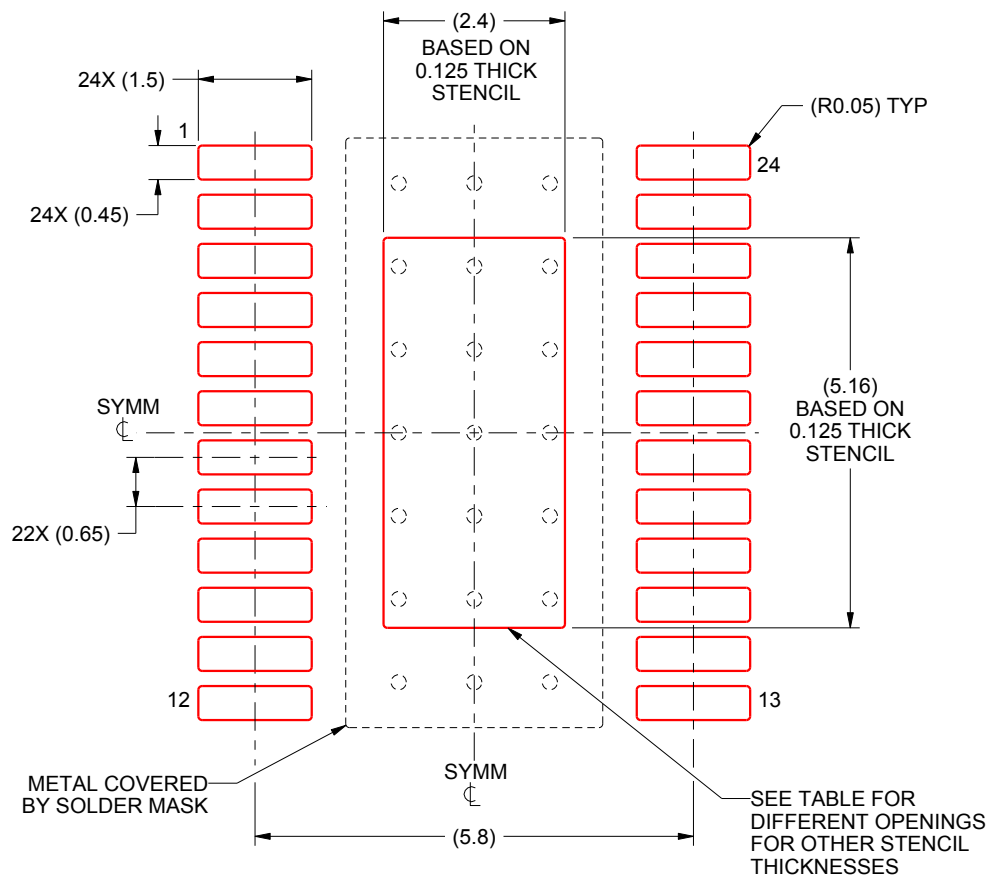
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

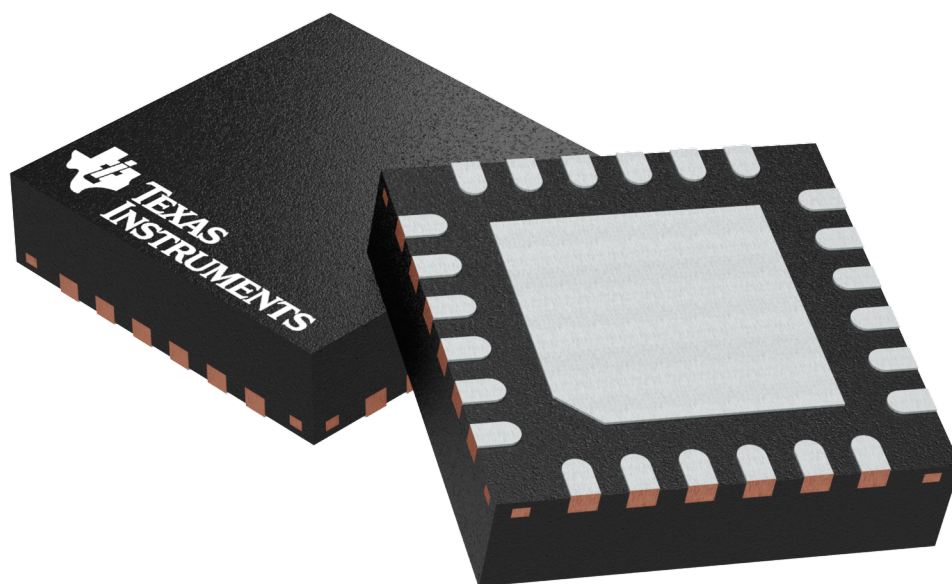
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

RGE 24

GENERIC PACKAGE VIEW

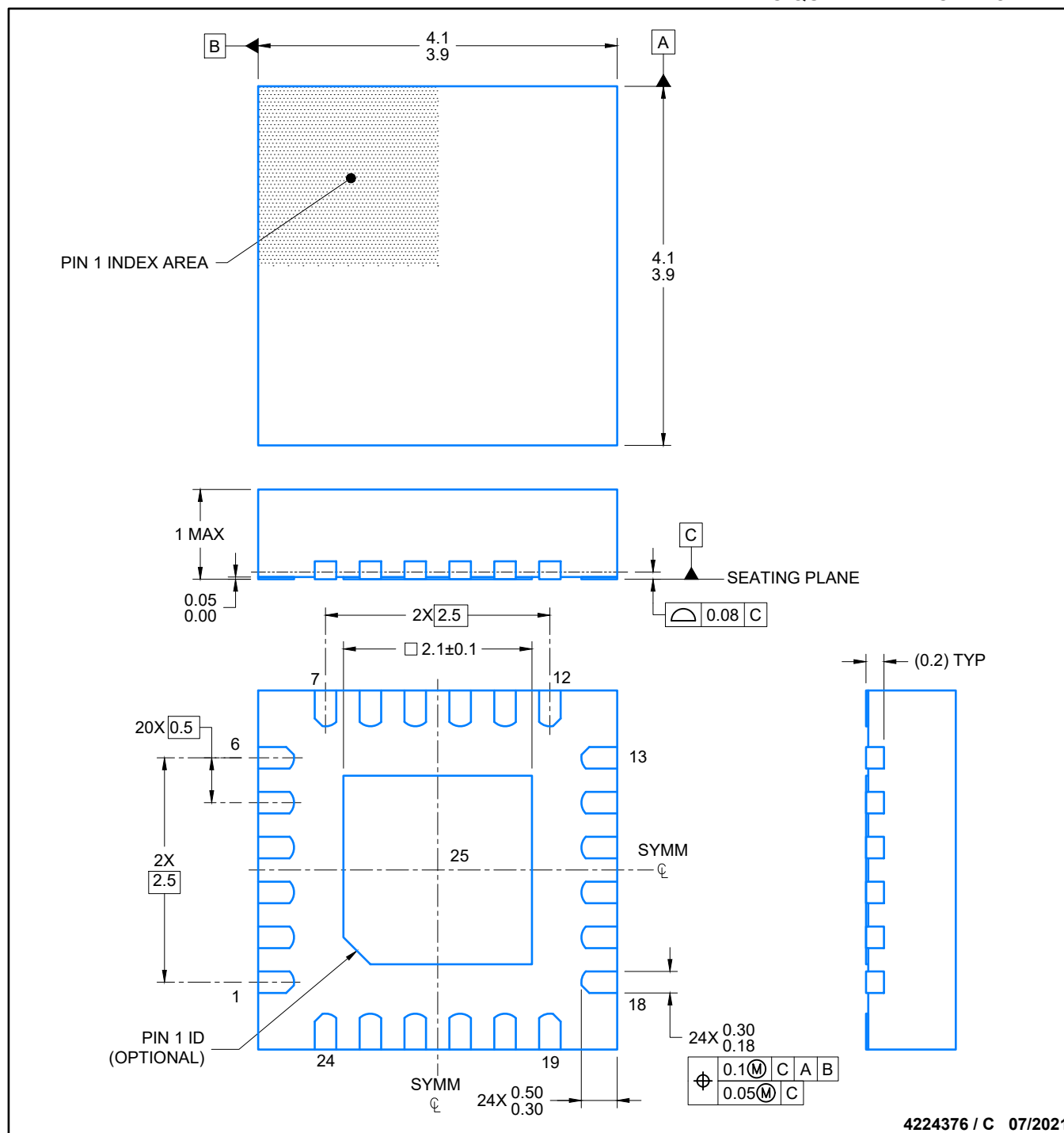
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

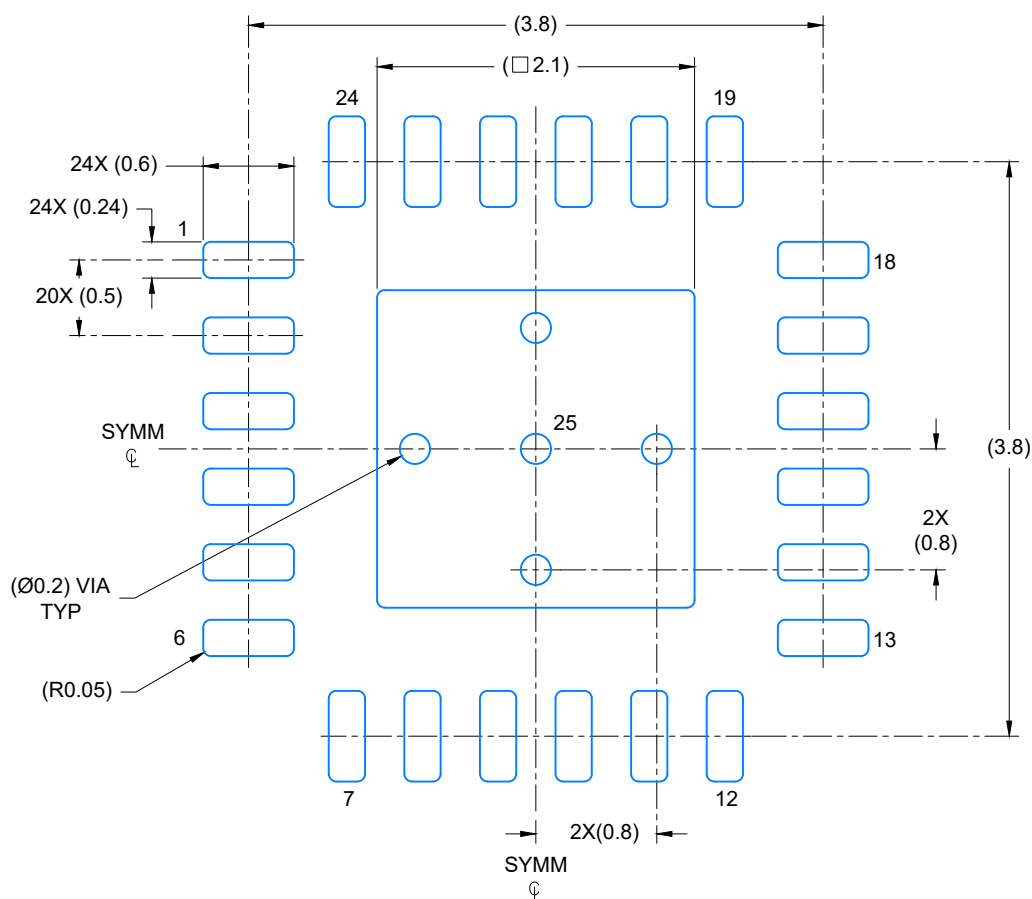
4204104/H



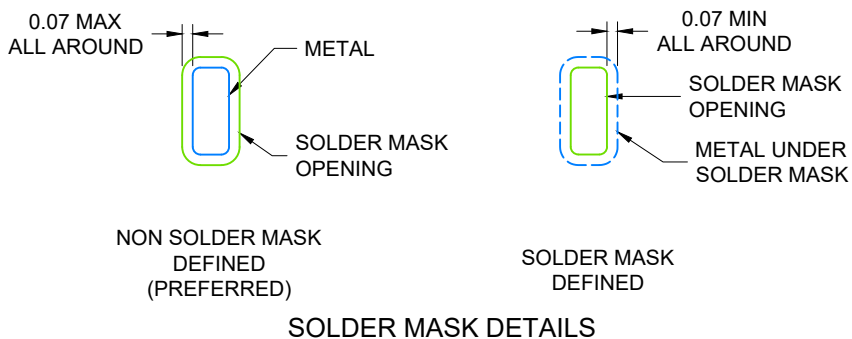
4224376 / C 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



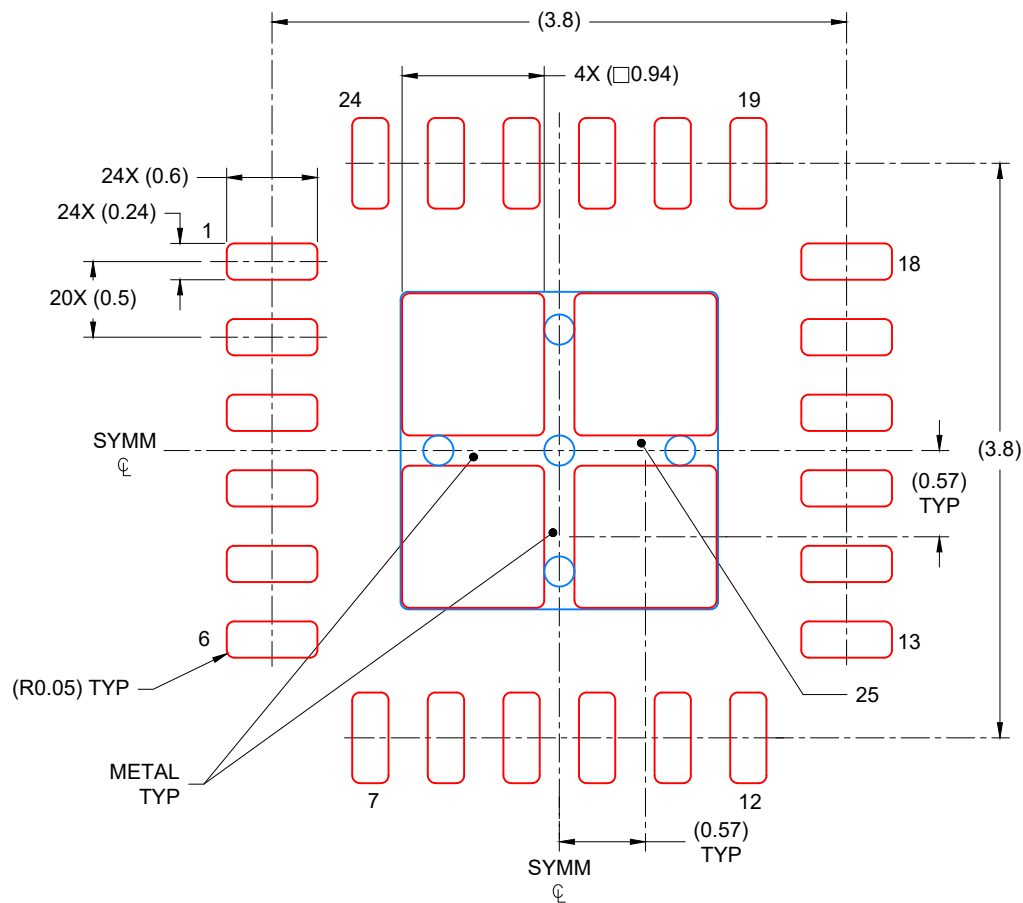
LAND PATTERN EXAMPLE
SCALE: 20X



4224376 / C 06/2021

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

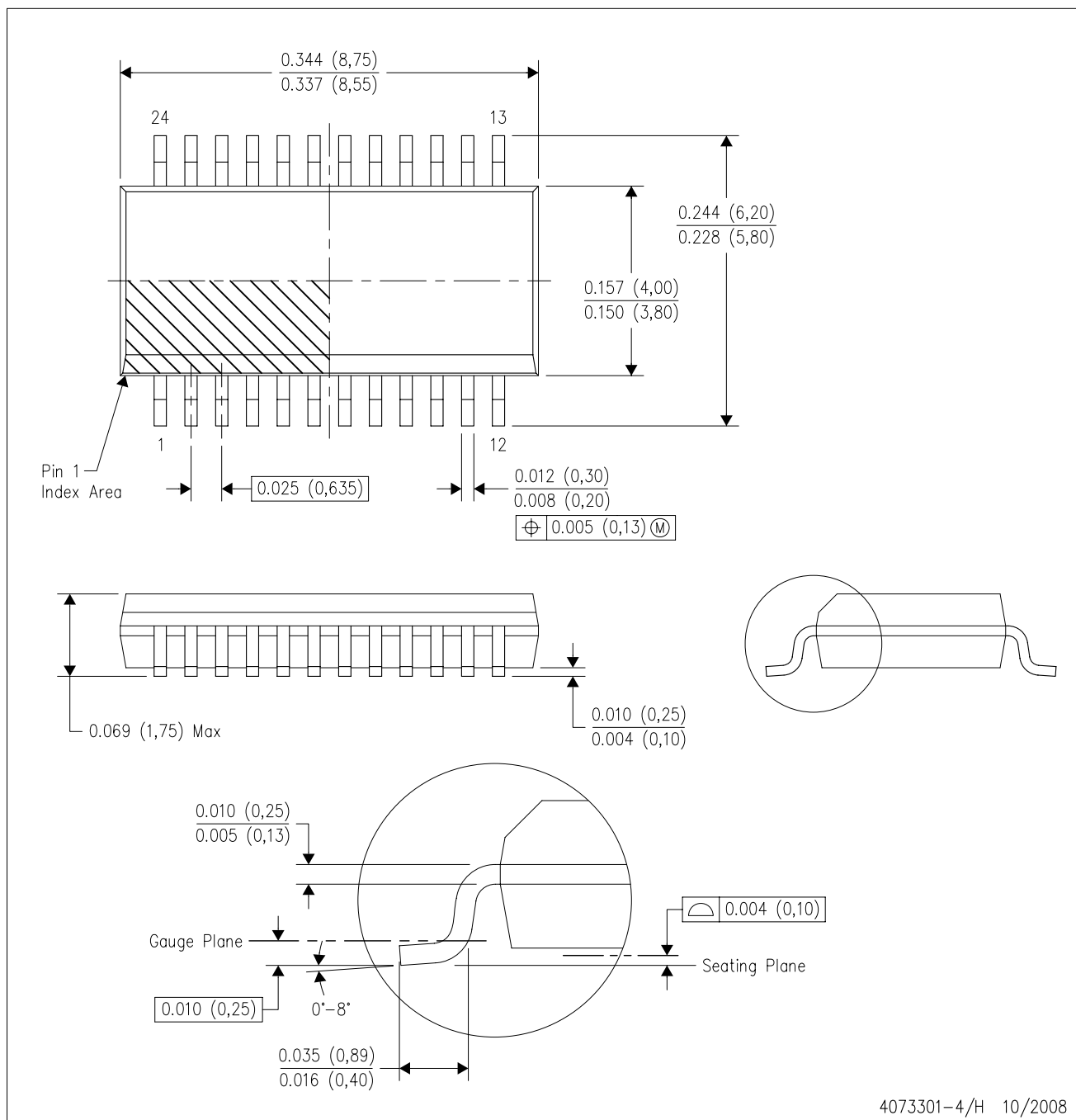
4224376 / C 06/2021

NOTES: (continued)

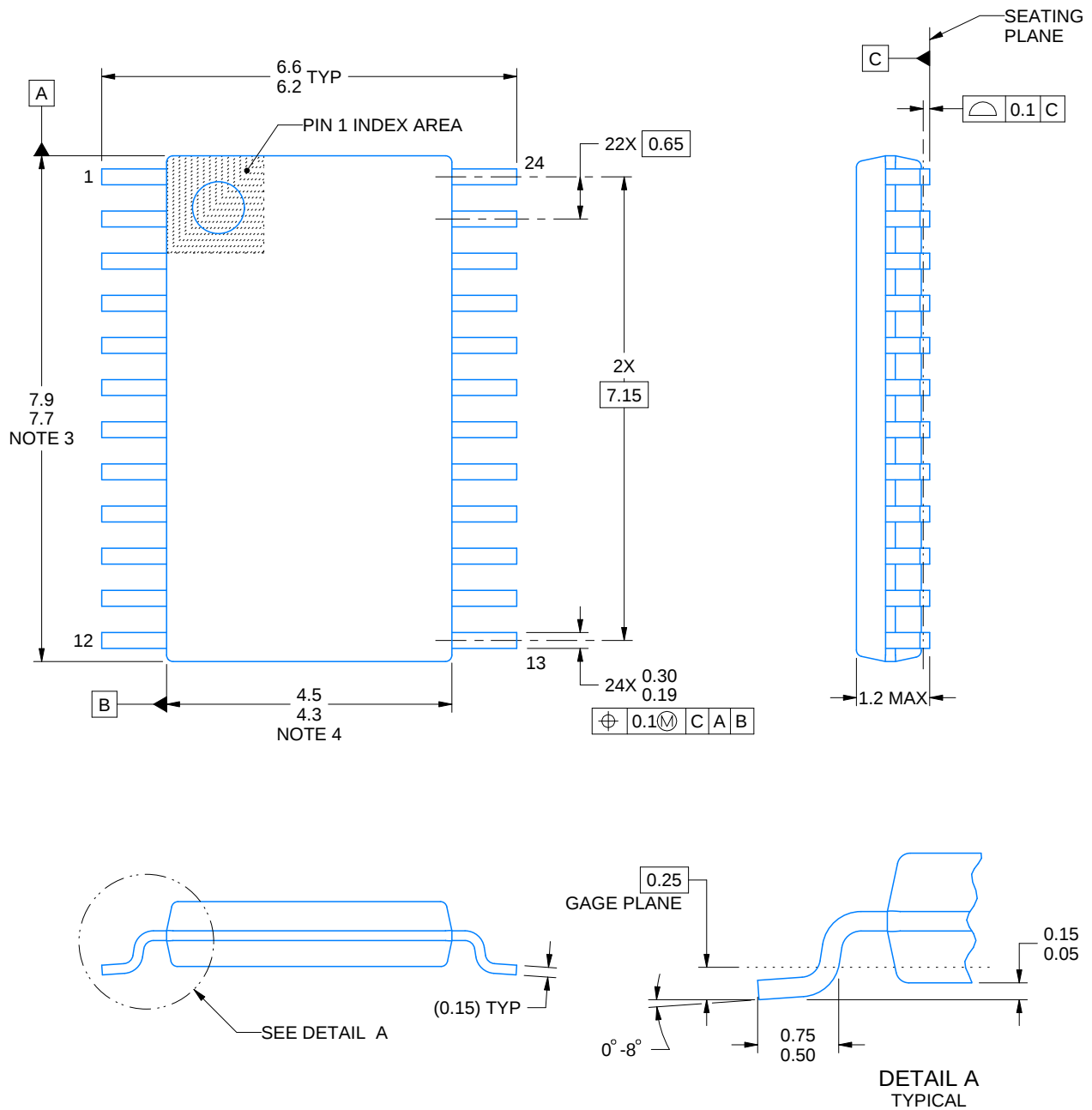
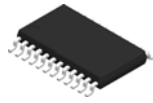
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
 - D. Falls within JEDEC MO-137 variation AE.



4220208/A 02/2017

NOTES:

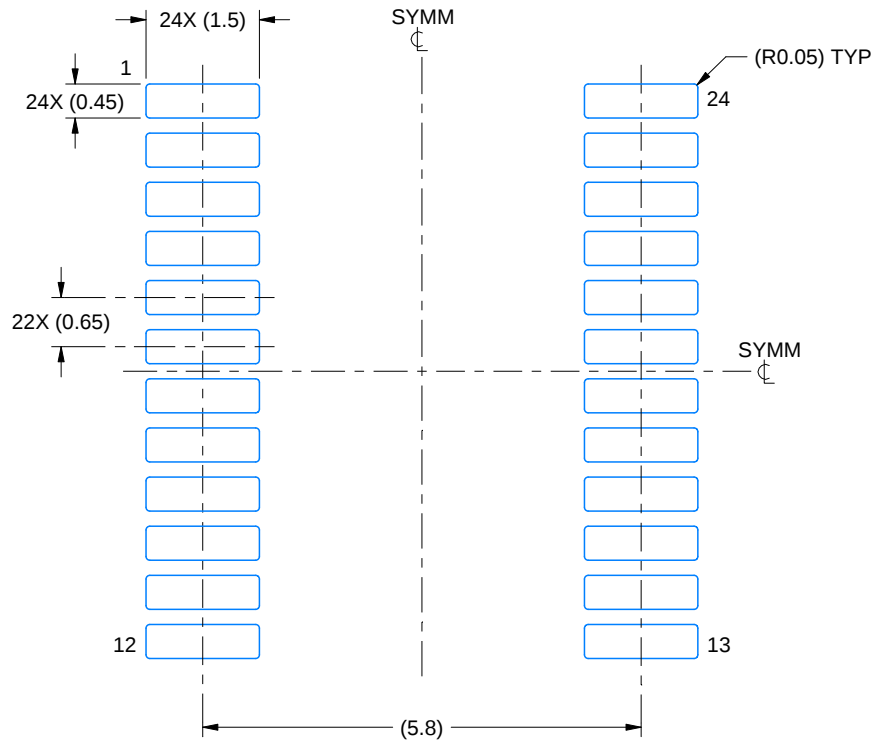
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

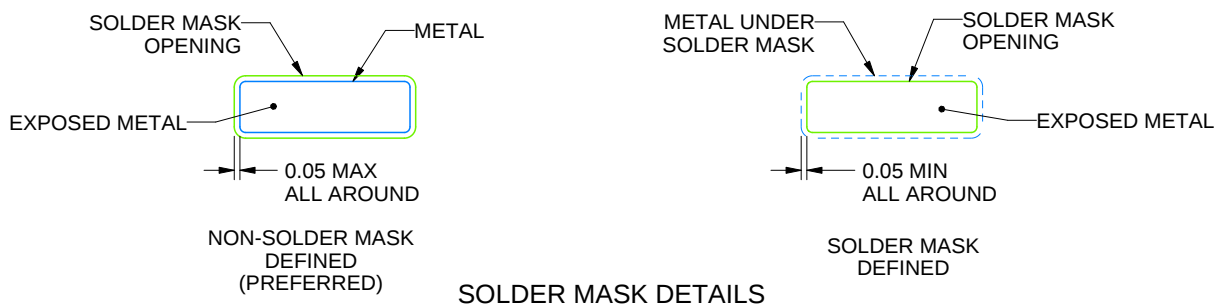
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

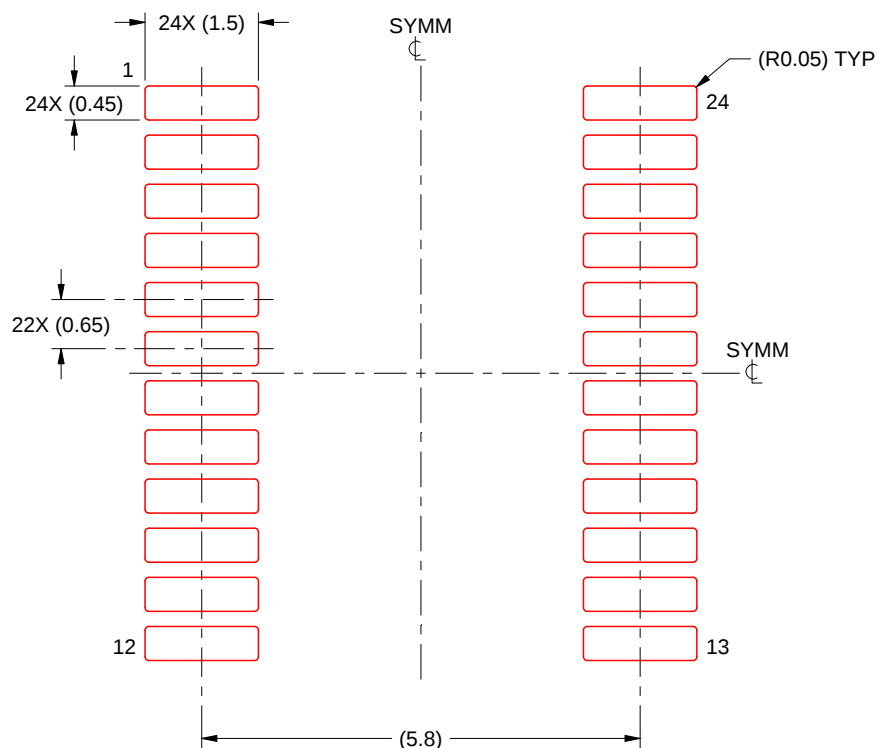
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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