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SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1748 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.11 \Omega$ ($V_{GS} = 10 V, I_D = 4 A$)
 $R_{DS(on)} = 0.16 \Omega$ ($V_{GS} = 4 V, I_D = 4 A$)
- Low C_{iss} $C_{iss} = 850 pF$ TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

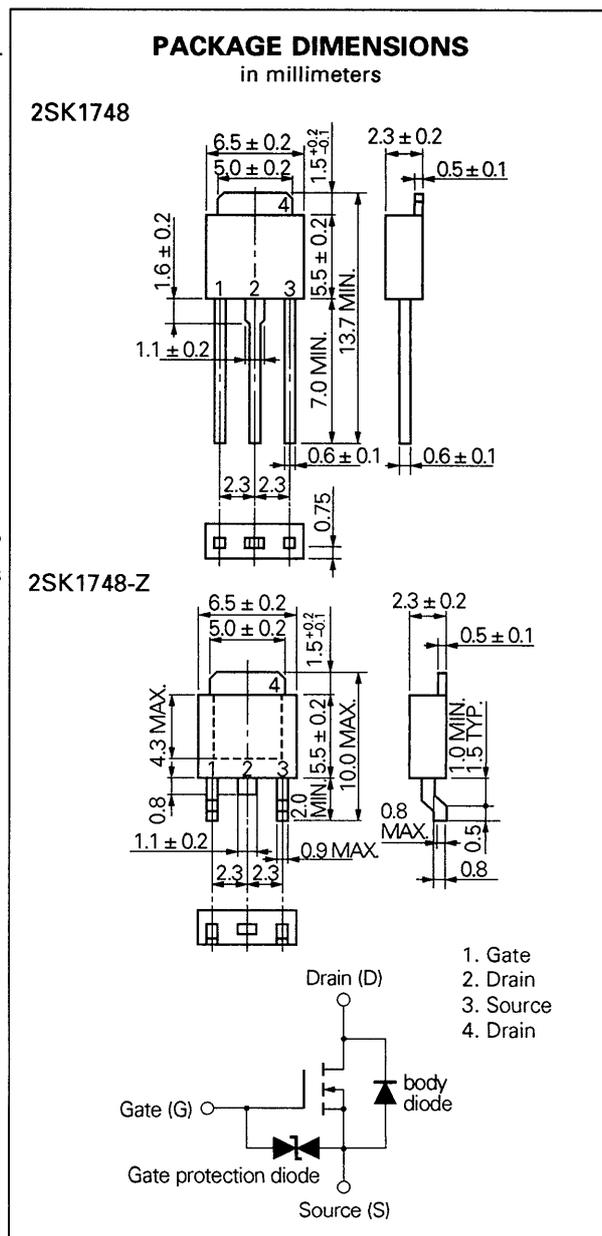
Standard

Please refer to "Quality grade on NEC Semi-conductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ C$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 8.0	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 24	A
Total Power Dissipation ($T_c = 25^\circ C$)	P_{T1}	20	W
Total Power Dissipation ($T_a = 25^\circ C$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$

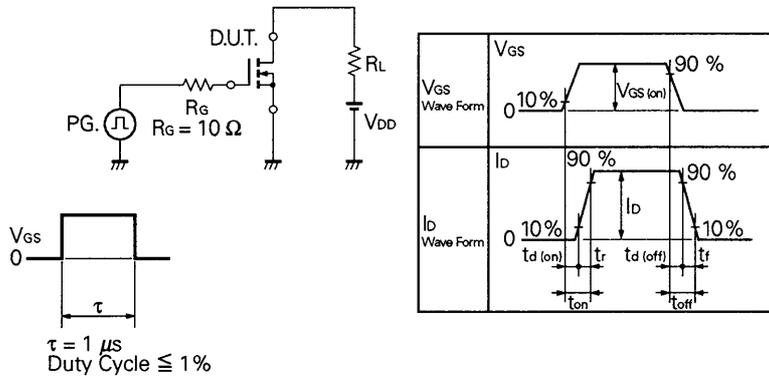
* $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$



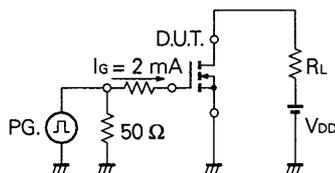
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.08	0.11	Ω	V _{GS} = 10 V, I _D = 4 A
Drain to Source On-state Resistance	R _{DS(on)}		0.11	0.16	Ω	V _{GS} = 4 V, I _D = 4 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	5.0			S	V _{DS} = 10 V, I _D = 4 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		850		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		350		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		100		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		15		ns	V _{GS(on)} = 10 V V _{DD} = 30 V I _D = 4 A, R _G = 10 Ω R _L = 7.5 Ω
Rise Time	t _r		60		ns	
Turn-Off Delay Time	t _{d(off)}		100		ns	
Fall Time	t _f		45		ns	
Total Gate Charge	Q _G		3		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		7		nC	I _D = 8 A
Gate to Drain Charge	Q _{GD}		25		nC	V _{DD} = 48 V
Reverse Recovery Time	t _{rr}		120		ns	I _F = 8 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		200		nC	di/dt = 50 A/μs

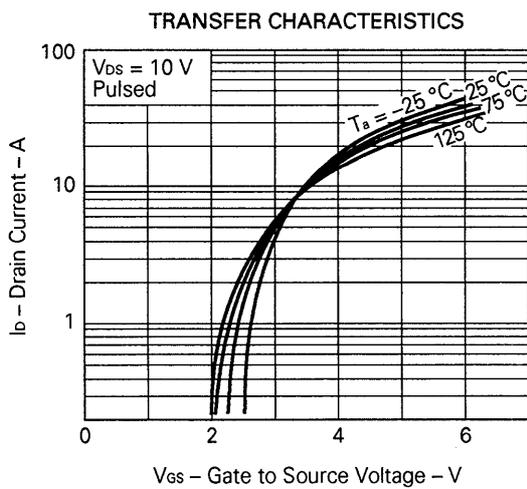
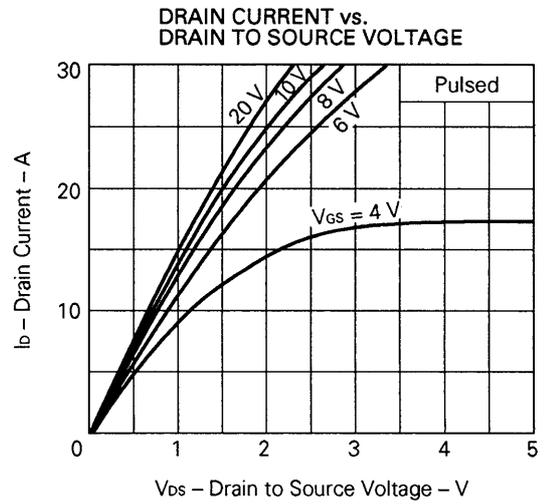
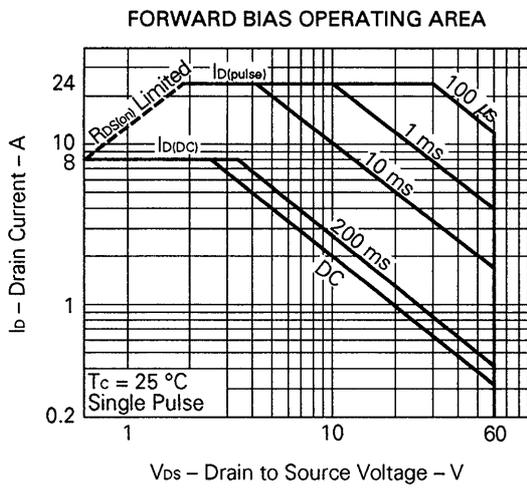
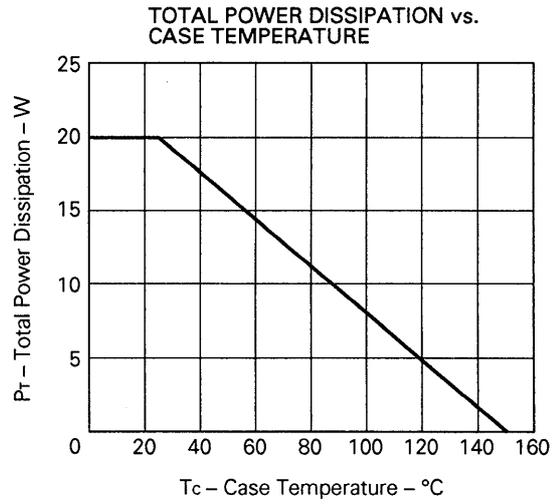
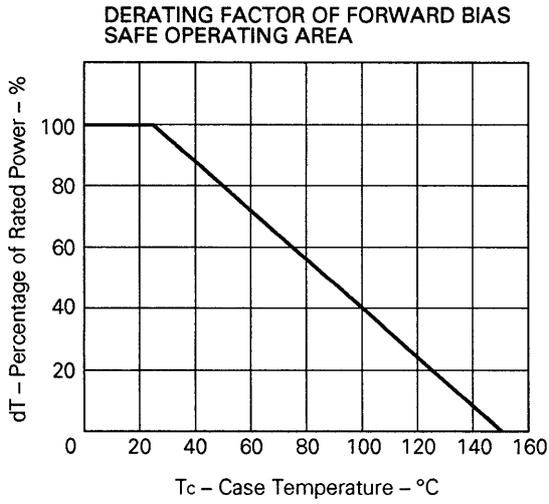
Test Circuit 1: Switching Time



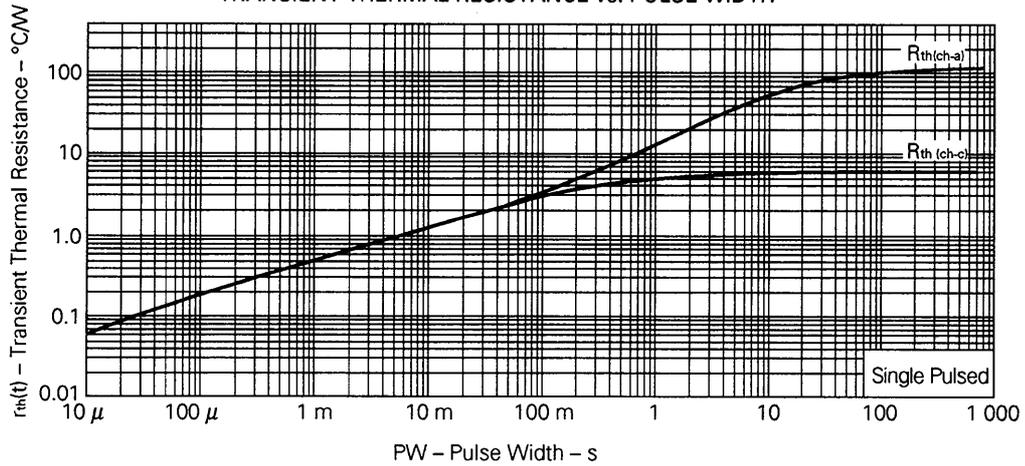
Test Circuit 2: Gate Charge



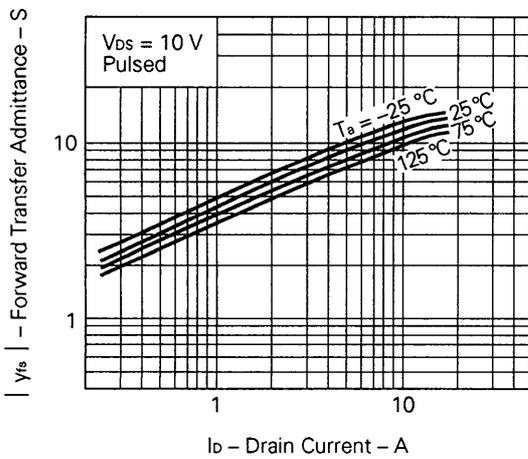
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



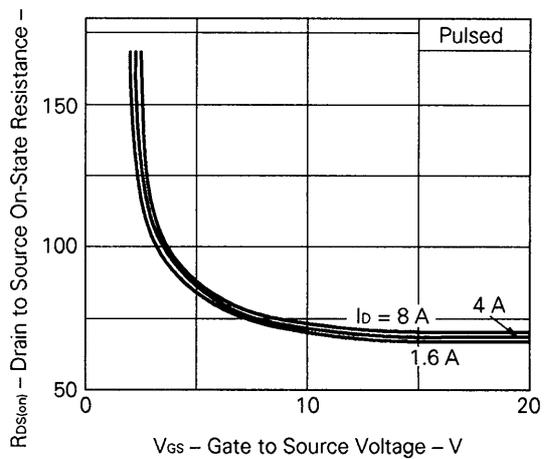
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



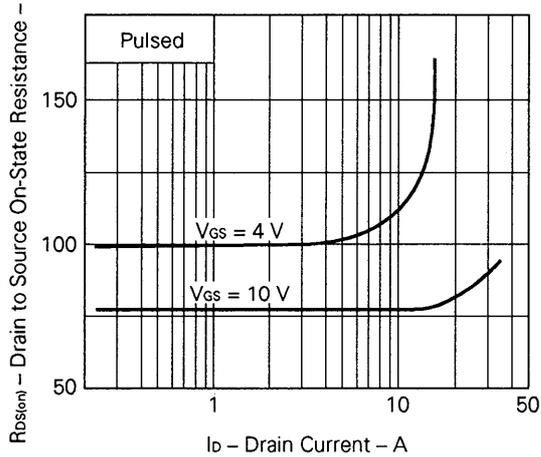
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



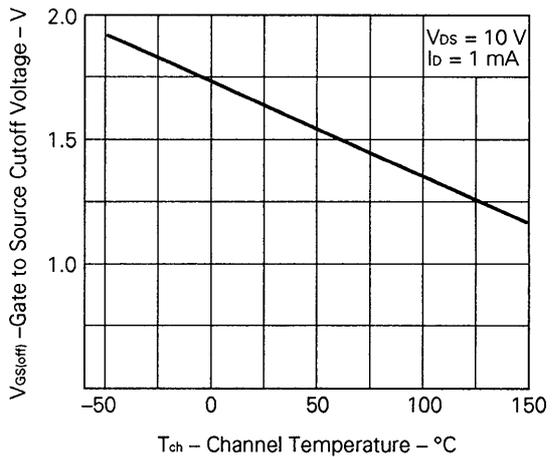
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

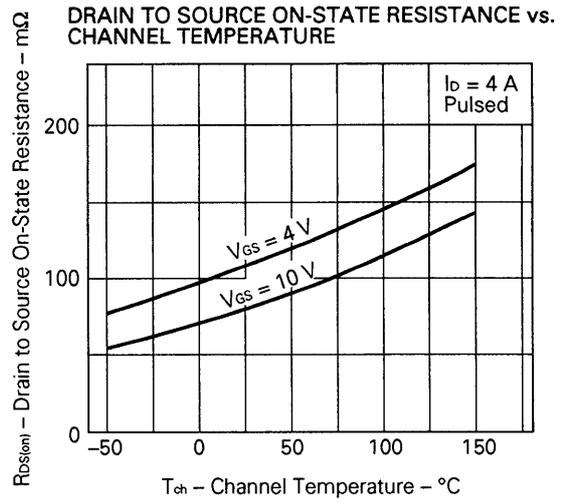
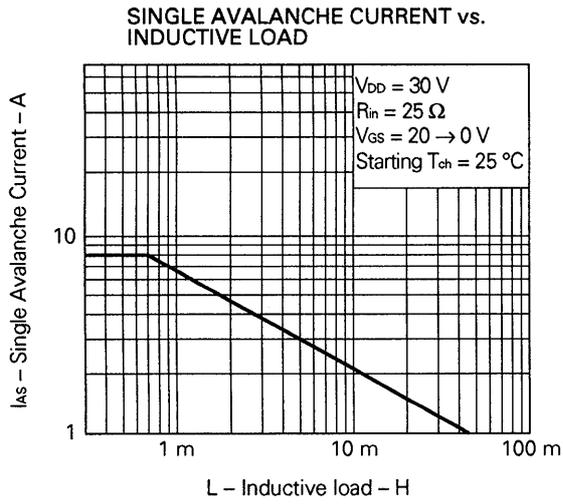


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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