

# QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1190

## 3MSPS, 12-BIT, SERIAL ADC

### LTC2360/61/62/65/66

## DESCRIPTION

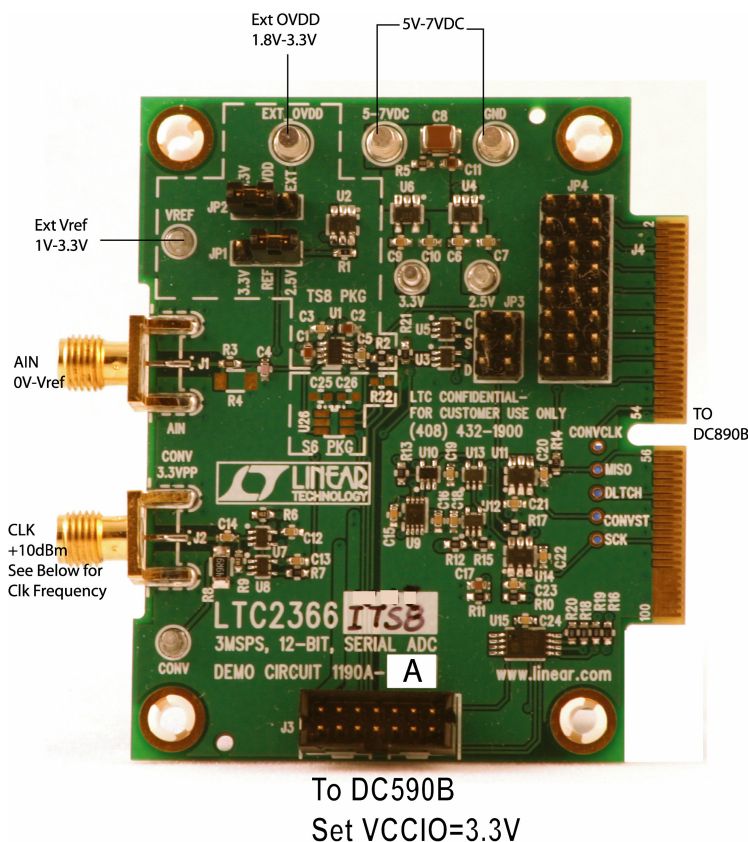
Demonstration circuit 1190 features the LTC2360 family. With up to 3MSPS these unipolar, single channel, 12-Bit, SPI compatible serial ADCs are available in 6- or 8-Lead TSOT packages. The 8-Lead package has external  $V_{REF}$  and  $OV_{DD}$  pins while the 6-pin version has  $V_{REF}$  and  $OV_{DD}$  internally connected to the  $V_{DD}$  supply pin. The following text refers to the LTC2366 but applies to all members of the family. DC1190 demonstrates the DC and AC performance of the LTC2366 in conjunction with

the DC590B Quick Eval and DC890B Fast DAACS data collection boards. Alternatively, by connecting the DC1190 into a customer application the performance of the LTC2366 can be evaluated directly in that circuit.

**Design files for this circuit board are available.  
Call the LTC factory.**

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Figure 1. DC1190A Connection Diagram



To DC590B  
Set VCCIO=3.3V

| Demo Board | IC          | Max Clk Frequency |
|------------|-------------|-------------------|
| DC1190A-A  | LTC2366ITS8 | 48MHz             |
| DC1190A-B  | LTC2365ITS8 | 16MHz             |
| DC1190A-C  | LTC2362ITS8 | 50MHz             |
| DC1190A-D  | LTC2361ITS8 | 25MHz             |
| DC1190A-E  | LTC2360ITS8 | 10MHz             |

## DC890B QUICK START PROCEDURE

Connect DC1190 to a DC890B USB High Speed Data Collection Board using connector J4. Connect DC890B to a host PC with a standard USB A/B cable. Apply 5V-7V DC to the 5-7VDC and GND terminals. Apply a low jitter signal source to J1. As a clock source, apply a low jitter 10dBm sine wave or square wave to connector J2. See table on page 1 for maximum frequencies. Note that J2 has a 50-ohm termination resistor to ground. Run the QuickEval-II software (Pscope.exe version K51 or later) supplied with DC890B or download it from

[www.linear.com](http://www.linear.com). Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added. The Pscope software should recognize DC1190 and configure itself automatically.

Click the Collect button (See Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be used to pause data acquisition.

## DC590B QUICK START PROCEDURE

Connect DC1190 to a DC590B USB serial controller using the supplied 14-conductor ribbon cable. **Make sure that VCCIO of DC590B is set to 3.3V.** Connect DC590B to a host PC with a standard USB A/B cable. Apply a signal source to J1. Run the

evaluation software supplied with DC590B or download it from [www.linear.com](http://www.linear.com). The correct control panel will be loaded automatically. Click the COLLECT (Figure 3) button to begin reading the ADC.

## HARDWARE SET UP

### SIGNAL CONNECTIONS

**J1** SMA connector for AIN. Limit input voltage swings to  $GND-V_{REF}$ . For optimum performance, the input should be bandlimited to the frequencies of interest.

**J2** Conversion Clock Input. This input has a 50-ohm termination resistor, and is intended to be driven by a low jitter, 10dBm sine or square wave. To achieve full AC performance of this part, the clock jitter should be kept under 20ps. This input is capacitively coupled so that the input clock can be either 0V-3.3V or  $\pm 1.65V$  so that level shifting is not required. To run at the maximum conversion rate, apply the frequency specified in the table on page 1.

**J3** Quick Eval interface. Connect to DC590B. **Make sure that VCCIO of DC590B is set to 3.3V.**

**J4** FastDAACS interface. Connect to DC890B. Do not connect to both DC590 and DC890 at the same time.

**VREF** External  $V_{REF}$  connection or it can also be used to monitor the internal Vref voltage. To use this pin as an external  $V_{REF}$  input remove jumper JP1.

**EXT OVDD** External  $OV_{DD}$  connection. This can be used to drive the SDO output to logic levels other than 3.3V. To use this pin put jumper JP2 in the EXT position and apply desired  $OV_{DD}$  voltage.

**JP1** Reference voltage select. Use this jumper to select the ADC reference voltage. Options include 2.5V, 3.3V or an external reference voltage can be applied by removing the jumper and applying a voltage to VREF.

**JP2**  $OV_{DD}$  select. Set  $OV_{DD}$  to 3.3V or an external voltage.

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**JP3** I/O lines for ADC. See schematic for pinout.

**JP4** Factory use only. There should be a jumper from pins 8-16 for LTC2365 and LTC2366. There should be a jumper from pins 16-24 for LTC2362, LTC2361, and LTC2360.

Do not make connections to any other pins on this connector.

### GROUNDING AND POWER CONNECTION

Connect a 5V to 7V power supply to the 5-7VDC and GND input connectors. For

optimum performance, this supply should be floating with respect to any signal generators connected to the analog input (J1)

Figure 2. DC1190 Fast DAACS Screenshot

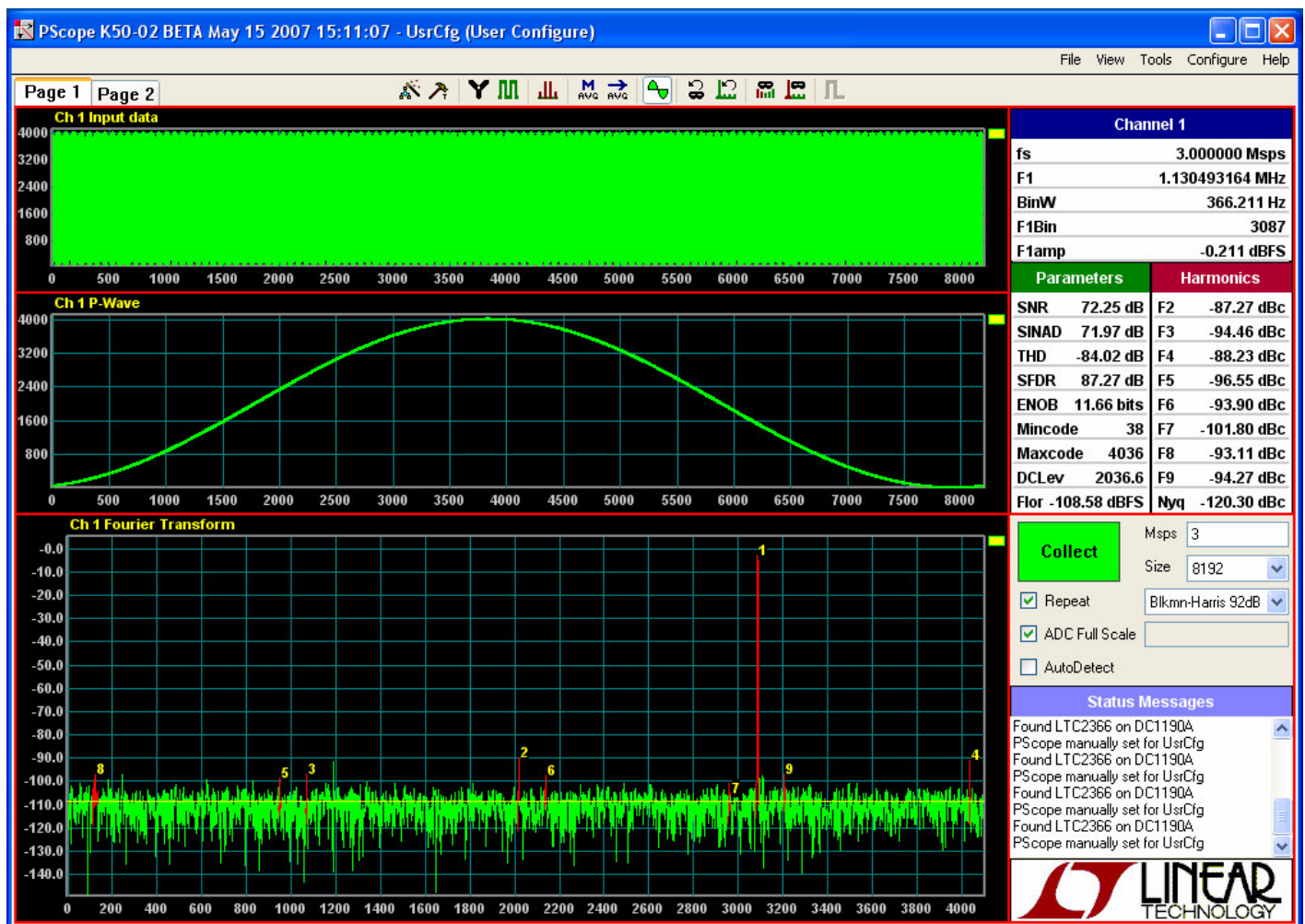
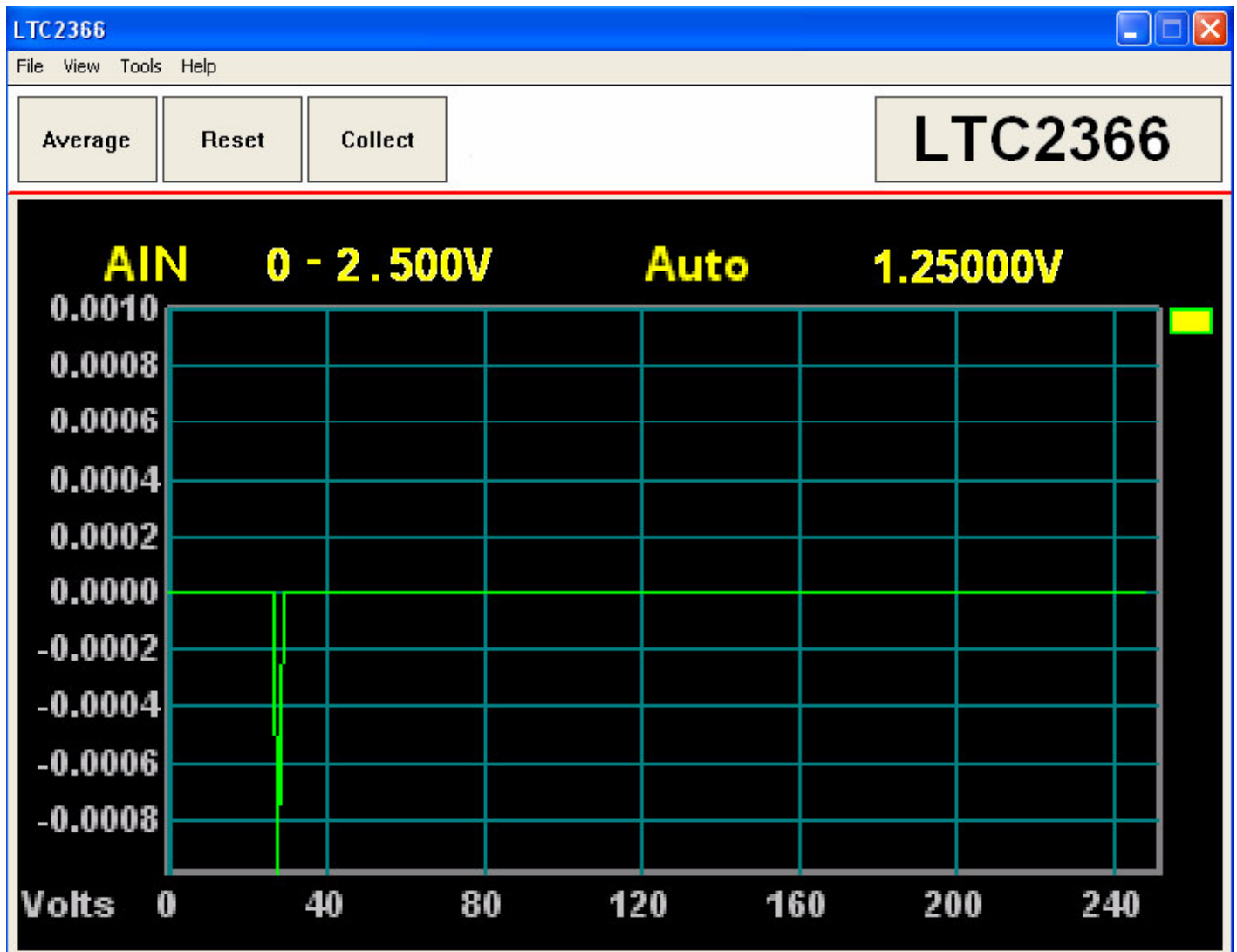


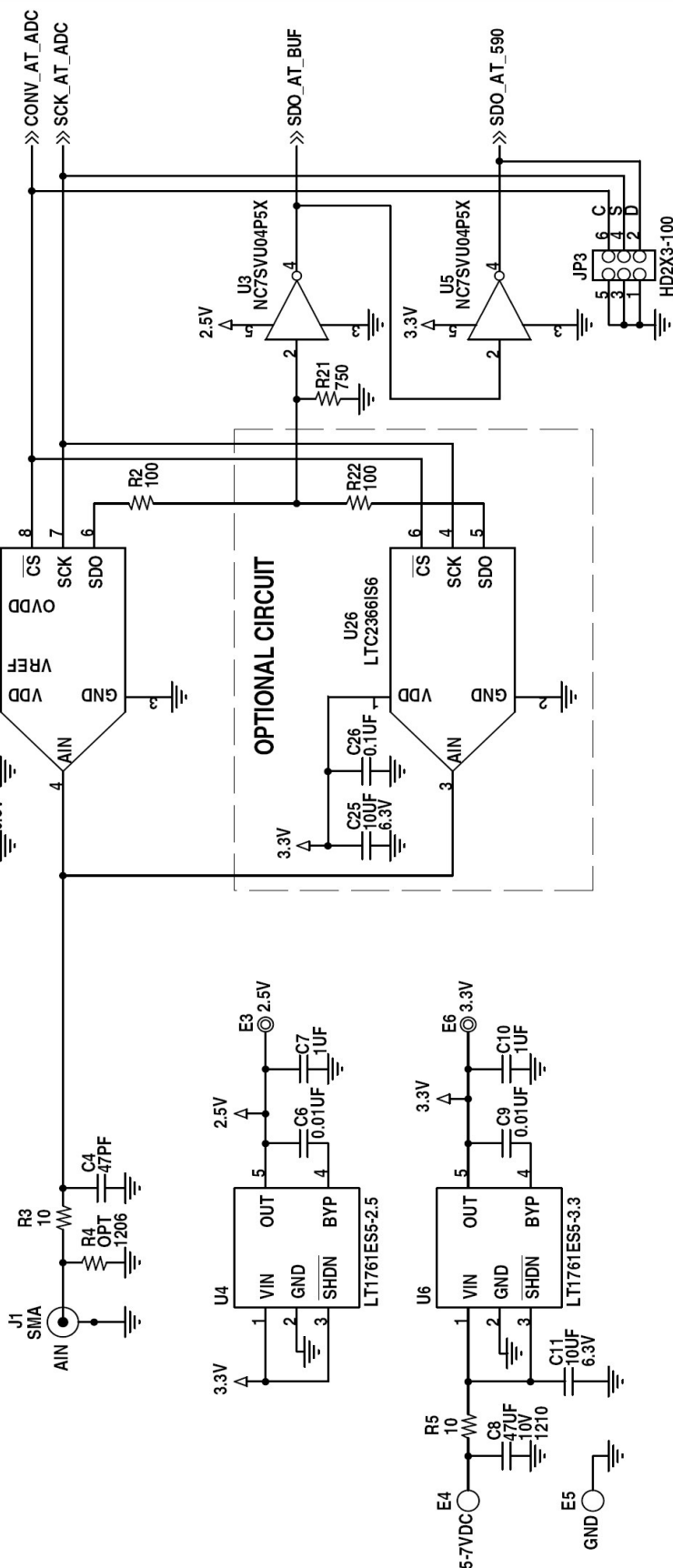
Figure 3. DC1190 Quick Eval Screenshot



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| ★ ASSY | U1          | MSPS |
|--------|-------------|------|
| -A     | LTC2366ITS8 | 3    |
| -B     | LTC2365ITS8 | 1    |
| -C     | LTC2362ITS8 | 0.5  |
| -D     | LTC2361ITS8 | 0.25 |
| -E     | LTC2360ITS8 | 0.1  |



### NOTES: UNLESS OTHERWISE SPECIFIED

- ALL RESISTORS ARE IN OHMS, 0603.  
ALL CAPACITORS ARE 0603.
- INSTALL SHUNTS ON JP1 AND JP2 PINS 2&3.

### CUSTOMER NOTICE

LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.

THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.

### CONTRACT NO.

### APPROVALS

DRAWN: KIM T.

CHECKED:

APPROVED:

ENGINEER: GUYH.

DESIGNER:



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### TITLE: SCHEMATIC

★ MSPS, 12-BIT, SERIAL ADC

SIZE

DWG NO.

REV

DC1190A-2 \* LTC2360 FAMILY

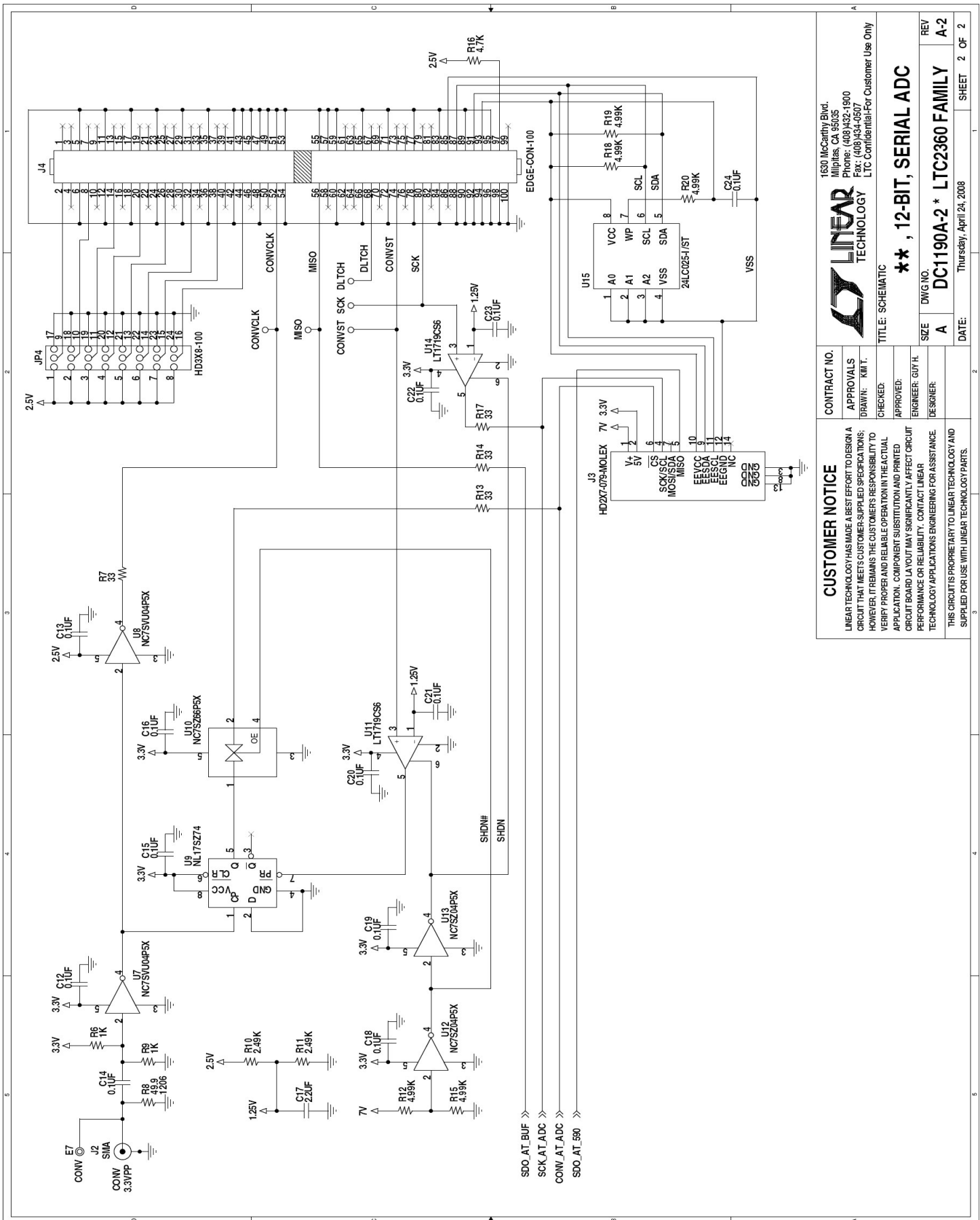
A-2

DATE: Thursday, April 24, 2008

SHEET 1 OF 2

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APPROVALS  
DRAWN: KMT  
CHECKED:  
APPROVED:  
ENGINEER: GUY H.  
DESIGNER:

### DATE:

THURSDAY, APRIL 24, 2008

### REVISION

REV A  
DC1190A-2 \* LTC2360 FAMILY  
SHEET 2 OF 2

### TITLE: SCHEMATIC

\*\*\* 12-BIT, SERIAL ADC

### LINEAR TECHNOLOGY

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