

## TC74HCT174AFN

### Hex D-Type Flip Flop with Clear

The TC74HCT174A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

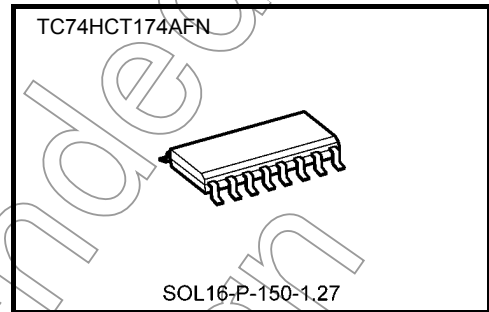
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the  $\overline{\text{CLR}}$  input is held low, the Q outputs are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Note: xxxFN (JEDEC SOP) is not available in Japan.

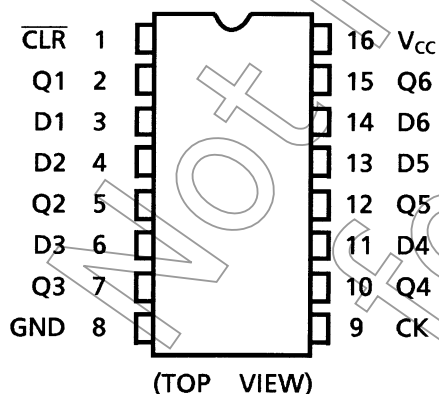


Weight  
SOL16-P-150-1.27 : 0.13 g (typ.)

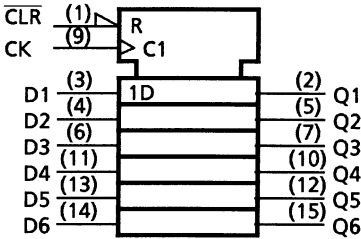
### Features

- High speed:  $f_{\text{max}} = 56 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{\text{IH}} = 2.0 \text{ V}$  (min)  
 $V_{\text{IL}} = 0.8 \text{ V}$  (max)
- Wide interfacing ability: LSTTL, NMOS, CMOS
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Pin and function compatible with 74LS174

### Pin Assignment



IEC Logic Symbol

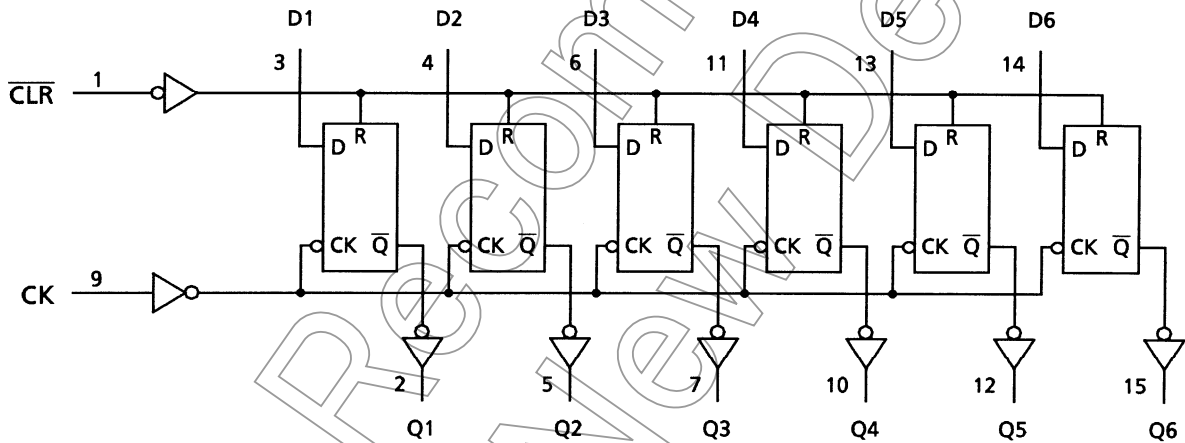


Truth Table

Inputs			Output	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q <sub>n</sub>	No Change

X: Don't care

System Diagram



**Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics****DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
High-level input voltage	VIH	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	VIL	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	VOH	VIN = VIH or VIL	IOH = -20 μA	4.5	4.4	4.5	—	4.4	—	V
			IOH = -4 mA	4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	VOL	VIN = VIH or VIL	IOL = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			IOL = 4 mA	4.5	—	0.17	0.26	—	0.33	
Input leakage current	IIN	VIN = VCC or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	ICC	VIN = VCC or GND		5.5	—	—	4.0	—	40.0	μA
	IC	Per input: VIN = 0.5 V or 2.4 V Other input: VCC or GND		5.5	—	—	2.0	—	2.9	mA

**Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (CK)	$t_W$ (L)	—	4.5	—	15	ns
	$t_W$ (H)		5.5	—	14	
Minimum pulse width ( $\overline{\text{CLR}}$ )	$t_W$ (L)	—	4.5	—	15	ns
			5.5	—	14	
Minimum set-up time	$t_s$	—	4.5	—	20	ns
			5.5	—	18	
Minimum hold time	$t_h$	—	4.5	—	5	ns
			5.5	—	5	
Minimum removal time ( $\overline{\text{CLR}}$ )	$t_{\text{rem}}$	—	4.5	—	10	ns
			5.5	—	10	
Clock frequency	f	—	4.5	—	30	MHz
			5.5	—	33	

**AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{\text{TLH}}$	—	—	12	15	ns
	$t_{\text{THL}}$					
Propagation delay time (CK-Q)	$t_{\text{PLH}}$	—	—	29	36	ns
	$t_{\text{PHL}}$					
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	$t_{\text{pHL}}$	—	—	29	36	ns
Maximum clock frequency	$f_{\text{max}}$	—	32	61	—	MHz

## AC Characteristics (C<sub>L</sub> = 50 pF, input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max
Output transition time	t <sub>TLH</sub>	—	4.5	—	8	15	—	19
	t <sub>THL</sub>		5.5	—	7	14	—	18
Propagation delay time (CK-Q)	t <sub>pLH</sub>	—	4.5	—	20	34	—	43
	t <sub>pHL</sub>		5.5	—	17	31	—	39
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	t <sub>pHL</sub>	—	4.5	—	20	34	—	43
			5.5	—	17	31	—	39
Maximum clock frequency	f <sub>max</sub>	—	4.5	30	54	—	24	—
			5.5	33	57	—	26	—
Input capacitance	C <sub>IN</sub>	—	—	—	5	10	—	10
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	—	30	—	—	—

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

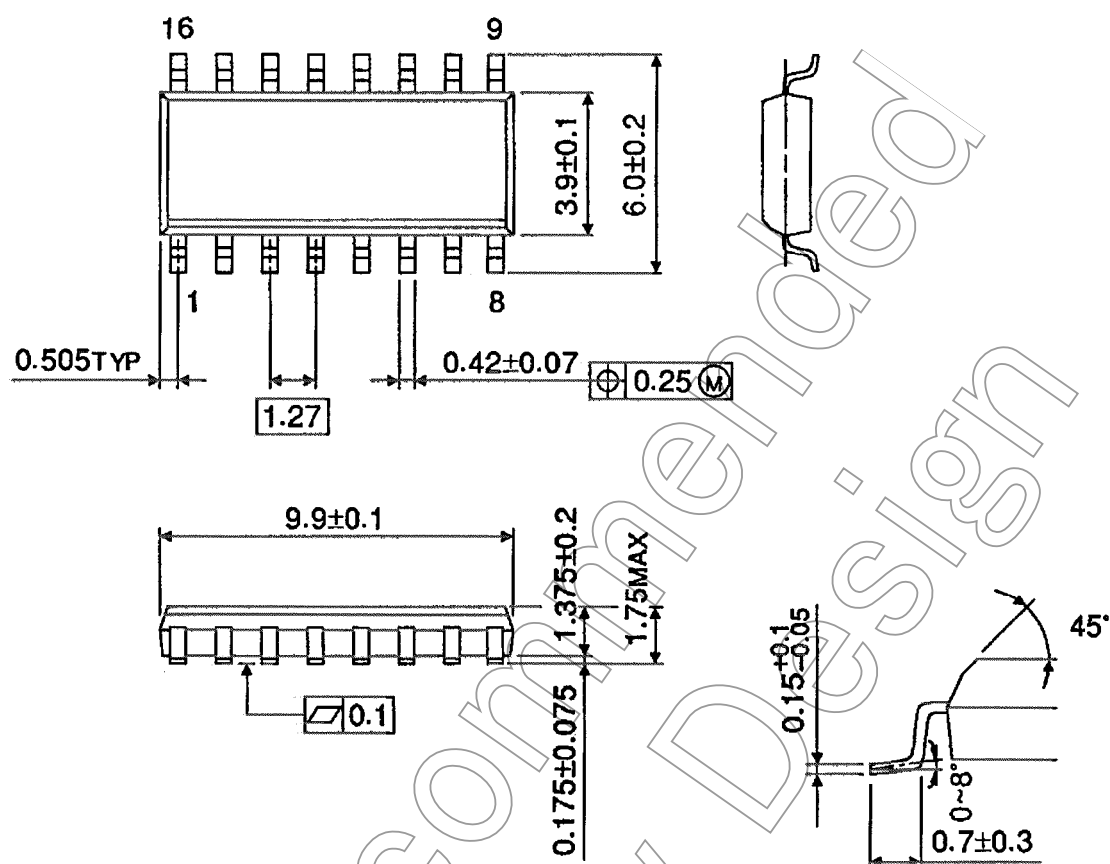
And the total C<sub>PD</sub> when n pcs. of flip flop operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 18 + 12 \cdot n$$

## Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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