

MAXIM**+2.7V to +5.5V, Low-Power, Dual, Parallel
8-Bit DAC with Rail-to-Rail Voltage Outputs****General Description**

The MAX5102 parallel-input, voltage-output, dual 8-bit digital-to-analog converter (DAC) operates from a single +2.7V to +5.5V supply and comes in a space-saving 16-pin TSSOP package. Internal precision buffers swing Rail-to-Rail®, and the reference input range includes both ground and the positive rail. Both DACs share a common reference input.

The MAX5102 has separate input latches for each of its DACs. Data is transferred to the input latches from a common 8-bit input port. The DACs are individually selected through address input A0 and are updated by bringing \overline{WR} low.

The MAX5102 features a shutdown mode that reduces current to 1nA, as well as a power-on reset mode that resets all registers to code 00 hex on power-up.

Applications

Digital Gain and Offset Adjustment

Programmable Attenuators

Portable Instruments

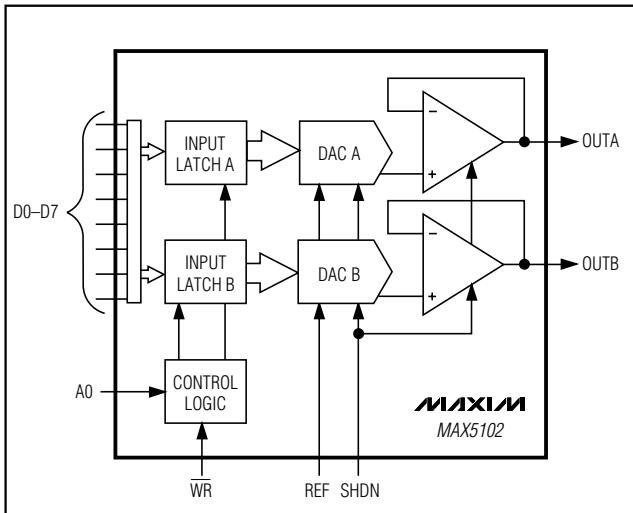
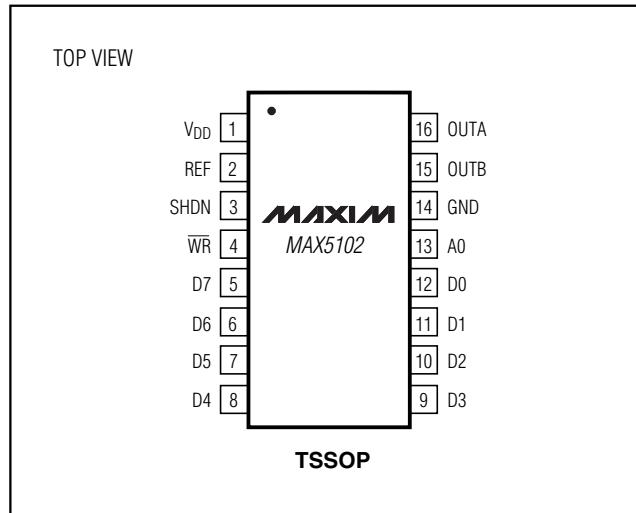
Power-Amp Bias Control

Features

- ◆ +2.7V to +5.5V Single-Supply Operation
- ◆ Ultra-Low Supply Current
0.2mA while Operating
1nA in Shutdown Mode
- ◆ Ultra-Small 16-Pin TSSOP Package
- ◆ Ground to V_{DD} Reference Input Range
- ◆ Output Buffer Amplifiers Swing Rail-to-Rail
- ◆ Power-On Reset Sets All Registers to Zero

MAX5102**Ordering Information**

| PART | TEMP. RANGE | PIN-PACKAGE | INL (LSB) |
|-------------|----------------|-------------|-----------|
| MAX5102AEUE | -40°C to +85°C | 16 TSSOP | ±1 |
| MAX5102BEUE | -40°C to +85°C | 16 TSSOP | ±2 |

Functional Diagram**Pin Configuration**

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

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ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{DD} to GND | -0.3V to +6V |
| D _l , A ₀ , WR, SHDN to GND | -0.3V to +6V |
| REF to GND | -0.3V to (V _{DD} + 0.3V) |
| OUT _l to GND | -0.3V to V _{DD} |
| Maximum Current into Any Pin | ±50mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| 16-Pin TSSOP (derate 5.7mW/°C above +70°C) | 457mW |

| | |
|-------------------------------------|-----------------|
| Operating Temperature Range | |
| MAX5102_EUE | -40°C to +85°C |
| Maximum Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10sec) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{REF} = +2.7V to +5.5V, GND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = V_{REF} = +3V and T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|------------------------------------|-----------------|---|--|--------|------------------|-----|--------|
| STATIC ACCURACY | | | | | | | |
| Resolution | | | | | 8 | | Bits |
| Integral Nonlinearity (Note 1) | INL | MAX5102A | | | ±1 | | LSB |
| | | MAX5102B | | | ±2 | | |
| Differential Nonlinearity (Note 1) | DNL | Guaranteed monotonic | | | ±1 | | LSB |
| Zero-Code Error | ZCE | Code = 00 hex | | | ±20 | | mV |
| Zero-Code-Error Supply Rejection | | Code = 00 hex, V _{DD} = 2.7V to 5.5V | | | 10 | | mV |
| Zero-Code Temperature Coefficient | | Code = 00 hex | | | ±10 | | µV/°C |
| Gain Error (Note 2) | | Code = F0 hex | | | ±1 | | % |
| Gain-Error Temperature Coefficient | | Code = F0 hex | | ±0.001 | | | LSB/°C |
| Power-Supply Rejection | | Code = FF hex | V _{DD} = 2.7V to 3.6V, V _{REF} = 2.5V | | 1 | | LSB |
| | | | V _{DD} = 4.5V to 5.5V, V _{REF} = 4.096V | | 1 | | |
| REFERENCE INPUT | | | | | | | |
| Input Voltage Range | | | | 0 | V _{DD} | | V |
| Input Resistance | | | | 320 | 460 | 600 | kΩ |
| Input Capacitance | | | | 15 | | | pF |
| DAC OUTPUTS | | | | | | | |
| Output Voltage Range | | R _L = ∞ | | 0 | V _{REF} | | V |
| DIGITAL INPUTS | | | | | | | |
| Input High Voltage | V _{IH} | V _{DD} = 2.7V to 3.6V | | 2 | | | V |
| | | V _{DD} = 3.6V to 5.5V | | 3 | | | |
| Input Low Voltage | V _{IL} | | | | 0.8 | | V |
| Input Current | I _{IN} | V _{IN} = V _{DD} or GND | | | ±1.0 | | µA |
| Input Capacitance | C _{IN} | | | 10 | | | pF |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = V_{REF} = +2.7V$ to $+5.5V$, $GND = 0V$, $R_L = 10k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{DD} = V_{REF} = +3V$ and $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------|--|-------|-----|-----|------------------------|
| DYNAMIC PERFORMANCE | | | | | | |
| Output Voltage Slew Rate | | From code 00 to code F0 hex | 0.6 | | | V/ μ s |
| Output Settling Time (Note 3) | | To $\pm 1/2$ LSB, from code 00 to code F0 hex | 6 | | | μ s |
| Channel-to-Channel Isolation (Note 4) | | Code 00 to code FF hex | 500 | | | nVs |
| Digital Feedthrough (Note 5) | | Code 00 to code FF hex | 0.5 | | | nVs |
| Digital-to-Analog Glitch Impulse | | Code 80 hex to code 7F hex | 90 | | | nVs |
| Signal-to-Noise plus Distortion Ratio | SINAD | REF = 2.5Vp-p at 1kHz, $V_{REF(DC)} = 1.5V$, $V_{DD} = 3V$, code FF hex | 70 | | | dB |
| | | REF = 2.5Vp-p at 10kHz, $V_{REF(DC)} = 1.5V$, $V_{DD} = 3V$, code FF hex | 60 | | | |
| Multiplying Bandwidth | | REF = 0.5Vp-p, $V_{REF(DC)} = 1.5V$, $V_{DD} = 3V$, -3dB bandwidth | 650 | | | kHz |
| Wideband Amplifier Noise | | | 60 | | | μ V _{RMS} |
| Shutdown Recovery Time | t _{SDR} | To $\pm 1/2$ LSB of final value of V _{OUT} | 13 | | | μ s |
| Time to Shutdown | t _{SDN} | $I_{DD} < 5\mu A$ | 20 | | | μ s |
| POWER SUPPLIES | | | | | | |
| Power-Supply Voltage | V _{DD} | | 2.7 | 5.5 | | V |
| Supply Current (Note 6) | I _{DD} | | 190 | 360 | | μ A |
| Shutdown Current | | | 0.001 | 1 | | μ A |
| DIGITAL TIMING (Figure 1) (Note 7) | | | | | | |
| Address to WR Setup | t _{AS} | | 5 | | | ns |
| Address to WR Hold | t _{AH} | | 0 | | | ns |
| Data to WR Setup | t _{DS} | | 25 | | | ns |
| Data to WR Hold | t _{DH} | | 0 | | | ns |
| WR Pulse Width | t _{WR} | | 20 | | | ns |

Note 1: Reduced digital code range (code 00 hex to code F0 hex) due to swing limitations when the output amplifier is loaded.

Note 2: Gain error is: $[100 (V_{F0,meas} - V_{F0,ideal}) / V_{REF}]$. Where $V_{F0,meas}$ is the DAC output voltage with input code F0 hex, and $V_{F0,ideal}$ is the ideal DAC output voltage with input code F0 hex (i.e., $V_{REF} \cdot 240 / 256$).

Note 3: Output settling time is measured from the 50% point of the falling edge of WR to $\pm 1/2$ LSB of V_{OUT}'s final value.

Note 4: Channel-to-channel isolation is defined as the glitch energy at a DAC output in response to a full-scale step change on any other DAC output. The measured channel has a fixed code of 80 hex.

Note 5: Digital feedthrough is defined as the glitch energy at any DAC output in response to a full-scale step change on all eight data inputs with WR at V_{DD}.

Note 6: $R_L = \infty$, digital inputs at GND or V_{DD}.

Note 7: Timing measurement reference level is $(V_{IH} + V_{IL}) / 2$.

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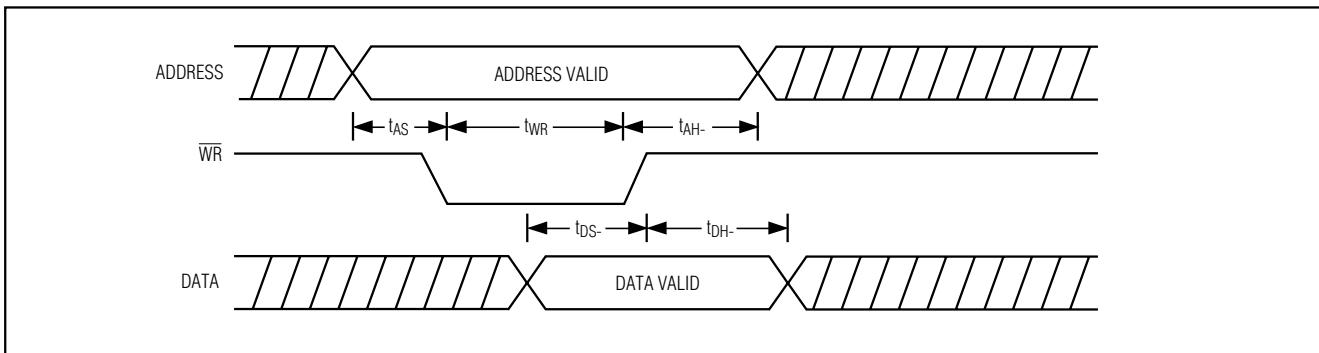
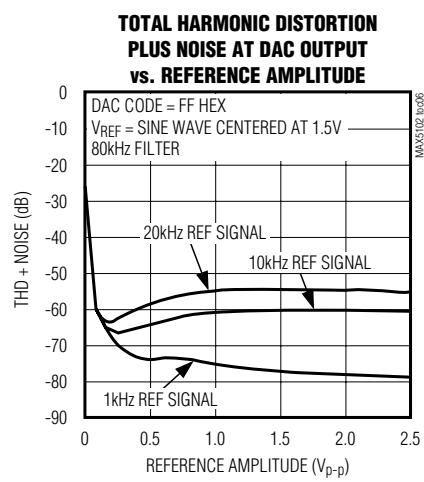
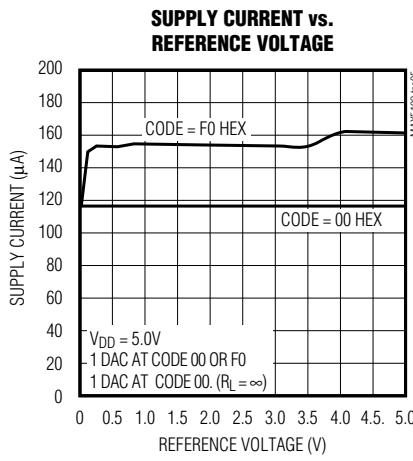
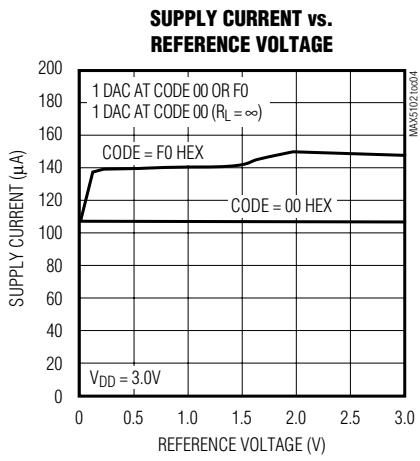
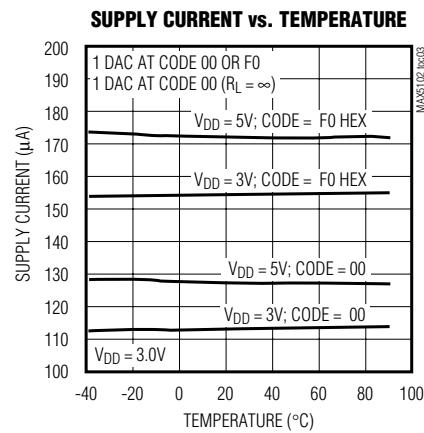
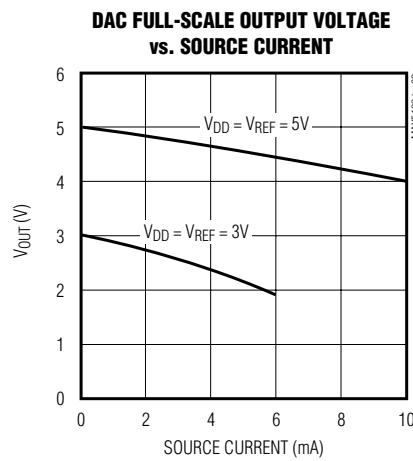
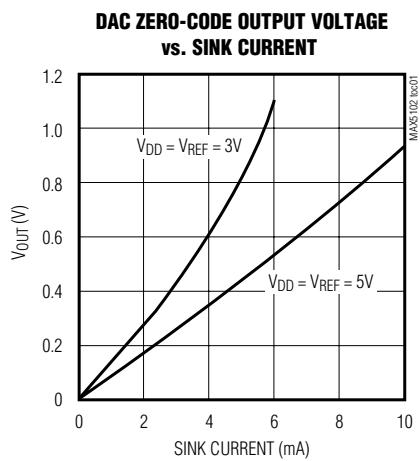


Figure 1. Timing Diagram

Typical Operating Characteristics

($V_{DD} = V_{REF} = +3V$, $R_L = 10k\Omega$, $C_L = 100pF$, code = FF hex, $T_A = +25^\circ C$, unless otherwise noted.)

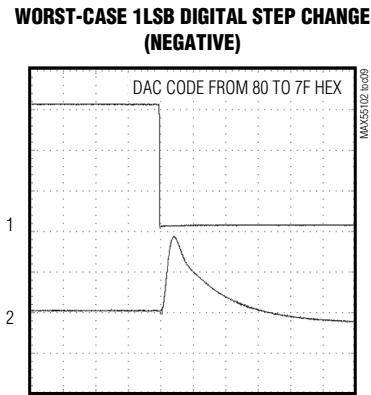
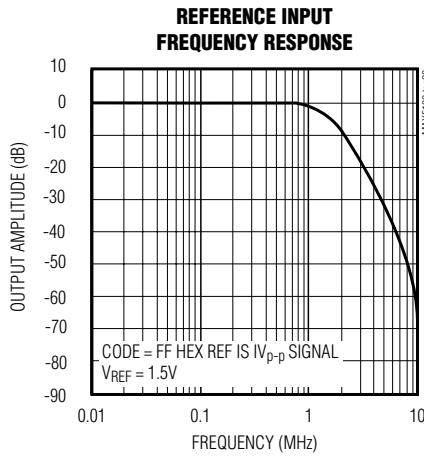
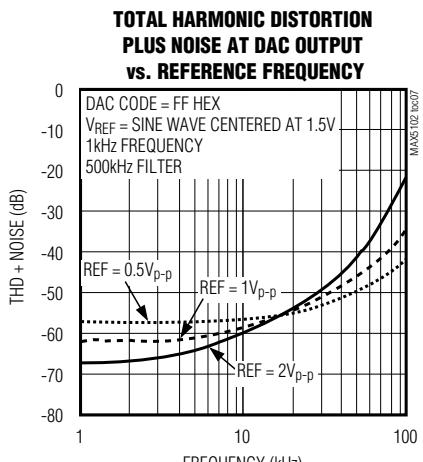


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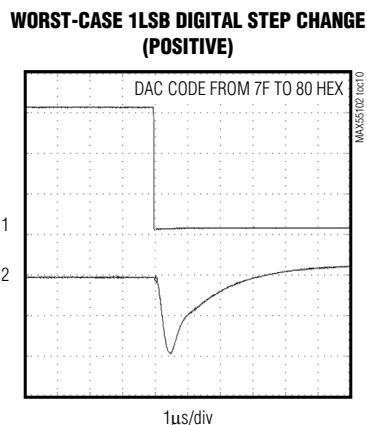
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Typical Operating Characteristics (continued)

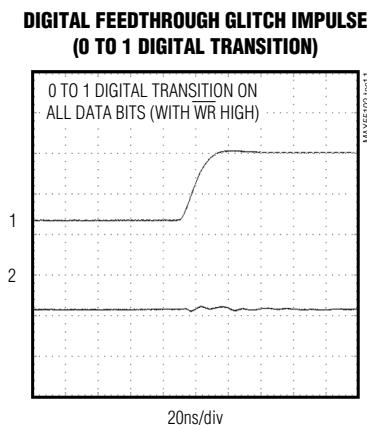
($V_{DD} = V_{REF} = +3V$, $R_L = 10k\Omega$, $C_L = 100pF$, code = FF hex, $T_A = +25^\circ C$, unless otherwise noted.)



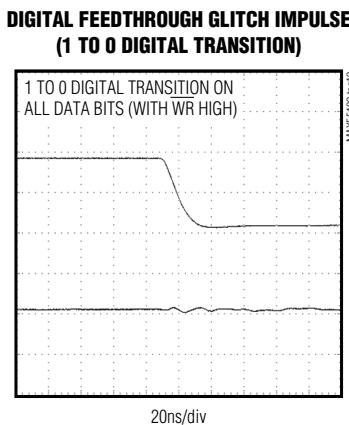
CH1 = \overline{WR} , 1V/div, CH2 = V_{OUTA} , 50mV/div, AC-COUPLED



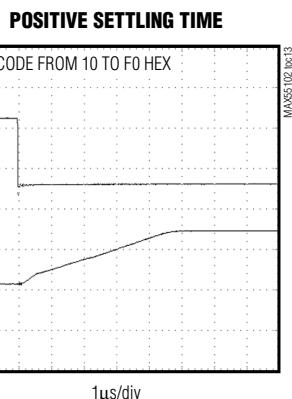
CH1 = \overline{WR} , 1V/div, CH2 = V_{OUTA} , 50mV/div, AC-COUPLED



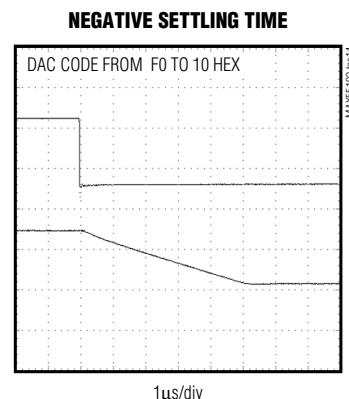
CH1 = D7, 2V/div, CH2 = V_{OUTA} , 1mV/div



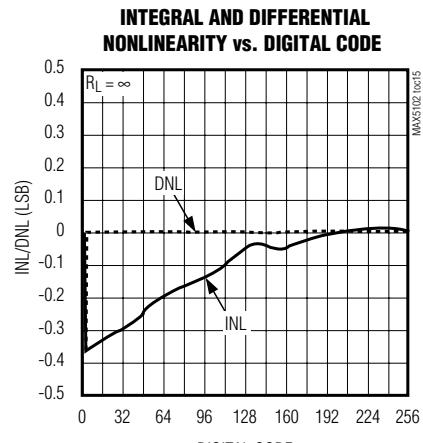
CH1 = D7, 2V/div, CH2 = V_{OUTA} , 1mV/div



CH1 = \overline{WR} = 2V/div, CH2 = V_{OUTA} = 2V/div



CH1 = \overline{WR} , 2V/div, CH2 = V_{OUTA} , 2V/div



+2.7V to +5.5V, Low-Power, Dual, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

Pin Description

| PIN | NAME | FUNCTION |
|------|-----------------|---|
| 1 | V _{DD} | Positive Supply Voltage. Bypass V _{DD} to GND using a 0.1 μ F capacitor. |
| 2 | REF | Reference Voltage Input |
| 3 | SHDN | Shutdown. Connect SHDN to GND for normal operation. |
| 4 | \overline{WR} | Write Input (active low). Use \overline{WR} to load data into the DAC input latch selected by A0. |
| 5–12 | D7–D0 | Data Inputs |
| 13 | A0 | DAC Address Select Bit |
| 14 | GND | Ground |
| 15 | OUTB | DAC B Voltage Output |
| 16 | OUTA | DAC A Voltage Output |

Detailed Description

Digital-to-Analog Section

The MAX5102 uses a matrix decoding architecture for the DACs. The external reference voltage is divided down by a resistor string placed in a matrix fashion. Row and column decoders select the appropriate tab from the resistor string to provide the needed analog voltages. The resistor network converts the 8-bit digital input into an equivalent analog output voltage in proportion to the applied reference voltage input. The resistor string presents a code-independent input impedance to the reference and guarantees a monotonic output.

These devices can be used in multiplying applications. Their voltages are buffered by rail-to-rail op amps connected in a follower configuration to provide a rail-to-rail output (see *Functional Diagram*).

Low-Power Shutdown Mode

The MAX5102 features a shutdown mode that reduces current consumption to 1nA. A high voltage on the SHDN pin shuts down the DACs and the output amplifiers. In shutdown mode, the output amplifiers enter a high-impedance state. When bringing the device out of shutdown, allow 13 μ s for the output to stabilize.

Output Buffer Amplifiers

The DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/ μ s. The typical settling time to $\pm 1/2$ LSB at the output is 6 μ s when loaded with 10k Ω in parallel with 100pF.

Reference Input

The MAX5102 provides a code-independent input impedance on the REF input. Input impedance is typically 460k Ω in parallel with 15pF, and the reference input voltage range is 0 to V_{DD}. The reference input accepts positive DC signals, as well as AC signals with peak values between 0 and V_{DD}. The voltage at REF sets the full-scale output voltage for the DAC. The output voltage (V_{OUT}) for any DAC is represented by a digitally programmable voltage source as follows:

$$V_{OUT} = (N_B \cdot V_{REF}) / 256$$

where N_B is the numeric value of the DAC binary input code.

Digital Inputs and Interface Logic

In the MAX5102, address line A0 selects the DAC that receives data from D0–D7, as shown in Table 1. When WR is low, the addressed DAC's input latch is transparent. Data is latched when WR is high. The DAC outputs (OUTA, OUTB) represent the data held in the two 8-bit

Table 1. MAX5102 Addressing Table (partial list)

| WR | A0 | LATCH STATE |
|----|----|-------------------------------|
| H | X | Input data latched |
| L | L | DAC A input latch transparent |
| L | H | DAC B input latch transparent |

H = High state, L = Low state, X = Don't care

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input latches. To avoid output glitches in the MAX5102, ensure that data is valid before WR goes low. When the device powers up (i.e., VDD ramps up), all latches are internally preset with code 00 hex.

Applications Information

External Reference

The reference source resistance must be considerably less than the reference input resistance. To keep within 1LSB error in an 8-bit system, R_S must be less than $R_{REF}/256$. Hence, maintain a value of $R_S < 1\text{k}\Omega$ to ensure 8-bit accuracy. If VREF is DC only, bypass REF to GND with a $0.1\mu\text{F}$ capacitor. Values greater than this improve noise rejection.

Power Sequencing

The voltage applied to REF should not exceed VDD at any time. If proper power sequencing is not possible,

connect an external Schottky diode between REF and VDD to ensure compliance with the absolute maximum ratings. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

Digital or AC transient signals on GND can create noise at the analog output. Return GND to the highest-quality ground available. Bypass VDD with a $0.1\mu\text{F}$ capacitor, located as close to VDD and GND as possible.

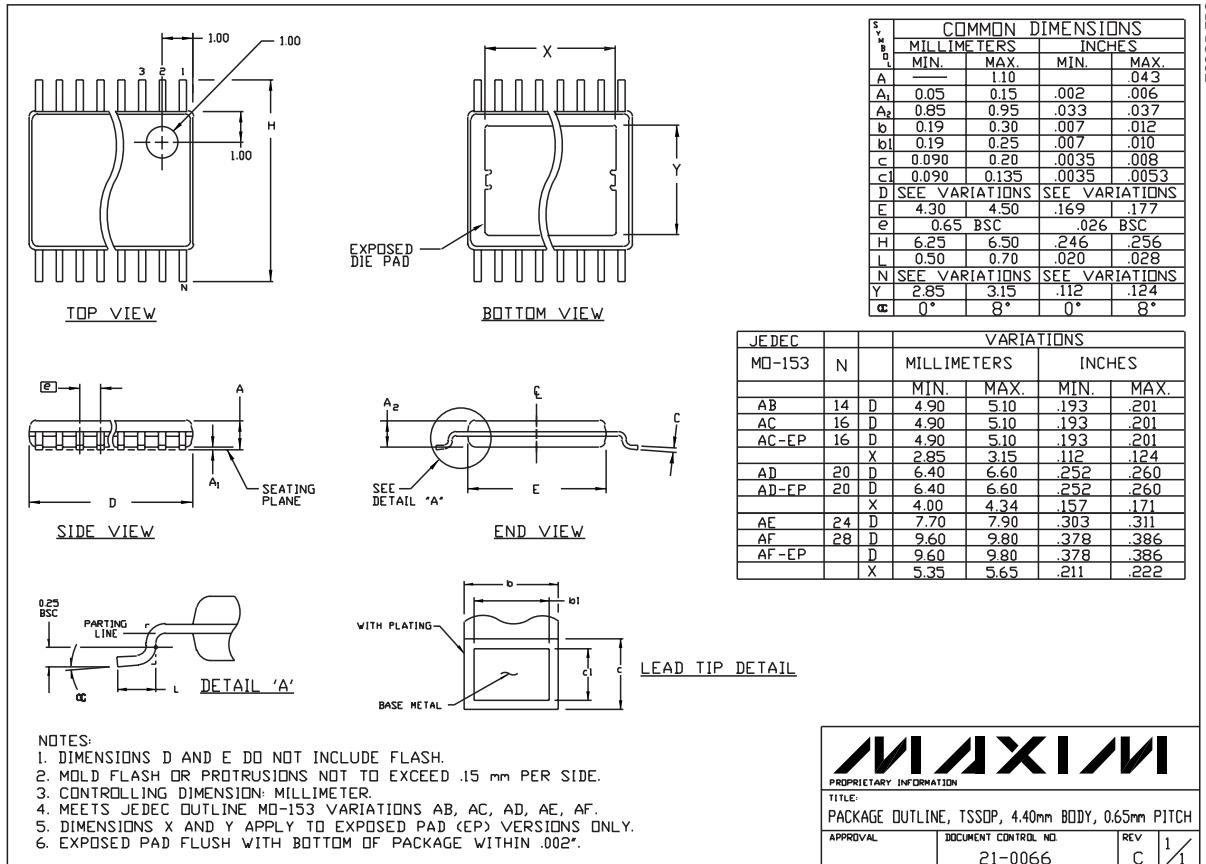
Careful PC board ground layout minimizes crosstalk between the DAC outputs and digital inputs.

Chip Information

TRANSISTOR COUNT: 6848

+2.7V to +5.5V, Low-Power, Dual, Parallel 8-Bit DAC with Rail-to-Rail Voltage Outputs

Package Information



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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