



FAN7602

Green Current Mode PWM Controller

Features

- Green Current Mode PWM Control
- Fixed 65kHz Operation with Frequency Modulation
- Internal High-Voltage Start-up Switch
- Burst Mode Operation
- Line Voltage Feed Forward to Limit Maximum Power
- Line Under-Voltage Protection
- Latch Protection & Internal Soft-Start (10ms) Function
- Overload Protection
- Over-Voltage Protection
- Low Operation Current: Typical 1mA
- 8-pin DIP/SOP

Applications

- Adapter
- LCD Monitor Power
- Auxiliary Power Supply

Related Application Notes

- **AN6014** - Green Current Mode PWM Controller FAN7602

Description

The FAN7602 is a green current mode PWM controller. It is specially designed for off-line adapter application, DVD, VCR, LCD monitor application, and auxiliary power supplies.

The internal high-voltage start-up switch and the burst-mode operation reduce the power loss in standby mode. Because of the internal start-up switch and the burst mode, it is possible to supply 0.5W load, limiting the input power to under 1W when the input line voltage is 265V_{AC}. On no-load condition, the input power is under 0.3W.

The maximum power can be limited constantly, regardless of the line voltage change, using the power limit function.

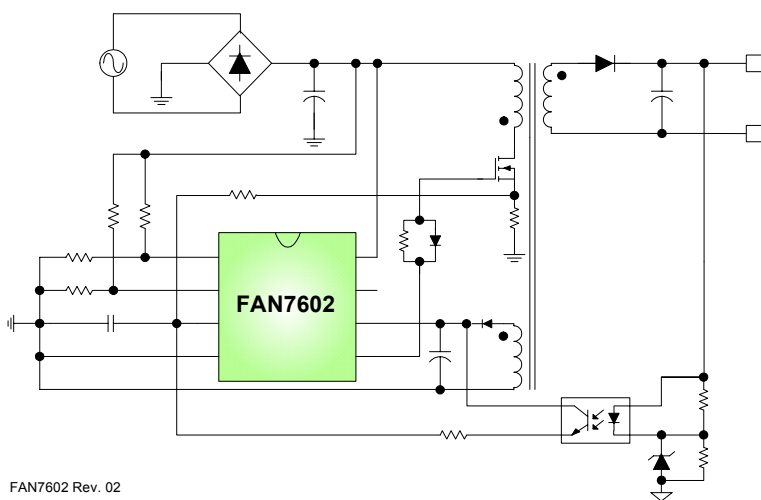
The switching frequency is internally fixed at 65kHz and the frequency modulation technique reduces EMI.

The FAN7602 includes various protections for the system reliability and the internal soft-start prevents the output voltage overshoot at start-up.

Ordering Information

| Part Number | Operating Temp. Range | Pb-Free | Package | Packing Method | Marking Code |
|-------------|-----------------------|---------|---------|----------------|--------------|
| FAN7602N | -25°C to +125°C | Yes | 8-DIP | Rail | FAN7602 |
| FAN7602M | | | 8-SOP | Rail | FAN7602 |
| FAN7602MX | | | | Tape & Reel | FAN7602 |

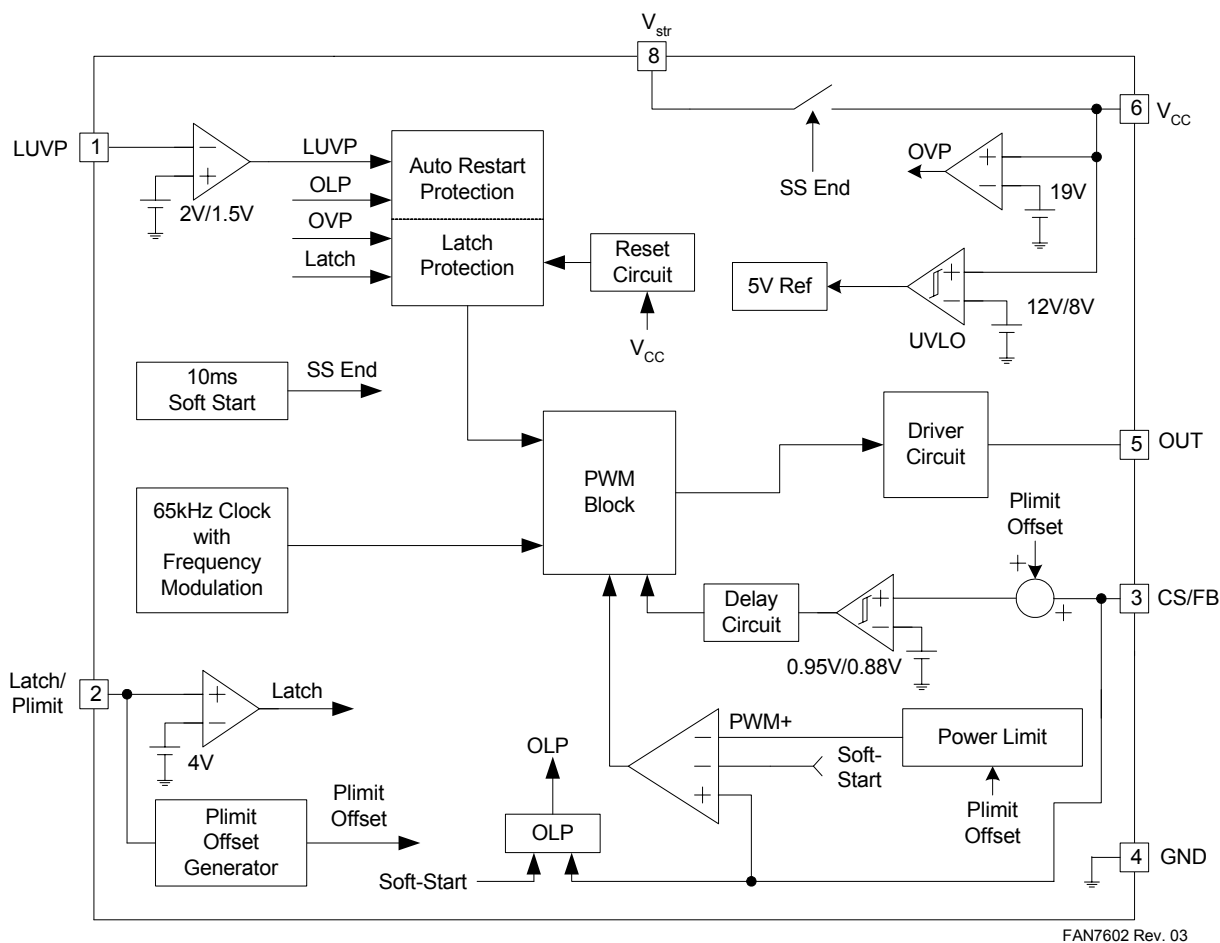
Typical Application Diagram



FAN7602 Rev. 02

Figure 1. Typical Flyback Application

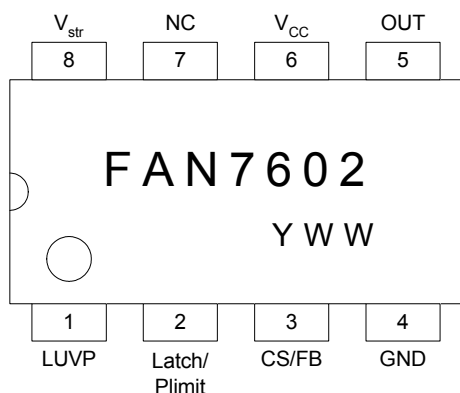
Internal Block Diagram



FAN7602 Rev. 03

Figure 2. Functional Block Diagram of FAN7602

Pin Assignments



FAN7602 Rev. 03

Figure 3. Pin Configuration (Top View)

Pin Definitions

| Pin Number | Pin Name | Pin Function Description |
|------------|--------------|---|
| 1 | LUVP | Line Under-Voltage Protection Pin. This pin is used to protect the set when the input voltage is lower than the rated input voltage range. |
| 2 | Latch/Plimit | Latch Protection and Power Limit Pin. When the pin voltage exceeds 4V, the latch protection works. The latch protection is reset when the V_{CC} voltage is lower than 5V. For the power limit function, the Over-Current Protection (OCP) level decreases as the pin voltage increases. |
| 3 | CS/FB | Current Sense and Feedback Pin. This pin is used to sense the MOSFET current for the current mode PWM and OCP. The output voltage feedback information and the current sense information are added using an external RC filter. |
| 4 | GND | Ground Pin. This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated. |
| 5 | OUT | Gate Drive Output Pin. This pin is an output pin to drive an external MOSFET. The peak sourcing current is 450mA and the peak sinking current is 600mA. For proper operation, the stray inductance in the gate driving path must be minimized. |
| 6 | V_{CC} | Supply Voltage Pin. IC operating current and MOSFET driving current are supplied using this pin. |
| 7 | NC | No Connection. |
| 8 | V_{str} | Start-up Pin. This pin is used to supply IC operating current during IC start-up. After start-up, the internal JFET is turned off to reduce power loss. |

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

| Symbol | Parameter | Value | Unit |
|------------------|--------------------------------------|------------|------|
| V_{CC} | Supply Voltage | 20 | V |
| I_{OH}, I_{OL} | Peak Drive Output Current | +450/-600 | mA |
| $V_{CS/FB}$ | CS/FB Input Voltage | -0.3 to 20 | V |
| V_{LUVP} | LUVP Input Voltage | -0.3 to 10 | V |
| V_{LATCH} | Latch/Plimit Input Voltage | -0.3 to 10 | V |
| V_{STR} | V_{STR} Input Voltage | 600 | V |
| T_J | Operating Junction Temperature | 150 | °C |
| T_A | Operating Temperature Range | -25 to 125 | °C |
| T_{STG} | Storage Temperature Range | -55 to 150 | °C |
| P_D | Power Dissipation | 1.2 | W |
| V_{ESD_HBM} | ESD Capability, Human Body Model | 2.0 | kV |
| V_{ESD_MM} | ESD Capability, Machine Model | 300 | V |
| V_{ESD_CDM} | ESD Capability, Charged Device Model | 500 | V |

Thermal Impedance

| Symbol | Parameter | Value | Unit |
|---------------------|---|-------|------|
| $\theta_{JA}^{(1)}$ | Thermal Resistance, Junction-to-Ambient | 8-DIP | 100 |
| | | | °C/W |

Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

Electrical Characteristics

$V_{CC} = 14V$, $T_A = -25^{\circ}C \sim 125^{\circ}C$, unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------------------------------|--|---|------|---------|------|---------|
| START UP SECTION | | | | | | |
| I_{str} | V_{str} Start-up Current | $V_{str} = 30V$, $T_A = 25^{\circ}C$ | 0.7 | 1 | 1.4 | mA |
| UNDER VOLTAGE LOCK OUT SECTION | | | | | | |
| $V_{th(start)}$ | Start Threshold Voltage | V_{CC} increasing | 11 | 12 | 13 | V |
| $V_{th(stop)}$ | Stop Threshold Voltage | V_{CC} decreasing | 7 | 8 | 9 | V |
| $H_{Y(uvlo)}$ | UVLO Hysteresis | | 3.6 | 4 | 4.4 | V |
| SUPPLY CURRENT SECTION | | | | | | |
| I_{st} | Start-up Supply Current | $T_A = 25^{\circ}C$ | | 250 | 320 | μA |
| I_{CC} | Operating Supply Current | Output no switching | | 1 | 1.5 | mA |
| SOFT-START SECTION | | | | | | |
| T_{SS} | Soft-Start Time ⁽²⁾ | | 5 | 10 | 15 | ms |
| PWM SECTION | | | | | | |
| F_{OSC} | Operating Frequency | $V_{CS/FB} = 0.2V$, $T_A = 25^{\circ}C$ | 59 | 65 | 73 | kHz |
| ΔF | Frequency Modulation | | | ± 2 | | kHz |
| $V_{CS/FB1}$ | CS/FB Threshold Voltage | $T_A = 25^{\circ}C$ | 0.9 | 1.0 | 1.1 | V |
| t_D | Propagation Delay to Output ⁽²⁾ | | | 100 | 150 | ns |
| D_{MAX} | Maximum Duty Cycle | | 70 | 75 | 80 | % |
| D_{MIN} | Minimum Duty Cycle | | | | 0 | % |
| BURST MODE SECTION | | | | | | |
| $V_{CS/FB2}$ | Burst On Threshold Voltage | $T_A = 25^{\circ}C$ | 0.84 | 0.95 | 1.06 | V |
| $V_{CS/FB3}$ | Burst Off Threshold Voltage | $T_A = 25^{\circ}C$ | 0.77 | 0.88 | 0.99 | V |
| POWER LIMIT SECTION | | | | | | |
| K_{Plimit} | Offset Gain | $V_{Latch/Plimit} = 2V$, $T_A = 25^{\circ}C$ | 0.12 | 0.16 | 0.20 | |
| OUTPUT SECTION | | | | | | |
| V_{OH} | Output Voltage High | $T_A = 25^{\circ}C$, $I_{source} = 100mA$ | 11.5 | 12 | 14 | V |
| V_{OL} | Output Voltage Low | $T_A = 25^{\circ}C$, $I_{sink} = 100mA$ | | 1 | 2.5 | V |
| t_r | Rising Time ⁽²⁾ | $T_A = 25^{\circ}C$, $C_l = 1nF$ | | 45 | 150 | ns |
| t_f | Falling Time ⁽²⁾ | $T_A = 25^{\circ}C$, $C_l = 1nF$ | | 35 | 150 | ns |

Note:

2. These parameters, although guaranteed by design, are not tested in production.

Electrical Characteristics (Continued)

$V_{CC} = 14V$, $T_A = -25^{\circ}C \sim 125^{\circ}C$, unless otherwise specified.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|---|---------------------|------|------|------|------|
| PROTECTION SECTION | | | | | | |
| V_{Latch} | Latch Voltage | | 3.6 | 4 | 4.4 | V |
| T_{OLP} | Overload Protection Time ⁽³⁾ | | 20 | 22 | 24 | ms |
| T_{OLP_ST} | Overload Protection Time at Start-up | | 30 | 37 | 44 | ms |
| V_{OLP} | Overload Protection Level | | | 0 | 0.1 | V |
| $V_{LUVPOff}$ | Line Under-Voltage Protection On to Off | $T_A = 25^{\circ}C$ | 1.9 | 2 | 2.1 | V |
| V_{LUVPOn} | Line Under-Voltage Protection Off to On | $T_A = 25^{\circ}C$ | 1.4 | 1.5 | 1.6 | V |
| V_{OVP} | Over Voltage Protection | $T_A = 25^{\circ}C$ | 18 | 19 | 20 | V |

Note:

3. These parameters, although guaranteed by design, are not tested in production.

Typical Performance Characteristics

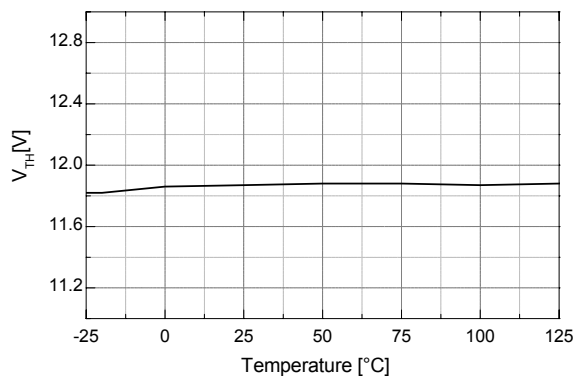


Figure 4. Start Threshold Voltage vs. Temp.

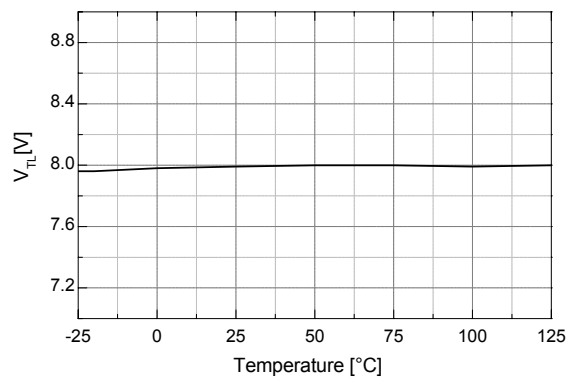


Figure 5. Stop Threshold Voltage vs. Temp.

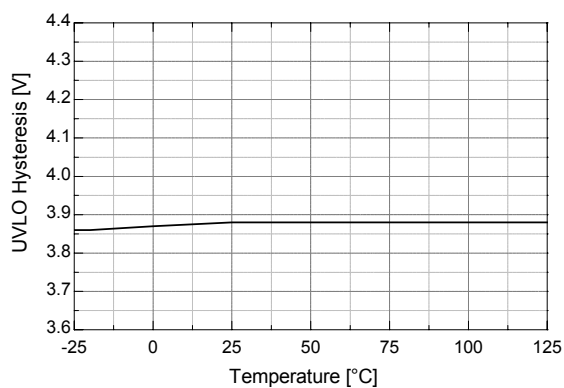


Figure 6. UVLO Hysteresis vs. Temp.

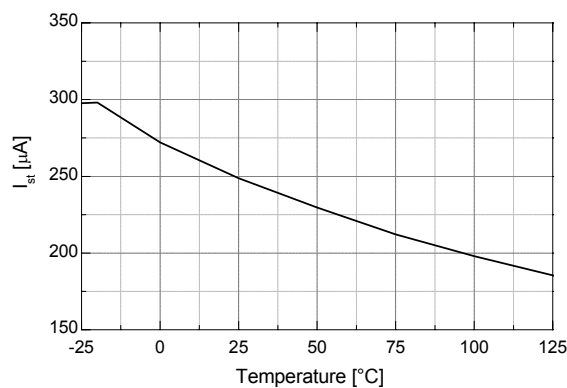


Figure 7. Start-up Supply Current vs. Temp.

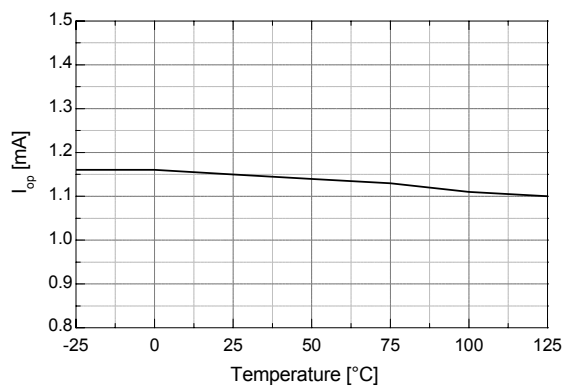


Figure 8. Operating Supply Current vs. Temp.

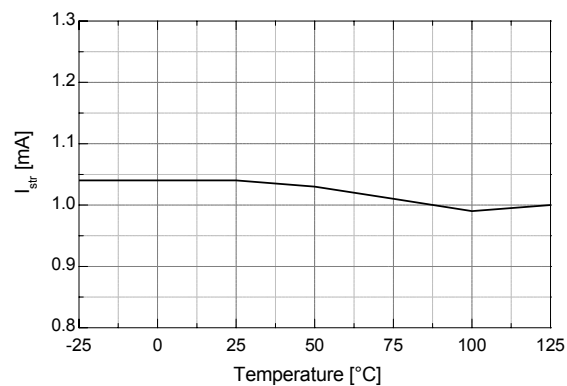


Figure 9. V_{STR} Star-up Current vs. Temp.

Typical Performance Characteristics (Continued)

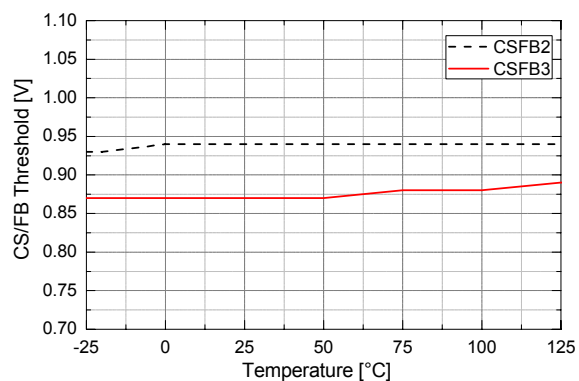


Figure 10. Burst On/Off Voltage vs. Temp.

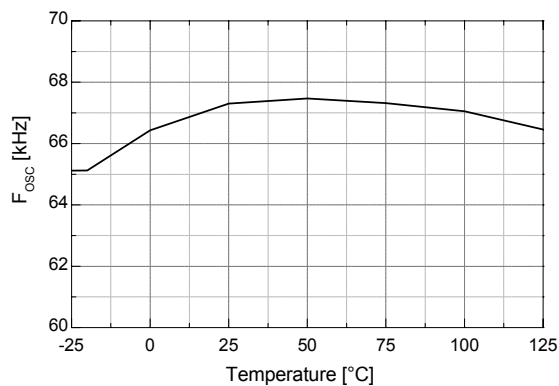


Figure 11. Operating Frequency vs. Temp.

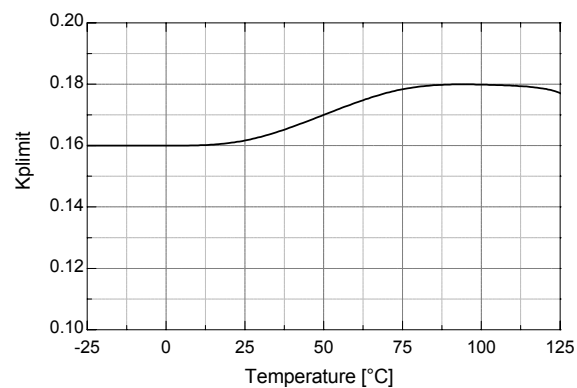


Figure 12. Offset Gain vs. Temp.

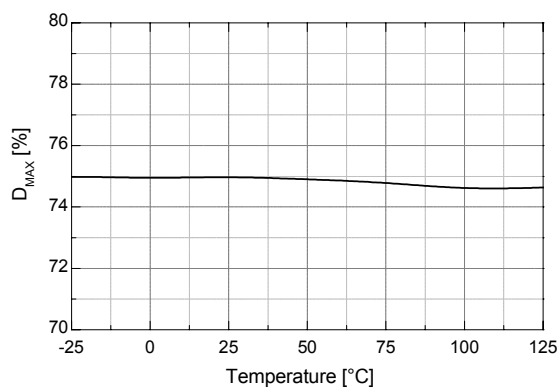


Figure 13. Maximum Duty Cycle vs. Temp.

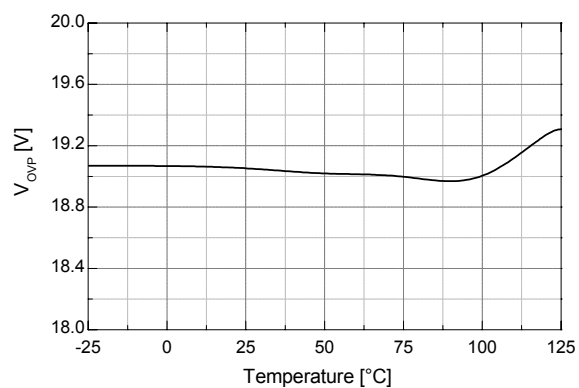


Figure 14. OVP Voltage vs. Temp.

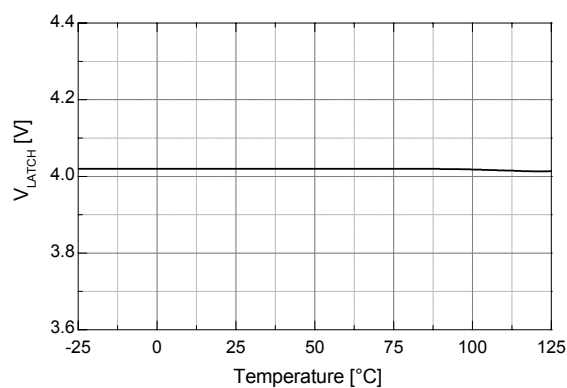
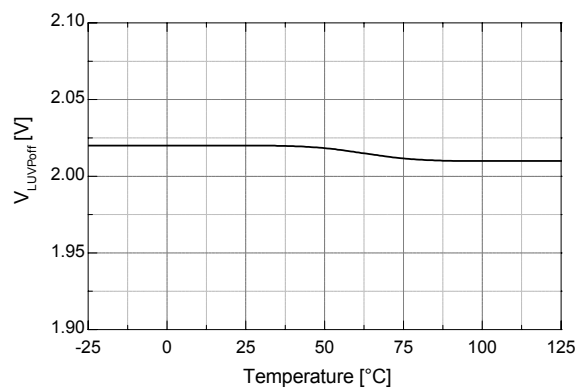
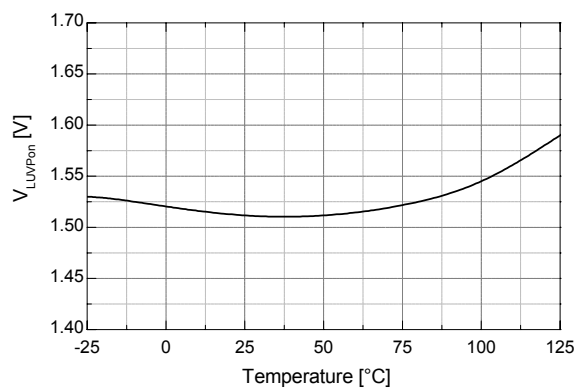
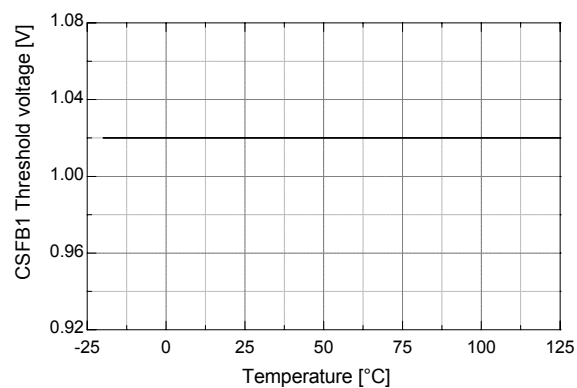


Figure 15. Latch Voltage vs. Temp.

Typical Performance Characteristics (Continued)**Figure 16. LUVP On to Off Voltage vs. Temp.****Figure 17. LUVP Off to On Voltage vs. Temp.****Figure 18. CS/FB Threshold Voltage vs. Temp.**

Applications Information

1. Start-up Circuit and Soft-Start Block

The FAN7602 contains a start-up switch to reduce the power loss of the external start-up circuit of the conventional PWM converters. The internal start-up circuit charges the V_{CC} capacitor with 0.9mA current source if the AC line is connected. The start-up switch is turned off 15ms after IC starts up, as shown in Figure 19. The soft-start function starts when the V_{CC} voltage reaches the start threshold voltage of 12V and ends when the internal soft-start voltage reaches 1V. The internal start-up circuit starts charging the V_{CC} capacitor again if the V_{CC} voltage is lowered to the minimum operating voltage, 8V. The UVLO block shuts down the output drive circuit and some blocks to reduce the IC operating current and the internal soft-start voltage drops to zero. If the V_{CC} voltage reaches the start threshold voltage, the IC starts switching again and the soft-start block works as well.

During the soft-start, pulse-width modulated (PWM) comparator compares the CS/FB pin voltage with the soft-start voltage. The soft-start voltage starts from 0.5V and the soft-start ends when it reaches 1V and the soft-start time is 10ms. The start-up switch is turned off when the soft-start voltage reaches 1.5V.

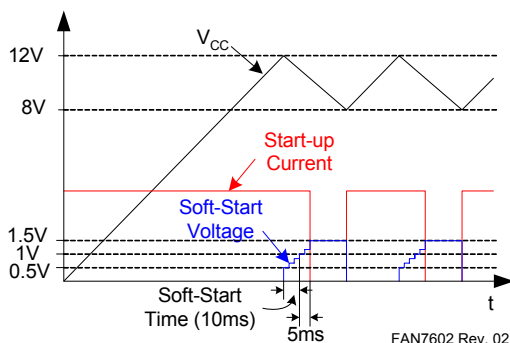


Figure 19. Start-up Current and V_{CC} Voltage

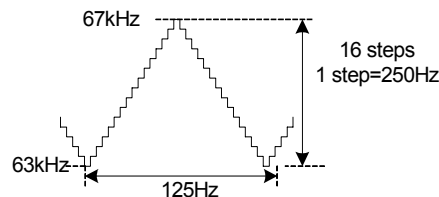
2. Oscillator Block

The oscillator frequency is set internally and a frequency modulation (FM) function reduces EMI. The average frequency is 65kHz and the modulation frequency is ± 2 kHz. The frequency varies from 63kHz to 67kHz with 16 steps. The frequency step is 250Hz and FM frequency is 125Hz, as shown in Figure 20.

3. Current Sense and Feedback Block

The FAN7602 performs the current sensing for the current mode PWM and the output voltage feedback with only one pin, pin 3. To achieve the two functions with one pin, an internal LEB (leading edge blanking) circuit to filter the current sense noise is not included because the external RC filter is necessary to add the output voltage feedback information and the current sense information.

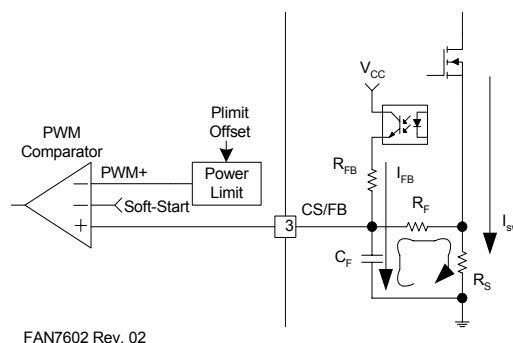
Figure 21 shows the current sense and feedback circuits. R_S is the current sense resistor to sense the switch current. The current sense information is filtered by an RC filter composed of R_F and C_F . According to the output voltage feedback information, I_{FB} charges or stops charging C_F to adjust the offset voltage. If I_{FB} is zero, C_F is discharged through R_F and R_S to lower the offset voltage.



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Figure 20. Frequency Modulation

Figure 22 shows typical voltage waveforms of the CS/FB pin. The current sense waveform is added to the offset voltage as shown in the figure. The CS/FB pin voltage is compared with PWM+ that is 1V - Plimit offset as shown in Figure 22. If the CS/FB voltage meets PWM+, the output drive is shut off. As shown in Figure 22, if the feedback offset voltage is low, the switch on time is increased. If the feedback offset voltage is high, the switch on time is decreased. In this way, the duty cycle is controlled according to the output load condition. In general, the maximum output power increases as the input voltage increases because the current slope during switch on-time increases. To limit the output power of the converter constantly, the power limit function is included in the FAN7602. Sensing the converter input voltage through the Latch/Plimit pin, the Plimit offset voltage is subtracted from 1V. As shown in Figure 22, the Plimit offset voltage is subtracted from 1V and the switch on-time decreases as the Plimit offset voltage increases. If the converter input voltage increases, the switch on-time decreases, controlling the output power constant. The offset voltage is proportional to the Latch/Plimit pin voltage and the gain is 0.16. If the Latch/Plimit voltage is 1V, the offset voltage is 0.16V.



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Figure 21. Current Sense and Feedback Circuits

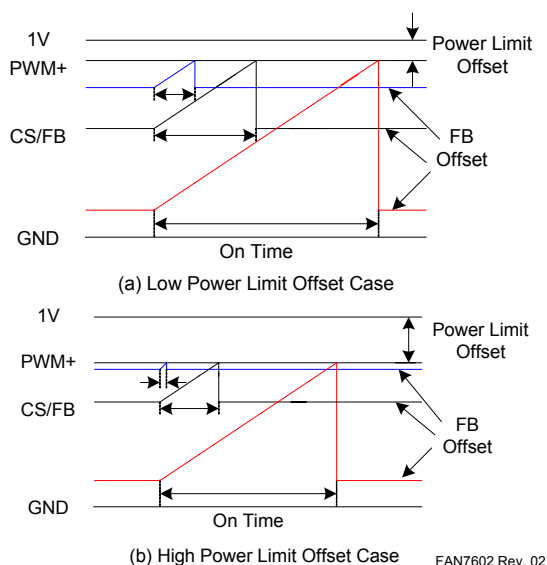


Figure 22. CS/FB Pin Voltage Waveforms

4. Burst Mode Block

The FAN7602 contains the burst mode block to reduce the power loss at a light load and no load as the FAN7601. A hysteresis comparator senses the offset voltage of the Burst+ for the burst mode as shown in Figure 23. The Burst+ is the sum of the CS/FB voltage and Plimit offset voltage. The FAN7602 enters the burst mode when the offset voltage of the Burst+ is higher than 0.95V and exits the burst mode when the offset voltage is lower than 0.88V. The offset voltage is sensed during the switch off time.

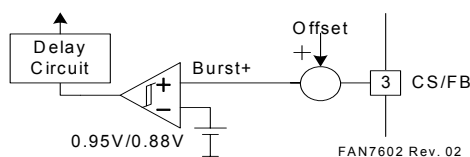


Figure 23. Burst Mode Block

5. Protection Block

The FAN7602 contains several protection functions to improve system reliability.

5.1 Overload Protection

The FAN7602 contains the overload protection function. If the output load is higher than the rated output current, the output voltage drops and the feedback error amplifier is saturated. The offset of the CS/FB voltage representing the feedback information is almost zero. As shown in Figure 24, the CS/FB voltage is compared with 50mV reference when the internal clock signal is high and, if the voltage is lower than 50mV, the OLP timer starts

counting. If the OLP condition persists for 22ms, the timer generates the OLP signal. And this protection is reset by the UVLO. The OLP block is enabled after the soft-start finishes.

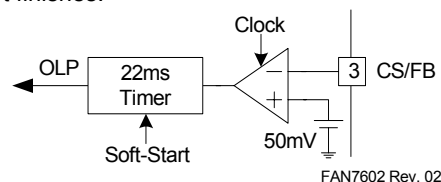


Figure 24. Overload Protection Circuit

5.2 Line Under-Voltage Protection

If the input voltage of the converter is lower than the minimum operating voltage, the converter input current increases too much, causing components failure. Therefore, if the input voltage is low, the converter should be protected. In the FAN7602, the LUV circuit senses the input voltage using the LUV pin and, if this voltage is lower than 2V, the LUV signal is generated. The comparator has 0.5V hysteresis. If the LUV signal is generated, the output drive block is shut down, the output voltage feedback loop is saturated, and the OLP works if the LUV condition persists more than 22ms.

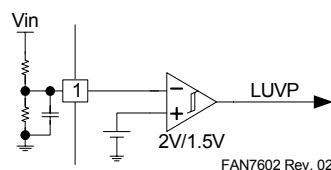


Figure 25. Line UVP Circuit

5.3 Latch Protection

The latch protection is provided to protect the system against abnormal conditions using the Latch/Plimit pin. The Latch/Plimit pin can be used for the output over-voltage protection and/or other protections. If the Latch/Plimit pin voltage is made higher than 4V by an external circuit, the IC is shut down. The latch protection is reset when the V_{CC} voltage is lower than 5V.

5.4 Over-Voltage Protection (OVP)

If the V_{CC} voltage reaches 19V, the IC shuts down and the OVP protection is reset when the V_{CC} voltage is lower than 5V.

6. Output Drive Block

The FAN7602 contains a single totem-pole output stage to drive a power MOSFET. The drive output is capable of up to 450mA sourcing current and 600mA sinking current with typical rise and fall time of 45ns, 35ns respectively with a 1nF load.

2. Inductor Schematic Diagram

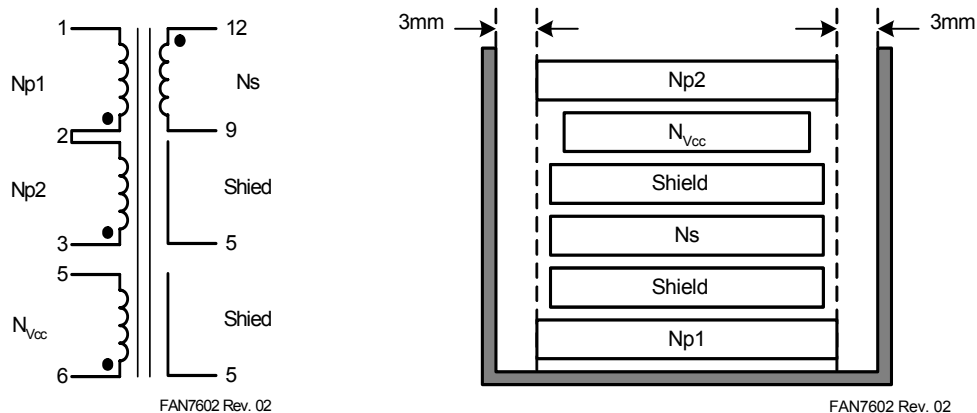


Figure 27. Inductor Schematic Diagram

3. Winding Specification

| No | Pin (s→f) | Wire | Turns | Winding Method |
|---|-----------|------------------------|-------|------------------|
| Np1 | 3 → 2 | $0.3^{\phi} \times 2$ | 31 | Solenoid Winding |
| Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |
| Shield | 5 | Copper Tape | 0.9 | Not Shorted |
| Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |
| Ns | 12 → 9 | $0.65^{\phi} \times 3$ | 10 | Solenoid Winding |
| Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |
| Shield | 5 | Copper Tape | 0.9 | Not Shorted |
| Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |
| N _{Vcc} | 6 → 5 | $0.2^{\phi} \times 1$ | 10 | Solenoid Winding |
| Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |
| Np2 | 2 → 1 | $0.3^{\phi} \times 2$ | 31 | Solenoid Winding |
| Outer Insulation: Polyester Tape $t = 0.03\text{mm}$, 2 Layers | | | | |

4. Electrical Characteristics

| | Pin | Specification | Remarks |
|------------|-------|------------------|----------------|
| Inductance | 1 - 3 | $607\mu\text{H}$ | 100kHz, 1V |
| Inductance | 1 - 3 | $15\mu\text{H}$ | 9 - 12 shorted |

5. Core & Bobbin

- Core: EER2828
- Bobbin: EER2828
- $A_e(\text{mm}^2)$: 82.1

6. Demo Circuit Part List

| Part | Value | Note | Part | Value | Note |
|-----------------|----------|-----------|------------------|------------|---------------|
| Fuse | | | Capacitor | | |
| FUSE | 1A/250V | | C101 | 220nF/275V | Box Capacitor |
| NTC | | | C102 | 150nF/275V | Box Capacitor |
| RT101 | 5D-9 | | C103, C104 | 102/1kV | Ceramic |
| Resistor | | | C105 | 150μF/400V | Electrolytic |
| R102, R112 | 10MΩ | 1/4W | C106 | 103/630V | Film |
| R103 | 56kΩ | 1/2W | C107 | 271 | Ceramic |
| R104 | 150Ω | 1/4W | C108 | 103 | Ceramic |
| R105 | 1kΩ | 1/4W | C109 | 22μF/25V | Electrolytic |
| R106 | 0.5Ω | 1/2W | C110 | 473 | Ceramic |
| R107 | 56kΩ | 1/4W | C201, C202 | 1000μF/25V | Electrolytic |
| R108 | 10kΩ | 1/4W | C203 | 102 | Ceramic |
| R109 | 0Ω | 1/4W | C204 | 102 | Ceramic |
| R110 | 1kΩ | 1/4W | C222 | 222/1kV | Ceramic |
| R111 | 6kΩ | 1/4W | MOSFET | | |
| R113 | 180kΩ | 1/4W | Q101 | FQPF8N60C | Fairchild |
| R114 | 50kΩ | 1/4W | Diode | | |
| R201 | 1.5kΩ | 1/4W | D101, D102 | UF4007 | Fairchild |
| R202 | 1.2kΩ | 1/4W | D103 | 1N5819 | Fairchild |
| R203 | 20kΩ | 1/4W | D202, D204 | FYPF2010DN | Fairchild |
| R204 | 27kΩ | 1/4W | ZD101, ZD201 | 1N4744 | Fairchild |
| R205 | 7kΩ | 1/4W | BD101 | KBP06 | Fairchild |
| R206 | 10Ω | 1/2W | TNR | | |
| R207 | 10kΩ | 1/4W | R101 | 471 | 470V |
| IC | | | Filter | | |
| IC101 | FAN7602 | Fairchild | LF101 | 23mH | 0.8A |
| IC201 | KA431 | Fairchild | L201 | 10μH | 4.2A |
| OP1, OP2 | H11A817B | Fairchild | | | |

7. PCB Layout

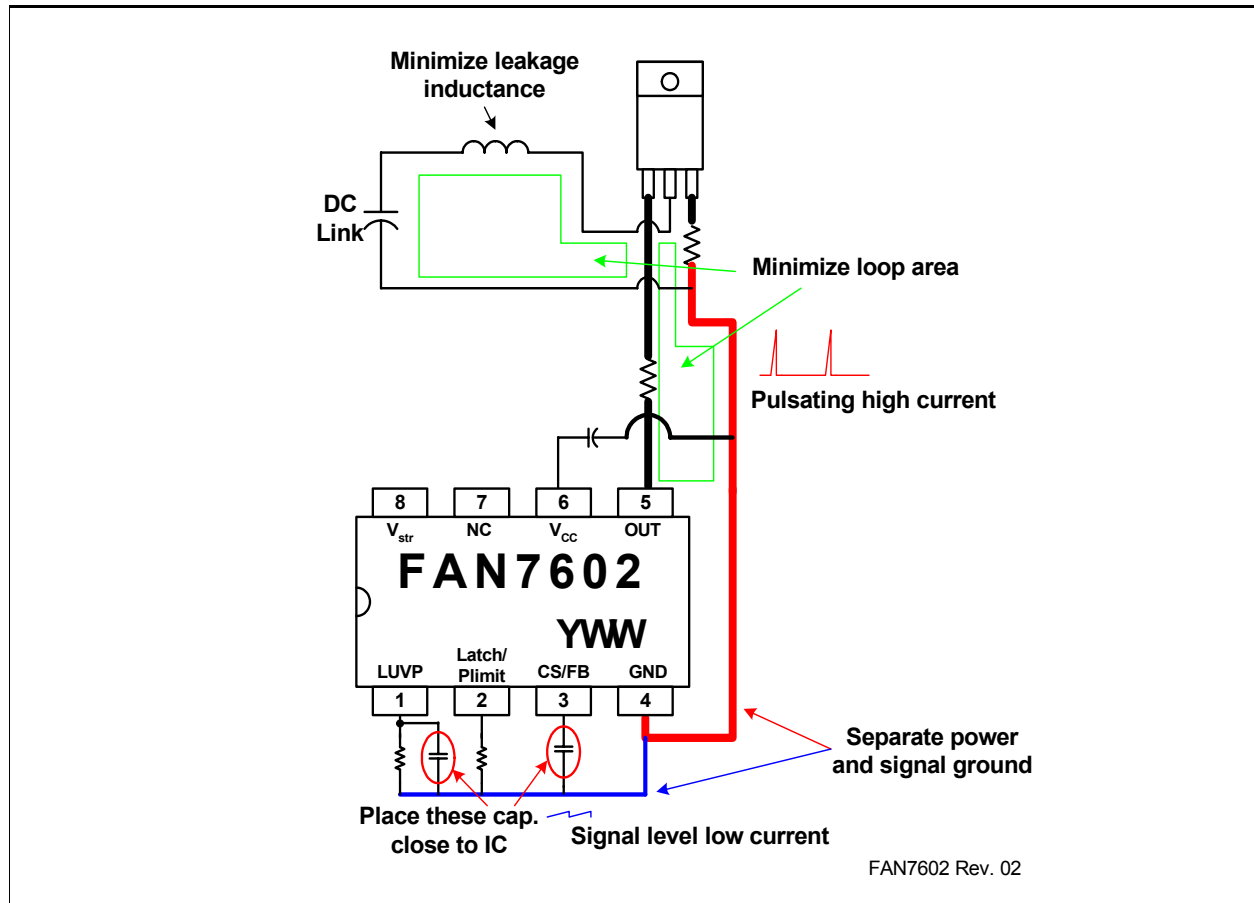


Figure 28. PCB Layout Recommendations for FAN7602

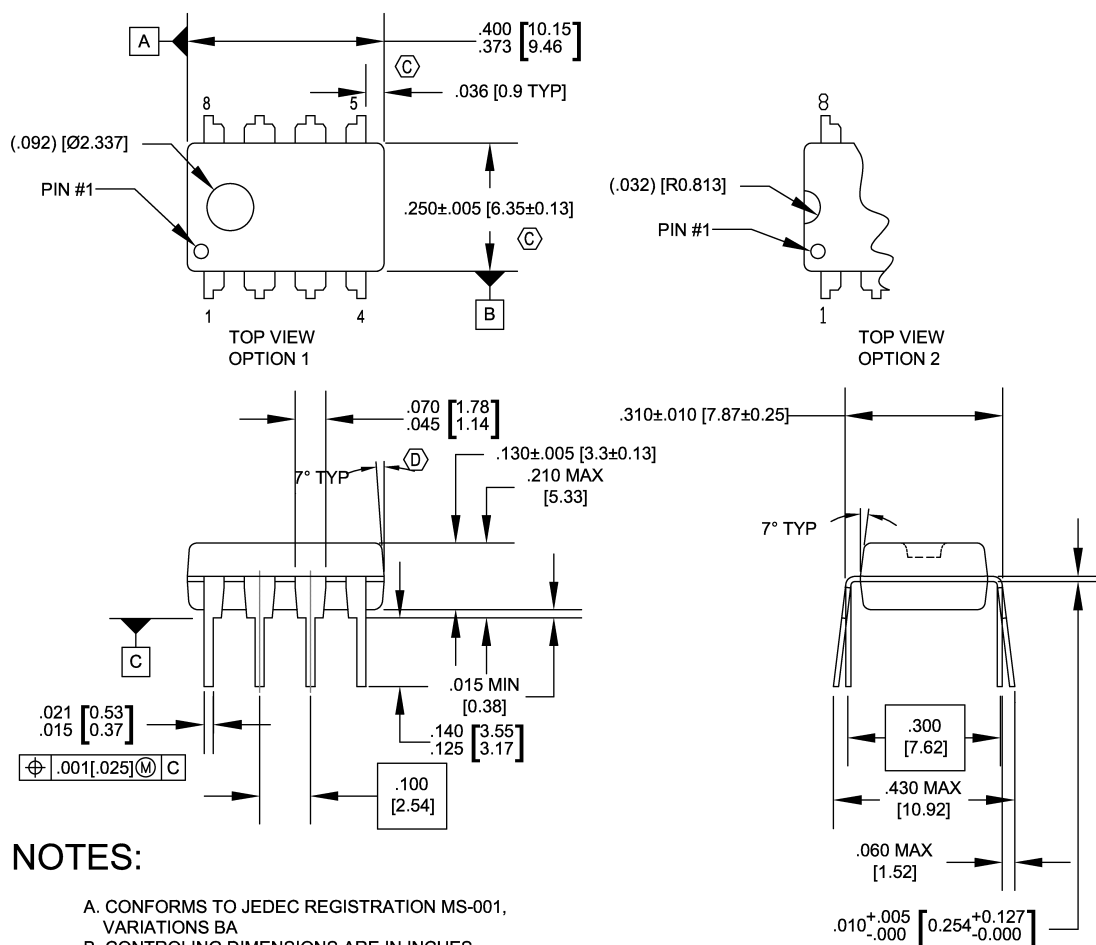
8. Performance Data

| | 85V _{AC} | 110V _{AC} | 220V _{AC} | 265V _{AC} |
|--------------------------|-------------------|--------------------|--------------------|--------------------|
| Input Power at No Load | 105.4mW | 119.8mW | 184.7mW | 205.5mW |
| Input Power at 0.5W Load | 739.4mW | 761.4mW | 825.4mW | 872.2mW |
| OLP Point | 4.42A | 4.66A | 4.6A | 4.4A |

Mechanical Dimensions

8-DIP

Dimensions are in inches (millimeters) unless otherwise noted.



NOTES:

- CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
- CONTROLLING DIMENSIONS ARE IN INCHES
REFERENCE DIMENSIONS ARE IN MILLIMETERS
- DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
.010 INCHES OR 0.25MM.
- DOES NOT INCLUDE DAMBAR PROTRUSIONS.
DAMBAR PROTRUSIONS SHALL NOT EXCEED
.010 INCHES OR 0.25MM.
- DIMENSIONING AND TOLERANCING
PER ASME Y14.5M-1994.

N08EREVG

Figure 29. 8-Lead Dual In-Line Package (DIP)

Mechanical Dimensions (Continued)**8-SOP**

Dimensions are in millimeters unless otherwise noted.

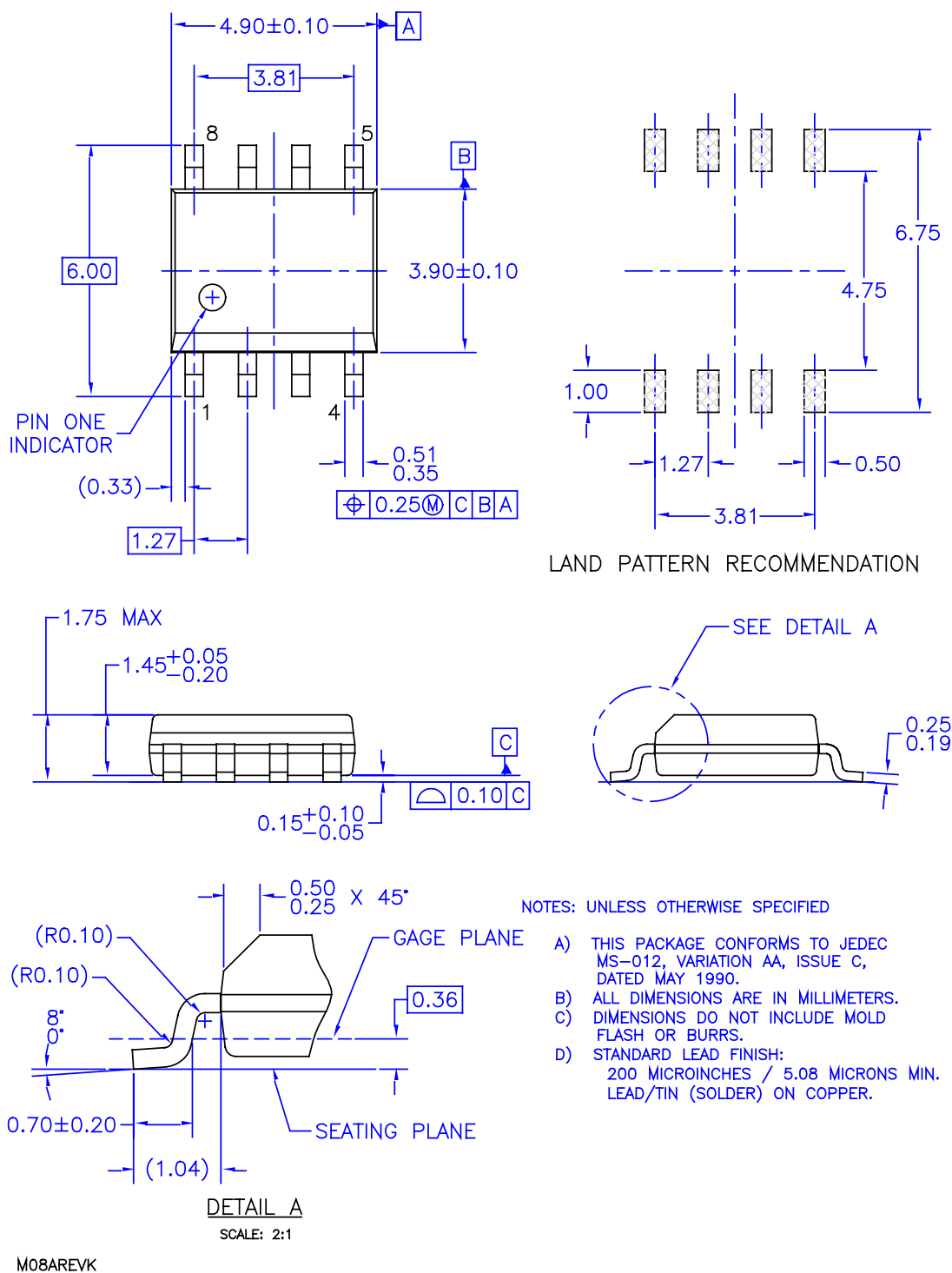


Figure 30. 8-Lead Small Outline Package (SOP)

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