



STD1NB50

N - CHANNEL 500V - 7.5Ω - 1.4A IPAK PowerMESH™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD1NB50	500V	< 9 Ω	1.4 A

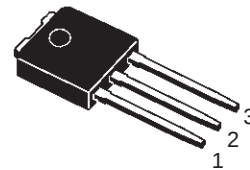
- TYPICAL R_{DS(on)} = 7.5 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- FOR SMD DPAK VERSION CONTACT SALES OFFICE

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R_{DS(on)} per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

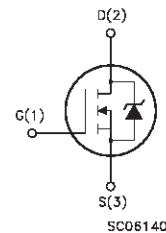
APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE



**IPAK
TO-251
(Suffix "-1")**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate-source Voltage	± 36	V
I _D	Drain Current (continuous) at T _c = 25 °C	1.4	A
I _D	Drain Current (continuous) at T _c = 100 °C	0.91	A
I _{DM} (•)	Drain Current (pulsed)	5.6	A
P _{tot}	Total Dissipation at T _c = 25 °C	45	W
	Derating Factor	0.36	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 1.4A, di/dt ≤ 150 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

STD1NB50

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.78	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	100	$^{\circ}C/W$
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	1.5	$^{\circ}C/W$
T_I	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}C$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	1.4	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}C$, $I_D = I_{AR}$, $V_{DD} = 50 V$)	40	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 0.5 A$		7.5	9	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	1.4			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 0.7 A$	0.45	0.7		S
C_{iss}	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		150	200	pF
C_{oss}	Output Capacitance			24	32	pF
C_{rss}	Reverse Transfer Capacitance			2.5	3.3	pF

ELECTRICAL CHARACTERISTICS (continued)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 250\text{ V}$ $I_D = 0.7\text{ A}$		8	12	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		8	12	ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$ $I_D = 1.4\text{ A}$ $V_{GS} = 10\text{ V}$		9	13	nC
Q_{gs}	Gate-Source Charge			5.5		nC
Q_{gd}	Gate-Drain Charge			2.4		nC

SWITCHING OFF

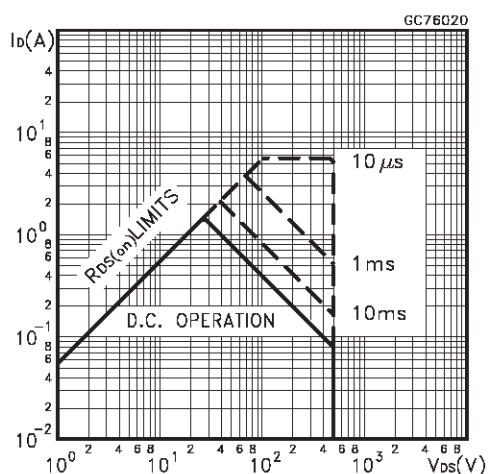
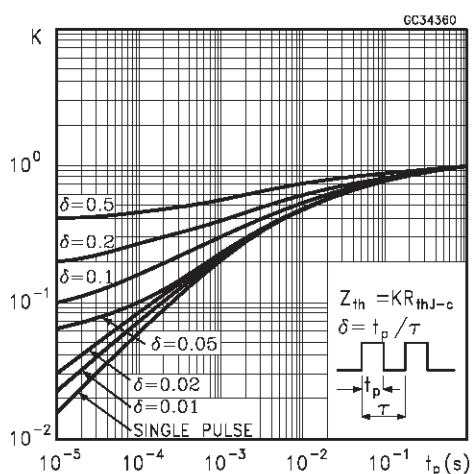
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_r(V_{off})$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$ $I_D = 1.4\text{ A}$		20	28	ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		22	31	ns
t_c	Cross-over Time			30	42	ns

SOURCE DRAIN DIODE

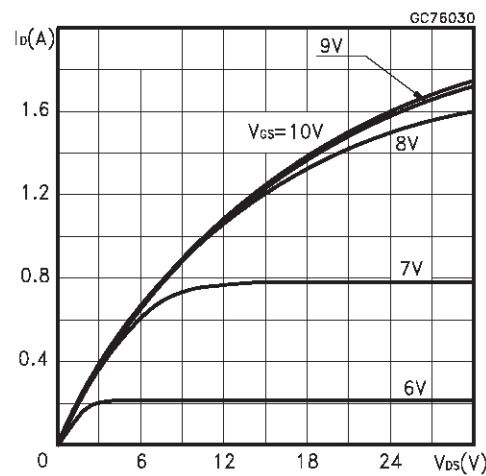
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				1.4	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				5.6	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 1.4\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 1.4\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		330		ns
Q_{rr}	Reverse Recovery Charge			780		nC
I_{RRM}	Reverse Recovery Current			4.7		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

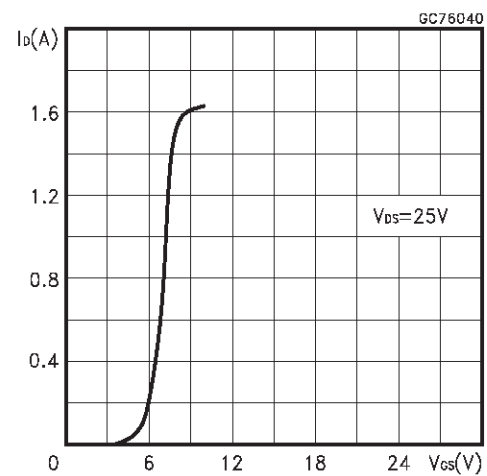
(\bullet) Pulse width limited by safe operating area

Safe Operating Area**Thermal Impedance**

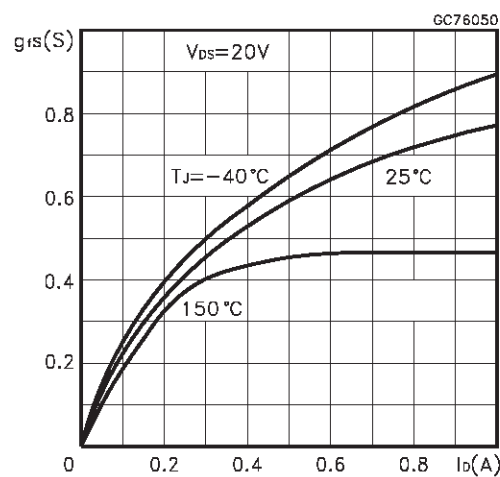
Output Characteristics



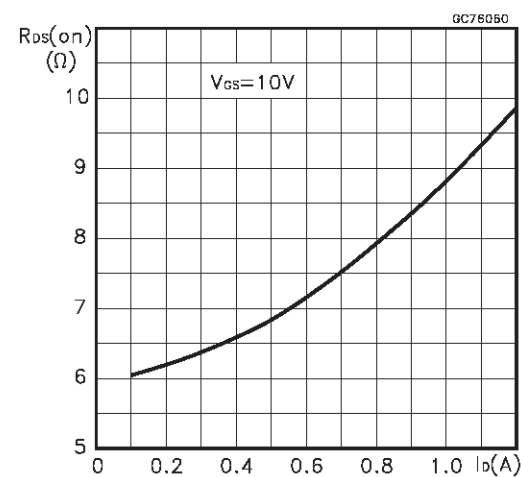
Transfer Characteristics



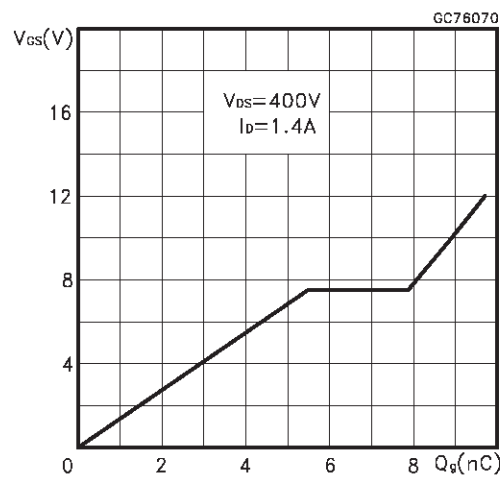
Transconductance



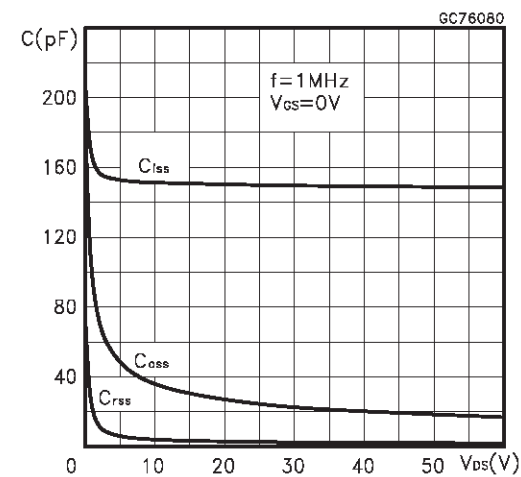
Static Drain-source On Resistance



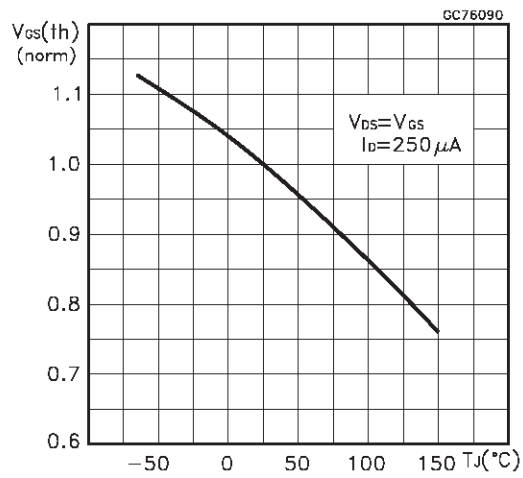
Gate Charge vs Gate-source Voltage



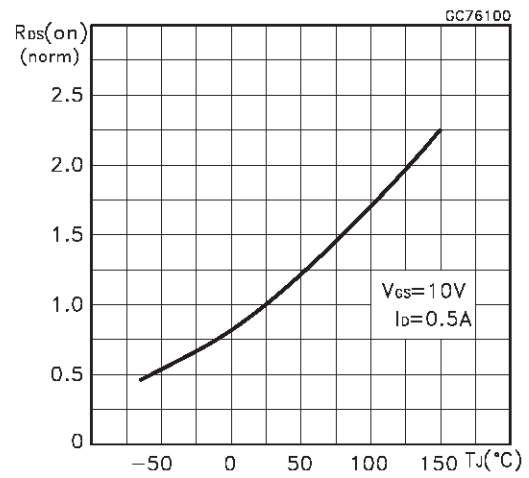
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

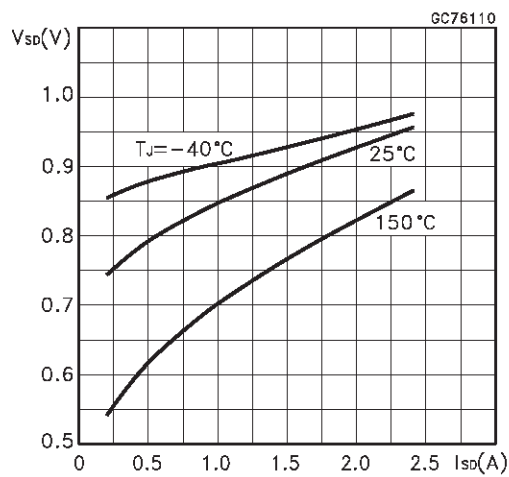


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform

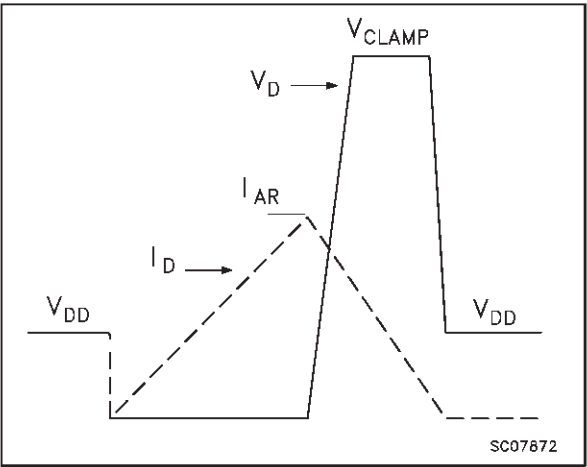


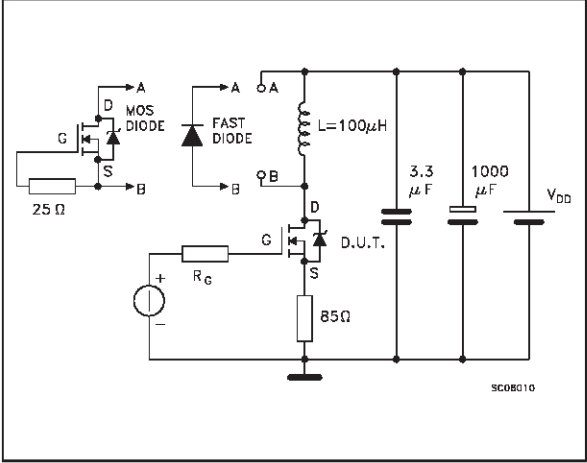
Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

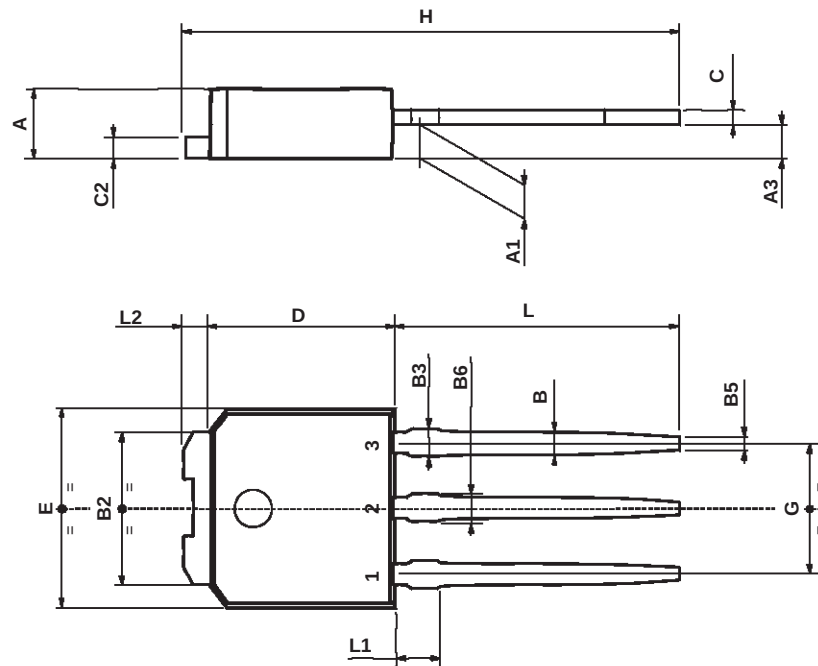


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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