

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$
- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCB}$  Voltage
- If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.4-V to 3.6-V Power-Supply Range
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCB164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCB164245 is designed so that the control pins (1DIR, 2DIR,  $1\overline{OE}$ , and  $2\overline{OE}$ ) are supplied by  $V_{CCB}$ .

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CCB}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either  $V_{CC}$  input is at GND, both ports are in the high-impedance state.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Tape and reel	74AVCB164245GRDR	WB4245
	FBGA – ZRD (Pb-Free)	Tape and reel	74AVCB164245ZRDR	
	TSSOP – DGG	Tape and reel	SN74AVCB164245GR	AVCB164245
	TVSOP – DGV	Tape and reel	SN74AVCB164245VR	WB4245
	VFBGA – GQL	Tape and reel	SN74AVCB164245KR	
	VFBGA – ZQL (Pb-Free)	Tape and reel	74AVCB164245ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

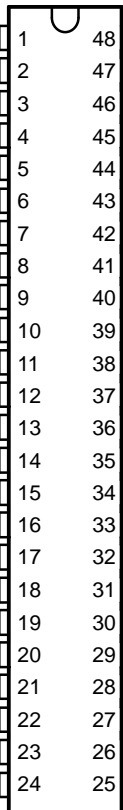


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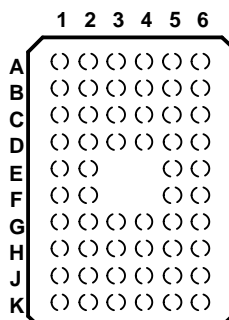
**TERMINAL ASSIGNMENTS**

DGG OR DGV PACKAGE  
(TOP VIEW)



1DIR	1	48	1 $\overline{OE}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V <sub>CCB</sub>	7	42	V <sub>CCA</sub>
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V <sub>CCB</sub>	18	31	V <sub>CCA</sub>
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2 $\overline{OE}$

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

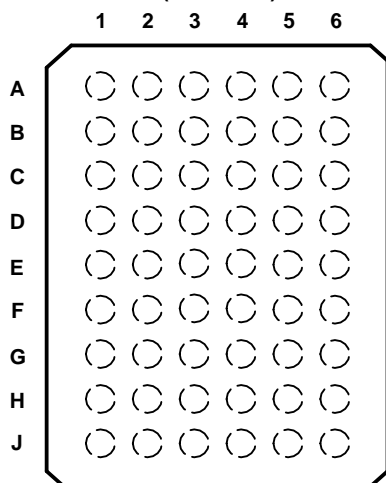


**TERMINAL ASSIGNMENTS  
(56-Ball GQL/ZQL Package)<sup>(1)</sup>**

	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1 $\overline{OE}$
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	V <sub>CCB</sub>	V <sub>CCA</sub>	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	V <sub>CCB</sub>	V <sub>CCA</sub>	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	2 $\overline{OE}$

(1) NC - No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS  
(54-Ball GRD/ZRD Package)<sup>(1)</sup>**

	1	2	3	4	5	6
<b>A</b>	1B1	NC	1DIR	1 $\overline{OE}$	NC	1A1
<b>B</b>	1B3	1B2	NC	NC	1A2	1A3
<b>C</b>	1B5	1B4	V <sub>CCB</sub>	V <sub>CCA</sub>	1A4	1A5
<b>D</b>	1B7	1B6	GND	GND	1A6	1A7
<b>E</b>	2B1	1B8	GND	GND	1A8	2A1
<b>F</b>	2B3	2B2	GND	GND	2A2	2A3
<b>G</b>	2B5	2B4	V <sub>CCB</sub>	V <sub>CCA</sub>	2A4	2A5
<b>H</b>	2B7	2B6	NC	NC	2A6	2A7
<b>J</b>	2B8	NC	2DIR	2 $\overline{OE}$	NC	2A8

(1) NC - No internal connection

**FUNCTION TABLE  
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

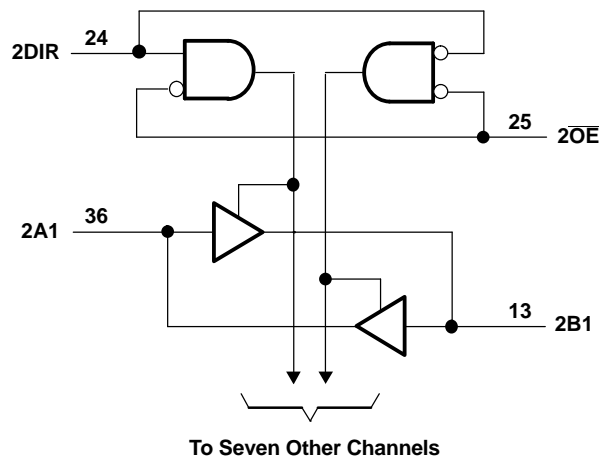
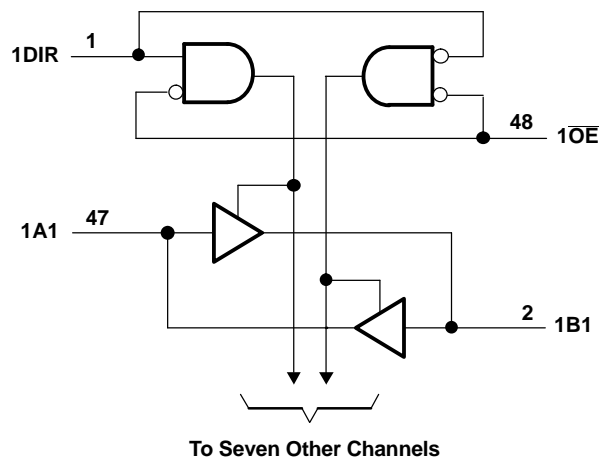
# SN74AVCB164245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES394D–JUNE 2002–REVISED JUNE 2005

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG and DGV packages.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage range		-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	-0.5	4.6	V
		B port	-0.5	4.6	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND			100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		70	°C/W
		DGV package		58	
		GQL/ZQL package		28	
		GRD/ZRD package		36	
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)(2)(3)</sup>

over operating free-air temperature range (unless otherwise noted)

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.4	3.6	V
V <sub>CCB</sub>	Supply voltage				1.4	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs	1.4 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs	1.4 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	Control inputs (referenced to V <sub>CCB</sub> )	1.4 V to 1.95 V		V <sub>CCB</sub> × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Control inputs (referenced to V <sub>CCB</sub> )	1.4 V to 1.95 V		V <sub>CCB</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.4 V to 1.6 V	−2		mA
				1.65 V to 1.95 V	−4		
				2.3 V to 2.7 V	−8		
				3 V to 3.6 V	−12		
I <sub>OL</sub>	Low-level output current			1.4 V to 1.6 V	2		mA
				1.65 V to 1.95 V	4		
				2.3 V to 2.7 V	8		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the data output port.

(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74AVCB164245

## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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#### Electrical Characteristics<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(3)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA	V <sub>I</sub> = V <sub>IH</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V	V <sub>CCO</sub> − 0.2			V
		I <sub>OH</sub> = −2 mA	V <sub>I</sub> = V <sub>IH</sub>	1.4 V	1.4 V	1.05			
		I <sub>OH</sub> = −4 mA	V <sub>I</sub> = V <sub>IH</sub>	1.65 V	1.65 V	1.2			
		I <sub>OH</sub> = −8 mA	V <sub>I</sub> = V <sub>IH</sub>	2.3 V	2.3 V	1.75			
		I <sub>OH</sub> = −12 mA	V <sub>I</sub> = V <sub>IH</sub>	3 V	3 V	2.3			
V <sub>OL</sub>		I <sub>OH</sub> = 100 μA	V <sub>I</sub> = V <sub>IL</sub>	1.4 V to 3.6 V	1.4 V to 3.6 V			0.2	V
		I <sub>OH</sub> = 2 mA	V <sub>I</sub> = V <sub>IL</sub>	1.4 V	1.4 V			0.35	
		I <sub>OH</sub> = 4 mA	V <sub>I</sub> = V <sub>IL</sub>	1.65 V	1.65 V			0.45	
		I <sub>OH</sub> = 8 mA	V <sub>I</sub> = V <sub>IL</sub>	2.3 V	2.3 V			0.55	
		I <sub>OH</sub> = 12 mA	V <sub>I</sub> = V <sub>IL</sub>	3 V	3 V			0.7	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCB</sub> or GND		1.4 V to 3.6 V	3.6 V			±2.5	μA
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V		0 V	0 to 3.6 V			±10	μA
	B port			0 to 3.6 V	0 V			±10	
I <sub>OZ</sub> <sup>(4)</sup>	A or B ports	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND	$\overline{OE}$ = V <sub>IH</sub>	3.6 V	3.6 V			±12.5	μA
	B port		$\overline{OE}$ = don't care	0 V	3.6 V			±12.5	
	A port			3.6 V	0 V			±12.5	
I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			20	μA
				1.95 V	1.95 V			20	
				2.7 V	2.7 V			30	
				0 V	3.6 V			−40	
				3.6 V	0 V			40	
				3.6 V	3.6 V			40	
I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0			1.6 V	1.6 V			20	μA
				1.95 V	1.95 V			20	
				2.7 V	2.7 V			30	
				0 V	3.6 V			40	
				3.6 V	0 V			−40	
				3.6 V	3.6 V			40	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3.3 V or GND		3.3 V	3.3 V	4		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 3.3 V or GND		3.3 V	3.3 V	5		pF	

(1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.

(3) All typical values are at T<sub>A</sub> = 25°C.

(4) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
$t_{en}$	$\overline{OE}$	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
		B	2.1	9	2.9	9.8	3.2	10	3	9.8	
$t_{dis}$	$\overline{OE}$	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
		B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.7	6.7	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
$t_{en}$	$\overline{OE}$	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
$t_{dis}$	$\overline{OE}$	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
		B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
$t_{en}$	$\overline{OE}$	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
		B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
$t_{dis}$	$\overline{OE}$	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
		B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V}$ 0.1 V		$V_{CCB} = 1.8 \text{ V}$ 0.15 V		$V_{CCB} = 2.5 \text{ V}$ 0.2 V		$V_{CCB} = 3.3 \text{ V}$ 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
$t_{en}$	$\overline{OE}$	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
		B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
$t_{dis}$	$\overline{OE}$	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
		B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

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## 16-BIT DUAL-SUPPLY BUS TRANSCEIVER

### WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

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#### Operating Characteristics

$V_{CCA}$  and  $V_{CCB} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
$C_{pdA}$ ( $V_{CCA}$ )	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	14	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		20	
		Outputs disabled		7	
$C_{pdB}$ ( $V_{CCB}$ )	Power dissipation capacitance per transceiver, A-port input, B-port output	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$	20	pF
		Outputs disabled		7	
	Power dissipation capacitance per transceiver, B-port input, A-port output	Outputs enabled		14	
		Outputs disabled		7	

#### Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

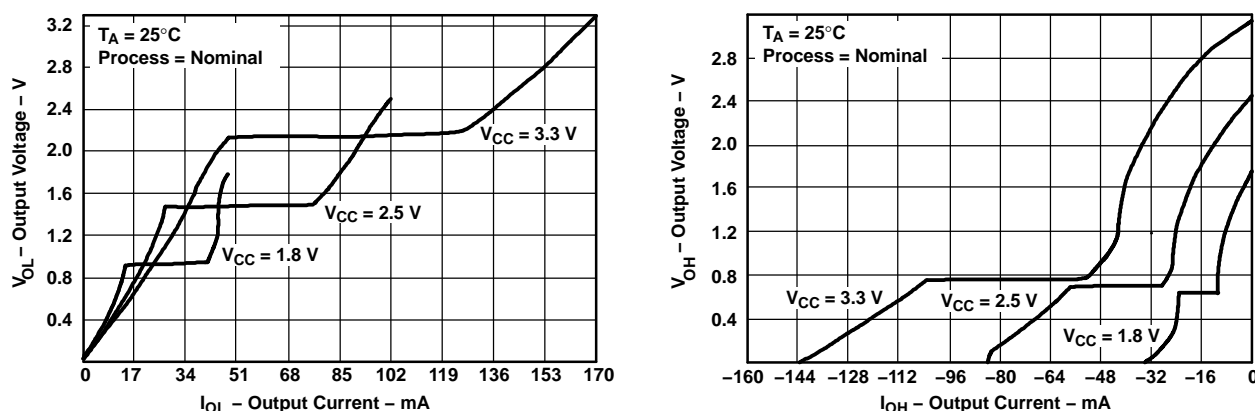
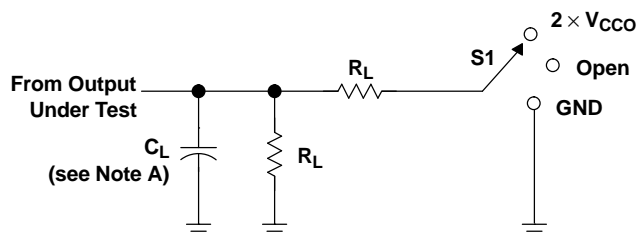


Figure 1. Typical Output Voltage vs Output Current



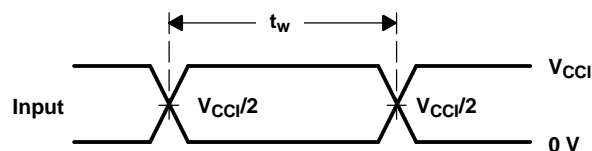
## PARAMETER MEASUREMENT INFORMATION



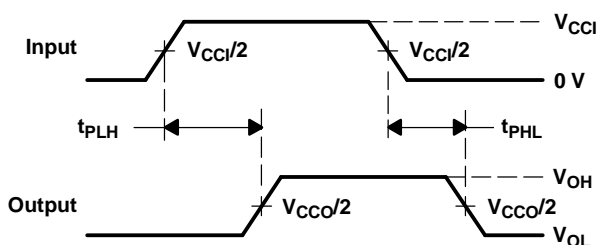
LOAD CIRCUIT

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.5\text{ V} \pm 0.1\text{ V}$	15 pF	2 k $\Omega$	0.1 V
$1.8\text{ V} \pm 0.15\text{ V}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	30 pF	500 $\Omega$	0.3 V

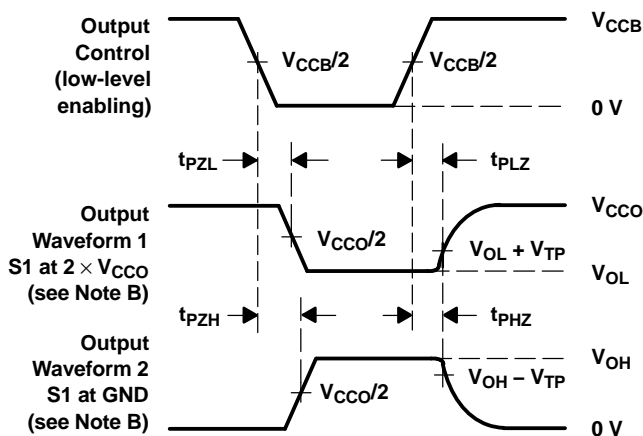
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVCB164245GRDR	OBSOLETE	BGA MICROSTAR JUNIOR	GRD	54		TBD	Call TI	Call TI	-40 to 85		
74AVCB164245GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	<a href="#">Samples</a>
74AVCB164245GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	<a href="#">Samples</a>
74AVCB164245VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WB4245	<a href="#">Samples</a>
74AVCB164245VRG4	ACTIVE	TVSOP	DGV	48		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
74AVCB164245ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WB4245	<a href="#">Samples</a>
74AVCB164245ZRDR	ACTIVE	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WB4245	<a href="#">Samples</a>
SN74AVCB164245GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCB164245	<a href="#">Samples</a>
SN74AVCB164245KR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	WB4245	
SN74AVCB164245VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WB4245	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AVCB164245 :**

- Automotive: [SN74AVCB164245-Q1](#)
- Enhanced Product: [SN74AVCB164245-EP](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVCB164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
74AVCB164245ZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1
SN74AVCB164245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74AVCB164245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

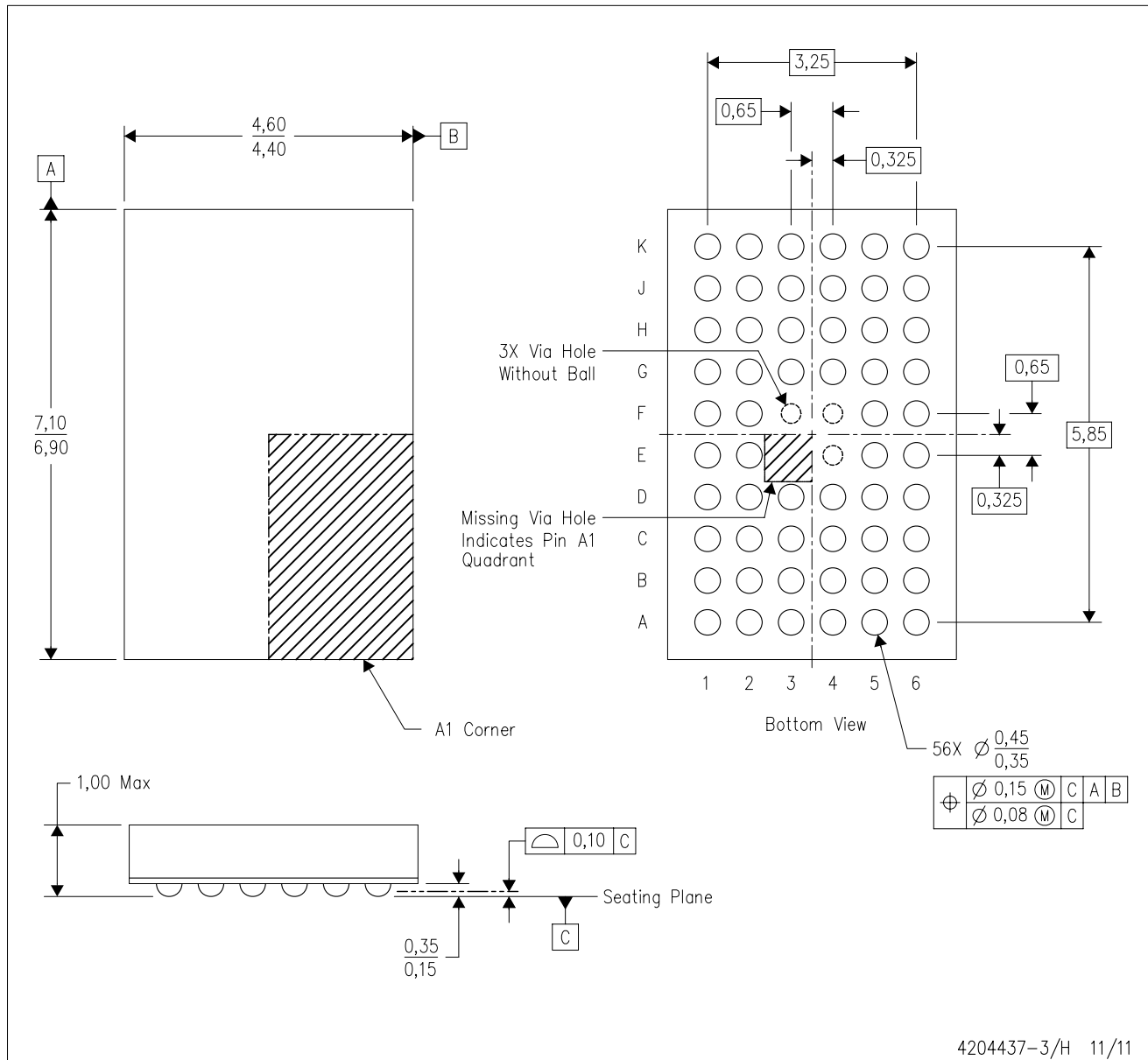


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVCB164245ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6
74AVCB164245ZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	336.6	336.6	28.6
SN74AVCB164245GR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVCB164245VR	TVSOP	DGV	48	2000	367.0	367.0	38.0

ZQL (R-PBGA-N56)

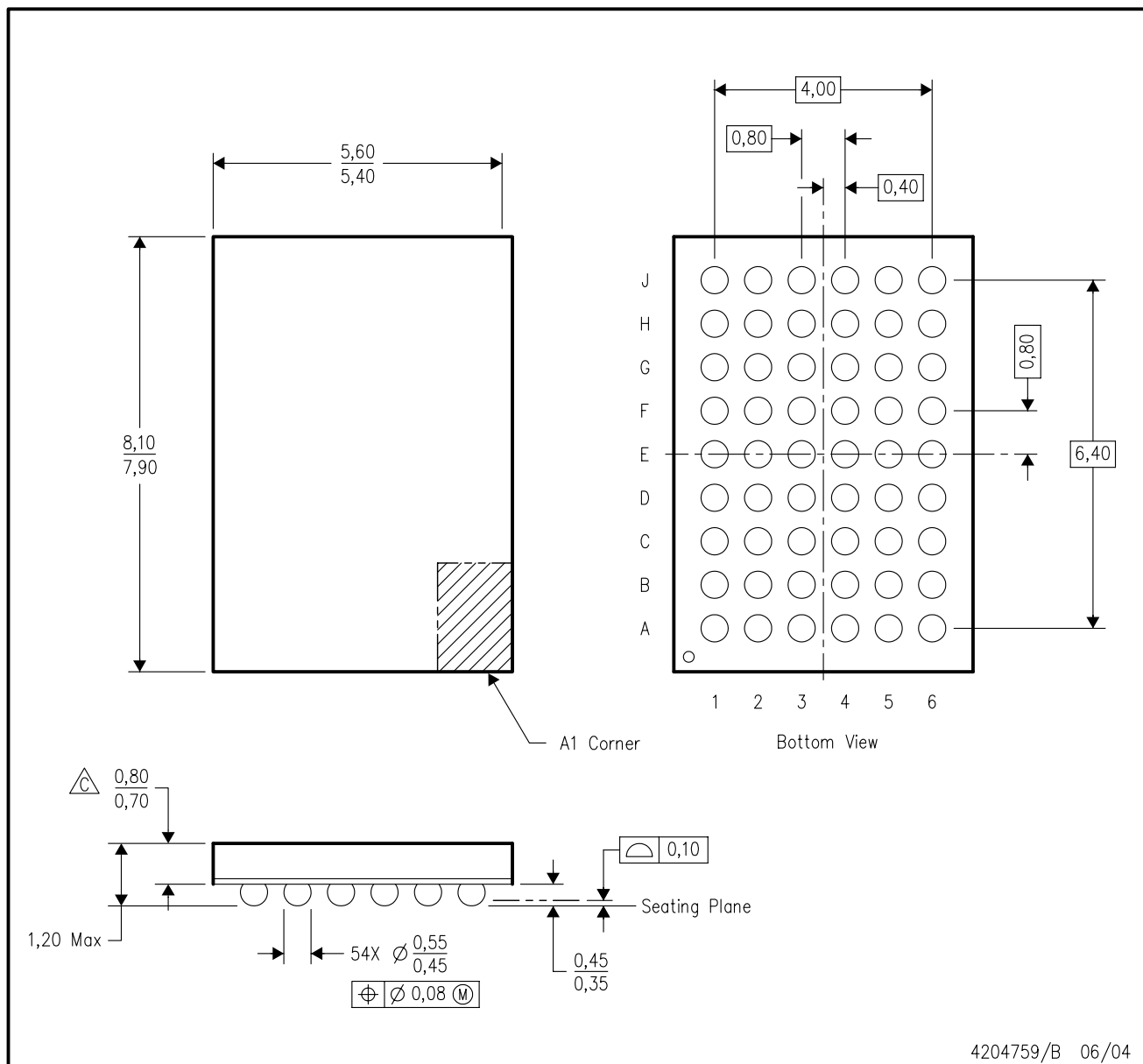
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

## GRD (R-PBGA-N54)

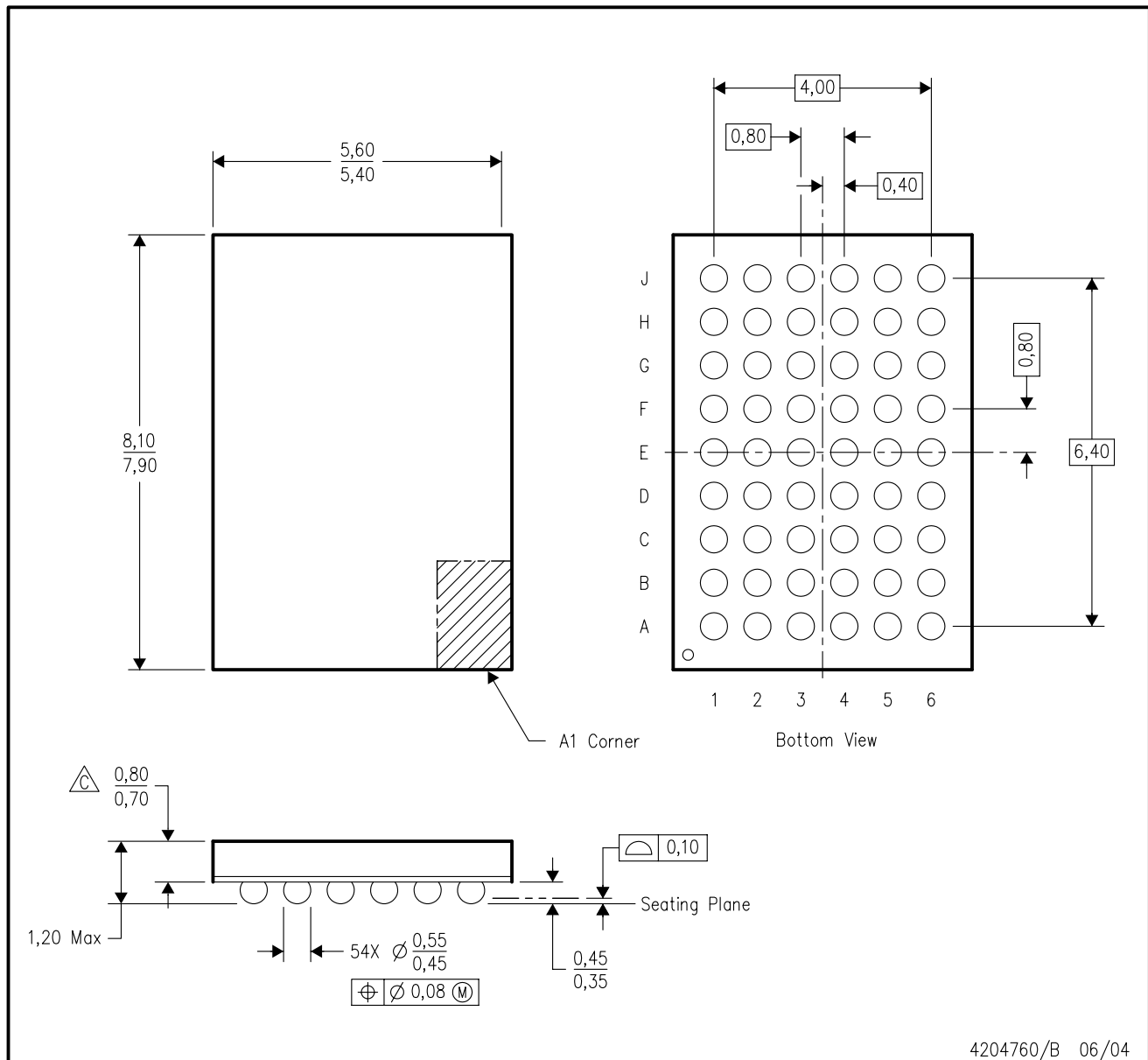
## PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DD.
  - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

## ZRD (R-PBGA-N54)

## PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DD.
  - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

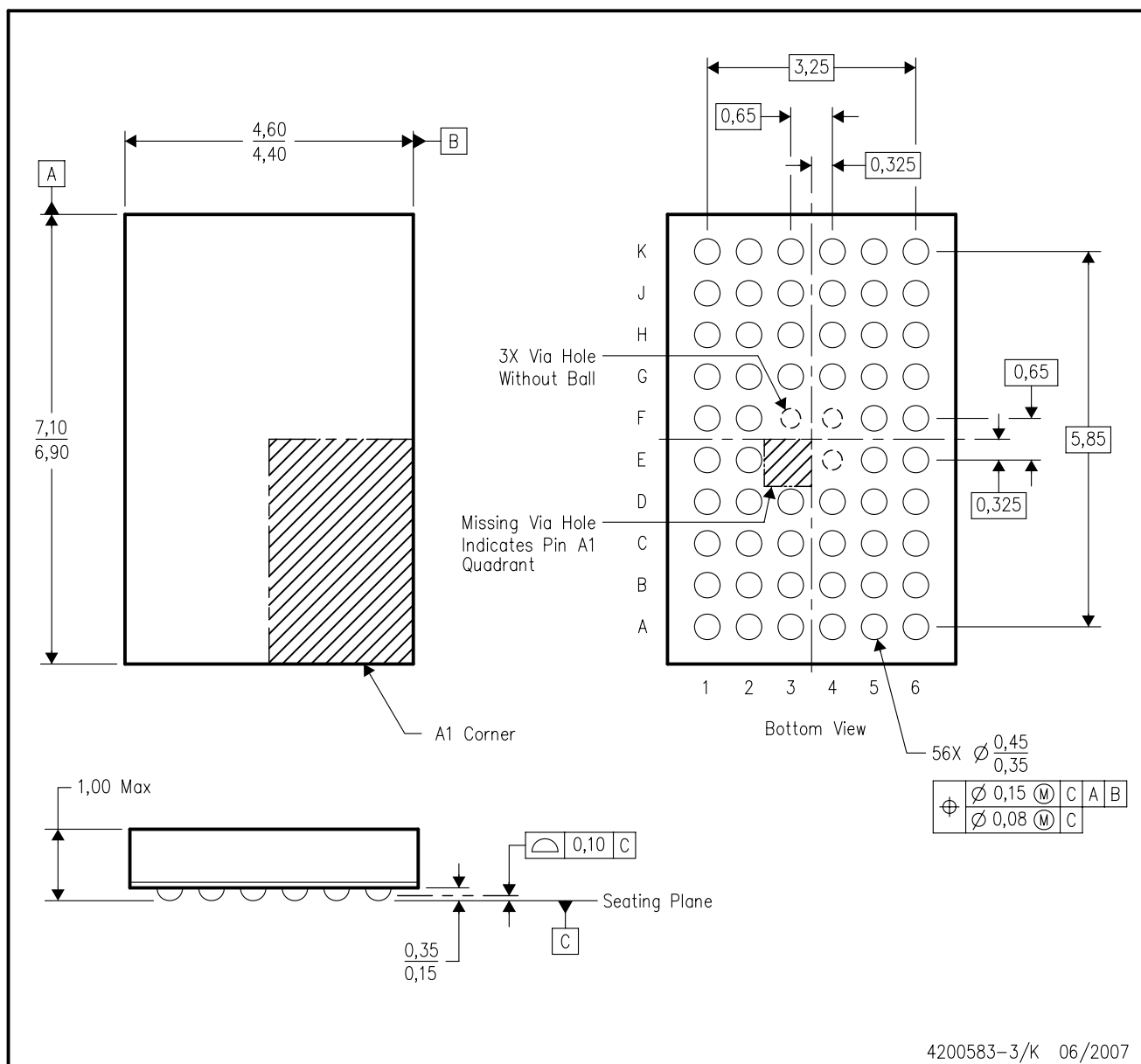
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Falls within JEDEC MO-285 variation BA-2.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

**DGG (R-PDSO-G\*\*)****PLASTIC SMALL-OUTLINE PACKAGE****48 PINS SHOWN**

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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