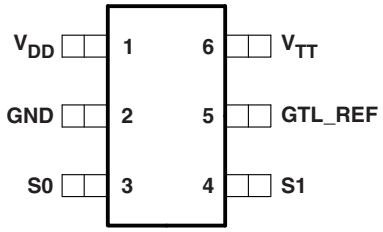
SELECTABLE GTL VOLTAGE REFERENCE

FEATURES

- V_{DD} Range: 3.0 V to 3.6 V
- V_{TT} Range: 1 V to 1.3 V
- Provides Selectable GTL V_{REF}
  - $0.615 \times V_{TT}$
  - $0.63 \times V_{TT}$
  - $0.65 \times V_{TT}$
  - $0.67 \times V_{TT}$
- ±1% Resistor Ratio Tolerance
- Ambient Temperature Range: –40°C to 85°C
- ESD Protection Exceeds the Following Levels Tests (Tested Per JESD-22):
  - 2500-V Human-Body Model (A114-B, Class II)
  - 250-V Machine Model (A115-A)
  - 1500-V Charged-Device Model (C101)

DCK PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74GTL3004 provides for a selectable GTL Voltage Reference (GTL V_{REF}). The value of the GTL V_{REF} can be adjusted using S0 and S1 select pins.

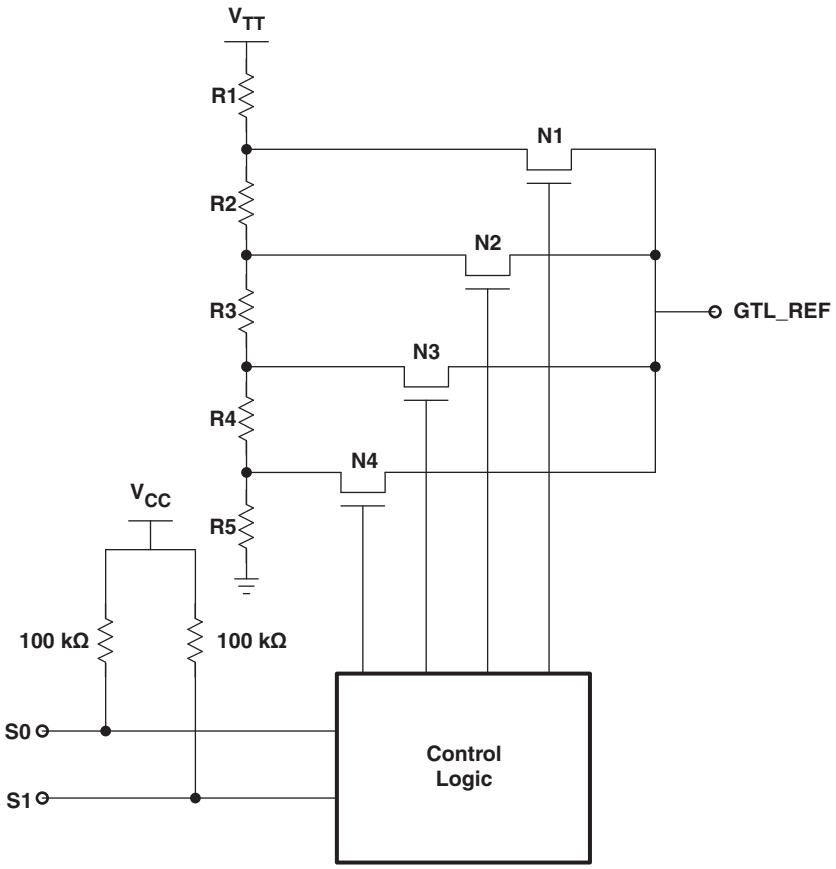
The S0 and S1 pins contain glitch-suppression circuitry for excellent noise immunity. When left floating, the S0 and S1 control input pins have 100-kΩ pullups that set the GTL V_{REF} default value to the $0.67 \times V_{TT}$ ratio (S0 = 1 and S1 =1).

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT (SC70) – DCK	Tape and reel	SN74GTL3004DCKR	2TK

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM



FUNCTION TABLE

S1	S0	RATIO SET
0	0	$0.615 \times V_{TT}$
0	1	$0.63 \times V_{TT}$
1	0	$0.65 \times V_{TT}$
1	1	$0.67 \times V_{TT}$

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Power supply voltage range		–0.3	4.6	V
V_{TT}	Termination voltage range(2)		–0.3	4.6	V
V_{IN}	Control input voltage range (2)		–0.3	V_{DD} + 0.3	V
V_{GTL_REF}	Resistor output voltage range(2)		–0.3	V_{DD} + 0.3	V
I_{IK}	Input clamp current	V_{IN} < 0		–18	mA
I_{OK}	Output clamp current	V_O < 0		–18	mA
	Continuous current through V_{DD} or GND			100	mA
θ_{JA}	Package thermal impedance(3)	DCK package		259	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power supply voltage	3	3.3	3.6	V
V_{TT}	Termination voltage	1	1.1	1.3	V
V_{IH}	High-level control input voltage	$V_{DD} \times 0.65$			V
V_{IL}	Low-level control input voltage			$V_{DD} \times 0.35$	V
V_I	Control input voltage	0		V_{DD}	V
I_{OUT}	I_{GTL_REF}, GTL_REF output current		0	10	µA
PW	Control input pulse width	110			ns
T_A	Operating free-air temperature	–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow of Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = –40°C to 85°C, V_{DD} = 3.3 V ±10%, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Control	V_{DD} = 3.6 V, I_{IN} = –18 mA			–1.8	V
I_{IN}	Control	V_{DD} = 3.6 V, V_{IN} = GND			43	µA
I_{DD}		V_{DD} = 3.6 V, V_{IN} = GND, I_O = 0 mA			85	µA
R	End-to-end resistance	V_{DD} = 3.6 V, V_{TT} = 1.1 V, I_O = 0 mA	4.25	7.12	10.6	kΩ
	GTL V_{REF} accuracy(1)	I_O = 0 µA, See Figure 1	–1		1	%
		I_O = 10 µA, See Figure 1	–7		7	

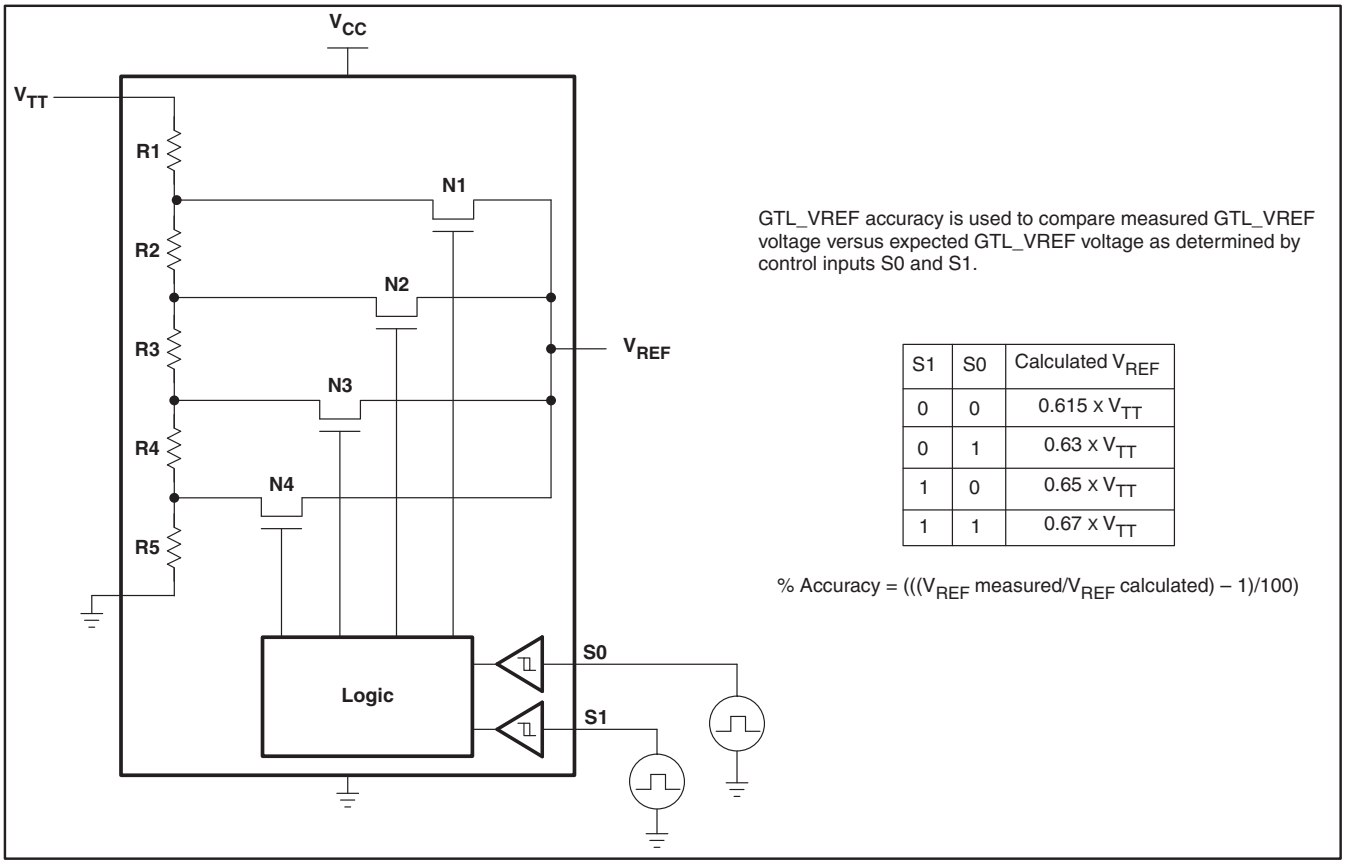
(1) GTL V_{REF} accuracy is used to compare measured GTL_VREF voltage versus expected GTL_VREF voltage as determined by control inputs S0 and S1. The resistor ratio tolerance is incorporated into this parameter.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,, T_A = –40°C to 85°C, V_{DD} = 3.3 V ±10%, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSR	Power supply rejection			–58		dB
	Pulse rejection				40	ns

PARAMETER MEASUREMENT INFORMATION



GTL_VREF accuracy is used to compare measured GTL_VREF voltage versus expected GTL_VREF voltage as determined by control inputs S0 and S1.

S1	S0	Calculated V_{REF}
0	0	0.615 x V_{TT}
0	1	0.63 x V_{TT}
1	0	0.65 x V_{TT}
1	1	0.67 x V_{TT}

% Accuracy = ((V_{REF} measured/V_{REF} calculated) – 1)/100)

Figure 1. GTL_REF Accuracy

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74GTL3004DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL3004DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

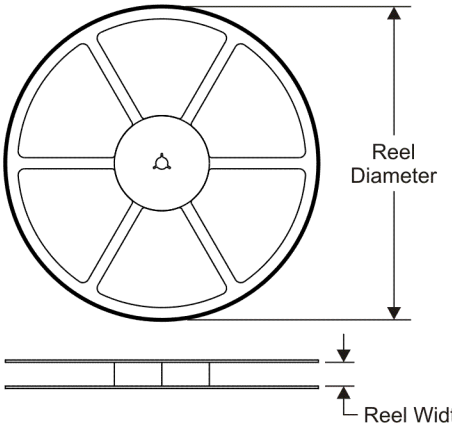
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

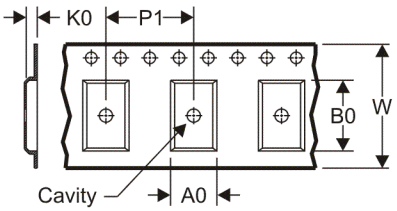
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

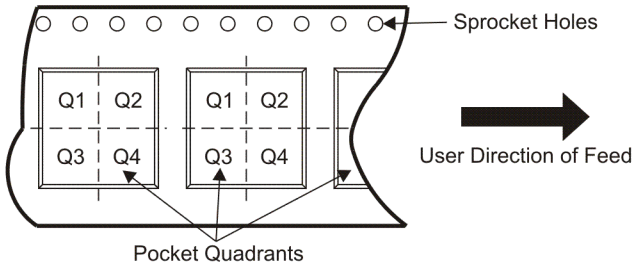


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

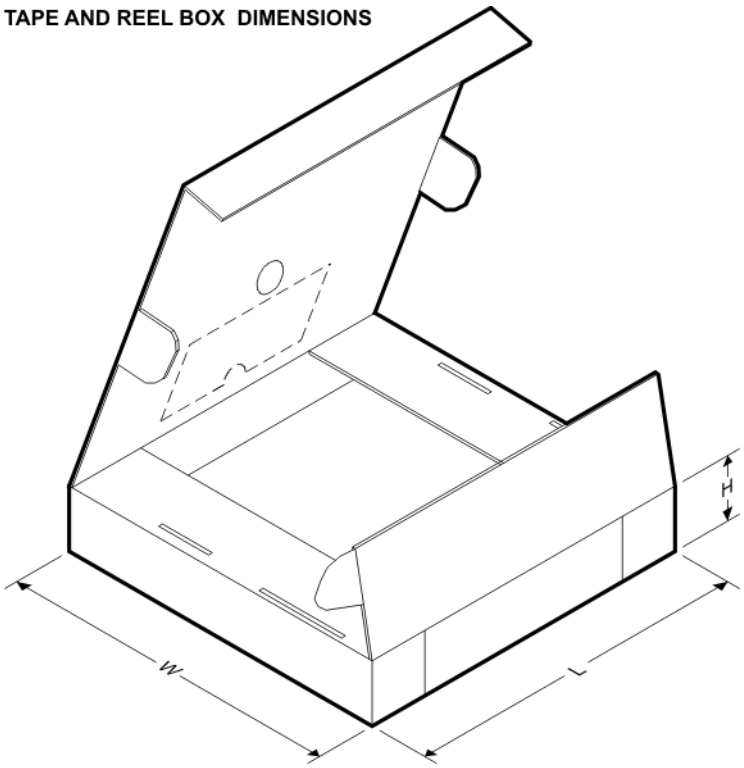
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL3004DCKR	SC70	DCK	6	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3

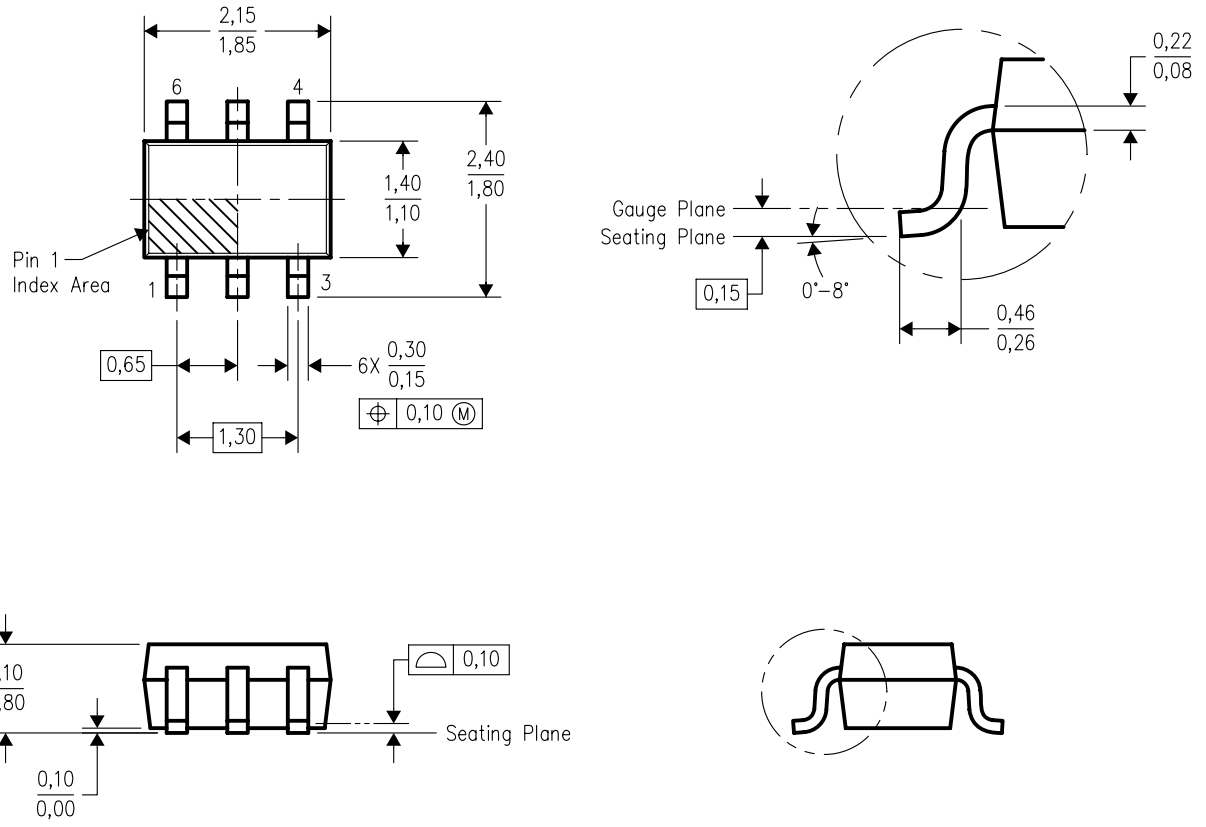
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL3004DCKR	SC70	DCK	6	3000	205.0	200.0	33.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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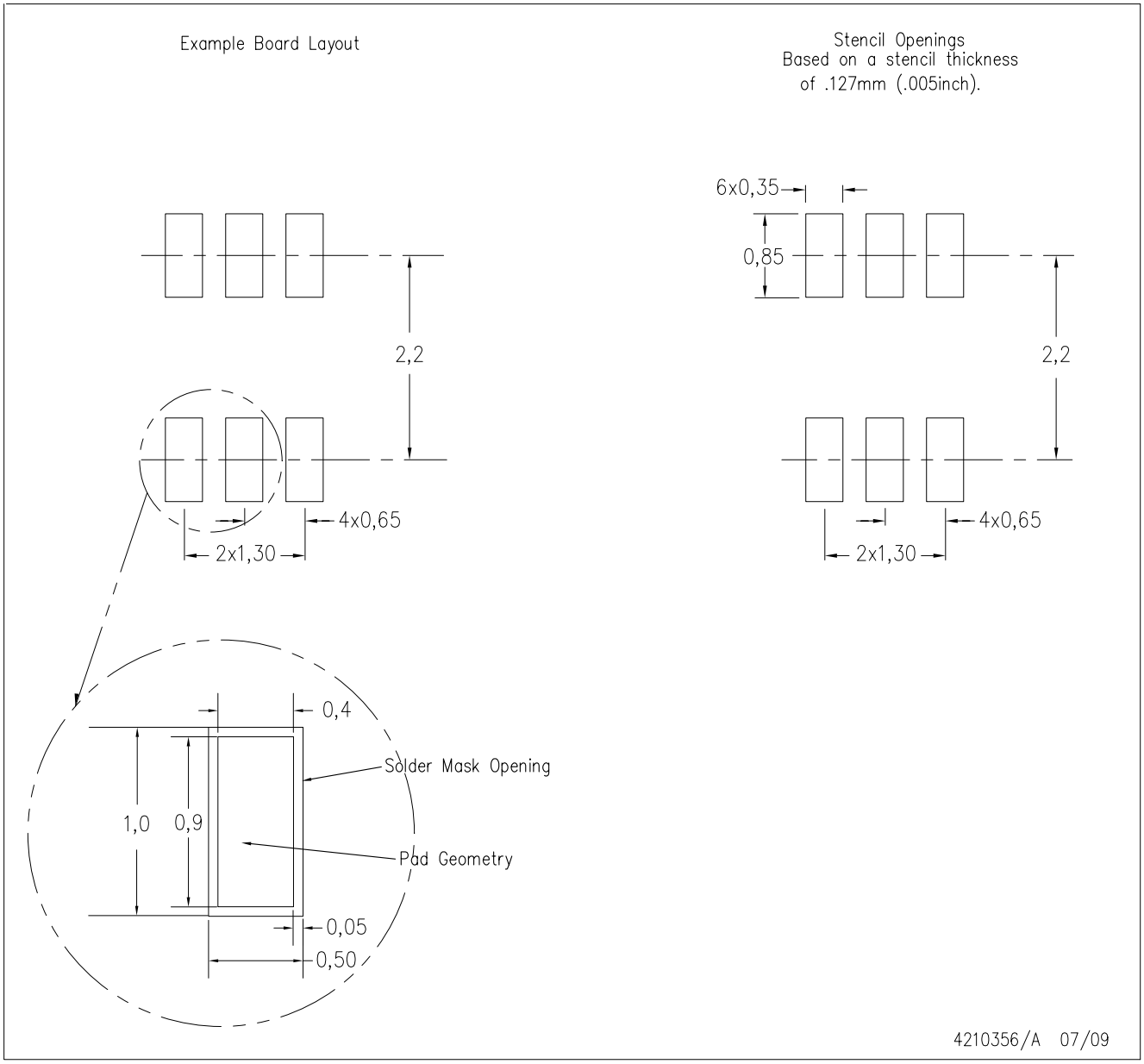
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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