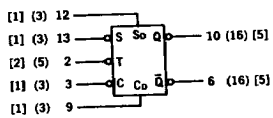
MC726P · MC826P

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



f_{req} = 4 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

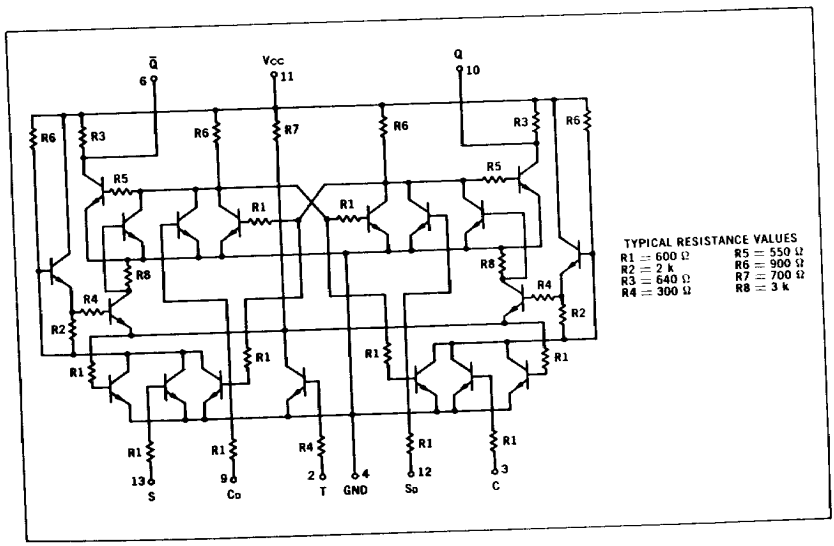
t_n ③		t_{n+1} ③	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

DIRECT INPUT OPERATION ④

So	Co	Q	$\bar{Q}$
0	0	⑤	⑤
1	0	1	0
0	1	0	1
1	1	0	0

1. Direct inputs (C_D and So) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from So = $\bar{C}_D$ to So = C_D = 0. The output state cannot be predetermined in the case where the input goes from So = C_D = 1 to So = C_D = 0.
6. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESES INDICATES LOADING FACTOR FOR mW MRTL
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL



TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 k	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 k

	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}
MC826P	0°C	0.960	0.930	1.80	0.570	3.60
	+25°C	0.910	0.880	1.80	0.500	3.60
	+75°C	0.820	0.790	1.80	0.450	3.60
MC726P	+15°C	0.865	0.865	1.80	0.475	3.60
	+25°C	0.850	0.850	1.80	0.460	3.60
	+55°C	0.800	0.800	1.80	0.430	3.60

ELECTRICAL CHARACTERISTICS

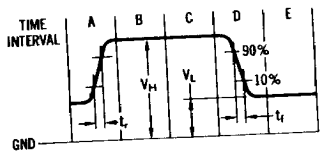
Characteristic	Symbol	Pin Under Test	MC826P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC726P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{in}	V_{on}	V_{BOT}	V_{off}	V_{CC}	Gnd
Input Current	$2I_{in}$	2	-	1200	-	1200	-	1140	μAdc	-	1000	-	1000	-	940	μAdc	2	-	3, 13	-	11	4
	I_{in}	3	-	600	-	600	-	570		-	500	-	500	-	470		3	-	12	-		
		9	-		-		-			-		-		-			9	-	-	-		
		12	-		-		-			-		-		-			12	-	-	-		
		13	-		-		-			-		-		-			13	-	9	-		
Output Current	I_{A5}	6	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	6, 12	9	-	11	4
		10	3.0	-	3.0	-	2.85	-	mAdc	2.65	-	2.65	-	2.5	-	mAdc	-	9, 10	12	-	11	4
Saturation Voltage	$V_{CE(sat)}$	6	-	400	-	300	-	350	mVdc	-	300	-	290	-	320	mVdc	-	12	-	9	11	4
		6*#	-		-		-			-		-		-			-	13	-	3		
		6*#	-		-		-			-		-		-			-	-	-	3, 13		
		6*##	-		-		-			-		-		-			-	3, 13	-	-		
		10	-		-		-			-		-		-			-	9	-	12		
		10*##	-		-		-			-		-		-			-	3	-	13		
		10*#	-		-		-			-		-		-			-	3, 13	-	-		
		10*##	-		-		-			-		-		-			-	-	-	3, 13		

Pins not listed are left open.

* Clock Pulse to pin 2, see Figure 1.

Pin 9 HIGH
Pin 12 HIGH
} Set by momentary application of V_{BOT} prior to the application of the negative-going clock pulse.

FIGURE 1 — CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical but should be $< 1.0\ \mu s$.
B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.
C. Apply momentary ground (when applicable).
D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 100 ns maximum.
E. Electrical measurements are read out. Load current over-shoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.

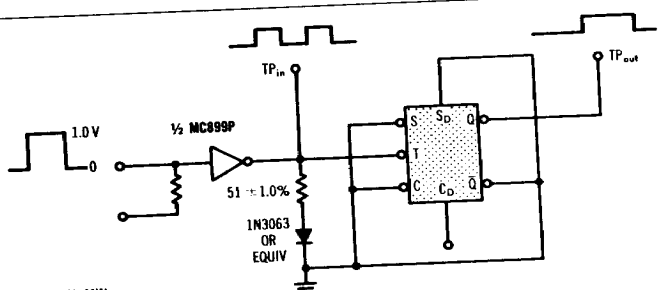
MC826P

T_A	V_L	V_H
+ 25°C	+ 0.500 V ± 2.0 mV	+ 0.930 V ± 2.0 mV
0°C	+ 0.570 V ± 2.0 mV	+ 0.980 V ± 2.0 mV
+ 75°C	+ 0.450 V ± 2.0 mV	+ 0.840 V ± 2.0 mV

MC726P

T_A	V_L	V_H
+ 25°C	+ 0.460 V ± 2.0 mV	+ 0.900 V ± 2.0 mV
+ 15°C	+ 0.475 V ± 2.0 mV	+ 0.915 V ± 2.0 mV
+ 55°C	+ 0.430 V ± 2.0 mV	+ 0.850 V ± 2.0 mV

FIGURE 2 — TOGGLE MODE TEST CIRCUIT



f = 4.0 MHz MIN
DUTY CYCLE = 25% MIN., 75% MAX.
t_r & t_f < 10 ns

OUTPUT FREQUENCY SHALL BE ½ OF TP_{in} FREQUENCY.