Isolated Half-Bridge Driver, 0.1 A Amp Output

ADuM1230

FEATURES

- Isolated high-side and low-side outputs
  - High-side or low-side relative to input: ±700 V_{PEAK}
  - High-side/low-side differential: 700 V_{PEAK}
- 0.1 A peak output current
- High frequency operation: 5 MHz max
- High common-mode transient immunity: >50 kV/µs
- High temperature operation: 105°C
- Wide body, 16-lead SOIC
- UL1577 2500 V rms input-to-output withstand voltage

APPLICATIONS

- Isolated IGBT/MOSFET gate drives
- Plasma displays
- Industrial inverters
- Switching power supplies

GENERAL DESCRIPTION

The ADuM1230[1] is an isolated half-bridge gate driver that employs Analog Devices' *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to optocoupler-based solutions.

By avoiding the use of LEDs and photodiodes, this *i*Coupler gate drive device is able to provide precision timing characteristics not possible with optocouplers. Furthermore, the reliability and performance stability problems associated with optocoupler LEDs are avoided.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM1230 offers the benefit of true, galvanic isolation between the input and each output. Each output may be operated up to ±700 V_P relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high-side and low-side can be as high as 700 V_P.

As a result, the ADuM1230 provides reliable control over the switching characteristics of IGBT/MOSFET configurations over a wide range of positive or negative switching voltages.

[1] Protected by U.S. Patents 5,952,849 6,873,065, and other pending patents.

FUNCTIONAL BLOCK DIAGRAM

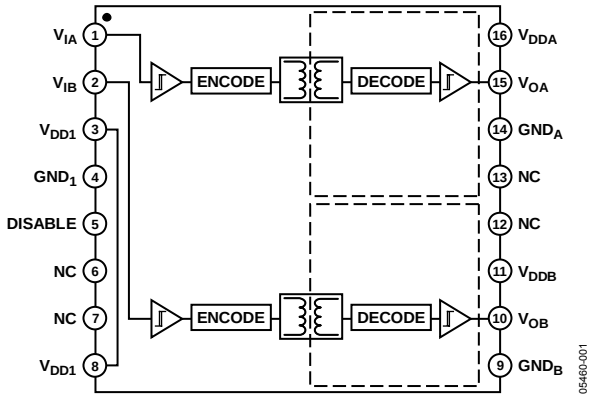

Figure 1.

Rev. A

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REVISION HISTORY

12/05—Rev. Sp0 to Rev. A

Changes to Figure 1 and Note 1 1
Added Typical Application Usage Section 9
Inserted Figure 14 9

5/05—Revision Sp0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 12 V ≤ V_{DDA} ≤ 18 V, 12 V ≤ V_{DDB} ≤ 18 V. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DDA} = 15 V, V_{DDB} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI (Q)}$			4.0	mA	
Output Supply Current, A or B, Quiescent	$I_{DDA (Q)}$, $I_{DDB (Q)}$			1.2	mA	
Input Supply Current, 10 Mbps	$I_{DDI (10)}$			8.0	mA	
Output Supply Current, A or B, 10 Mbps	$I_{DDA (10)}$, $I_{DDB (10)}$			22	mA	C_L = 200 pF
Input Currents	I_{IA}, I_{IB}, $I_{DISABLE}$	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB}, $V_{DISABLE}$ ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	2.0			V	
Logic Low Input Threshold	V_{IL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DDA} − 0.1, V_{DDB} − 0.1	V_{DDA}, V_{DDB}		V	I_{OA}, I_{OB} = −1 mA
Logic Low Output Voltages	V_{OAL}, V_{OBL}			0.1	V	I_{OA}, I_{OB} = 1 mA
Output Short-Circuit Pulsed Current[1]	$I_{OA (SC)}$, $I_{OB (SC)}$	100			mA	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 200 pF
Maximum Switching Frequency[3]		10			Mbps	C_L = 200 pF
Propagation Delay[4]	t_{PHL}, t_{PLH}	97	124	160	ns	C_L = 200 pF
Change vs. Temperature			100		ps/°C	
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			8	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising or Falling Edges[5]				5	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising vs. Falling Edges[6]				13	ns	C_L = 200 pF
Part-to-Part Matching, Rising or Falling Edges[7]				55	ns	C_L = 200 pF
Part-to-Part Matching, Rising vs. Falling Edges[8]				63	ns	C_L = 200 pF
Output Rise/Fall Time (10% to 90%)	t_R/t_F			20	ns	C_L = 200 pF

[1] Short-circuit duration less than 1 second. Average power must conform to the limit shown under the Absolute Maximum Ratings.
[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed.
[3] The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] Channel-to-channel matching, rising vs. falling edges is the magnitude of the propagation delay difference between two channels of the same part when the inputs are either both rising edges or falling edges. The supply voltages and the loads on each channel are equal.
[6] Channel-to-channel matching, rising or falling edges is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and the other input is a falling edge. The supply voltages and loads on each channel are equal.
[7] Part-to-part matching, rising or falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.
[8] Part-to-part matching, rising vs. falling edges is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JCa}		76		°C/W	

[1] The device is considered a 2-terminal device: Pins 1 through 8 are shorted together, and Pins 9 through 16 are shorted together.

REGULATORY INFORMATION

The ADuM1230 is approved, as shown in Table 3.

Table 3.

UL[1]
Recognized under 1577 component recognition program

[1] In accordance with UL1577, each ADuM1230 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	4.5	5.5	V
Output Supply Voltages[1]	V_{DDA}, V_{DDB}	12	18	V
Input Signal Rise and Fall Times			1	ms
Common-Mode Transient Immunity, Input-to-Output[2]		−50	+50	kV/µs
Common-Mode Transient Immunity, Between Outputs[2]		−50	+50	kV/µs
Transient Immunity, Supply Voltages[2]		−50	+50	kV/µs

[1] All voltages are relative to their respective ground.
[2] See the Common-Mode Transient Immunity section for transient diagrams and additional information.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	−55	+150	°C
Ambient Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD1}	−0.5	+7.0	V
Output Supply Voltage[1]	V_{DDA}, V_{DDB}	−0.5	+27	V
Input Voltage[1]	V_{IA}, V_{IB}	−0.5	V_{DDI} + 0.5	V
Output Voltage[1]	V_{OA}, V_{OB}	−0.5	V_{DDA} + 0.5, V_{DDB} + 0.5	V
Input-Output Voltage[2]		−700	+700	V_{PEAK}
Output Differential Voltage[3]			700	V_{PEAK}
Output DC Current	I_{OA}, I_{OB}	−20	+20	mA
Common-Mode Transients[4]		−100	+100	kV/µs

[1] All voltages are relative to their respective ground.
[2] Input-to-output voltage is defined as $GND_A - GND_1$ or $GND_B - GND_1$.
[3] Output differential voltage is defined as $GND_A - GND_B$.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

Table 7. ADuM1230 Truth Table (Positive Logic)

V_{IA}/V_{IB} Input	V_{DD1} State	DISABLE	V_{OA}/V_{OB} Output	Notes
H	Powered	L	H	
L	Powered	L	L	
X	Unpowered	X	L	Output returns to input state within 1 µs of V_{DDI} power restoration.
X	Powered	H	L	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

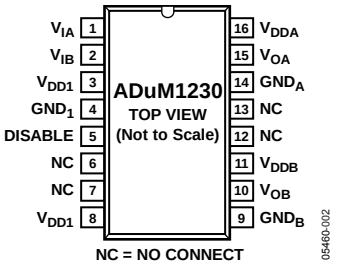


Figure 2. Pin Configuration

Note that Pin 3 and Pin 8 are internally connected. Connecting both to V_{DD1} is recommended. Pin 12 and Pin 13 are floating and should be left unconnected.

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{IA}	Logic Input A.
2	V_{IB}	Logic Input B.
3	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V.
4	GND_1	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits. Outputs take on default low state.
6, 7, 12, 13	NC	No Connect.
8	V_{DD1}	Input Supply Voltage, 4.5 V to 5.5 V.
9	GND_B	Ground Reference for Output B.
10	V_{OB}	Output B.
11	V_{DDB}	Output B Supply Voltage, 12 V to 18 V.
14	GND_A	Ground Reference for Output A.
15	V_{OA}	Output A.
16	V_{DDA}	Output A Supply Voltage, 12 V to 18 V.

TYPICAL PERFORMANCE CHARACTERISTICS

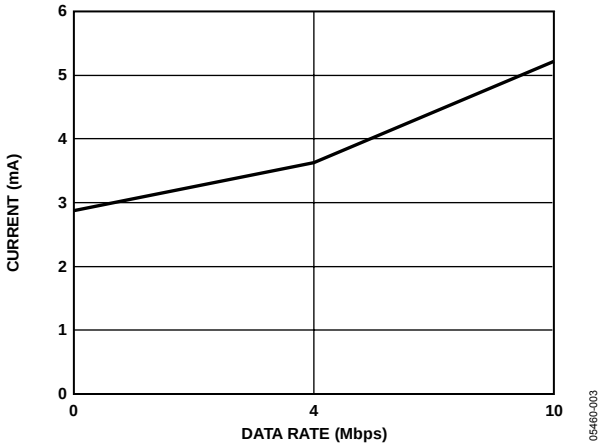


Figure 3. Typical Input Supply Current Variation with Data Rate

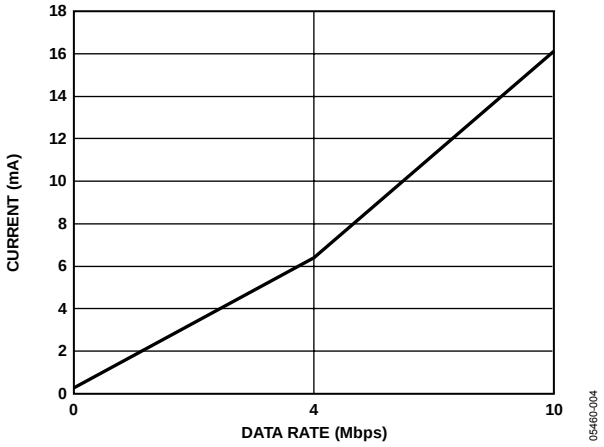


Figure 4. Typical Output Supply Current Variation with Data Rate

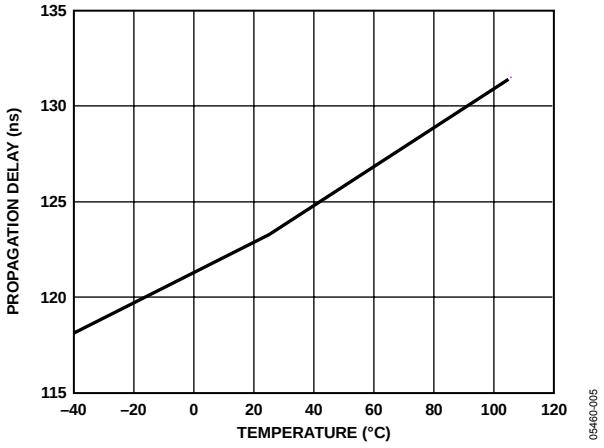


Figure 5. Typical Propagation Delay Variation with Temperature

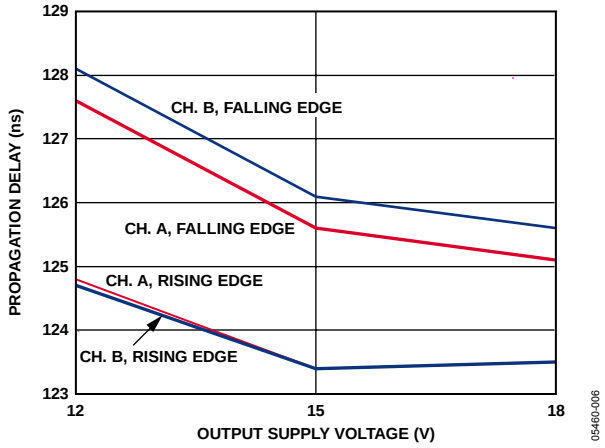


Figure 6. Typical Propagation Delay Variation with Output Supply Voltage (Input Supply Voltage = 5.0 V)

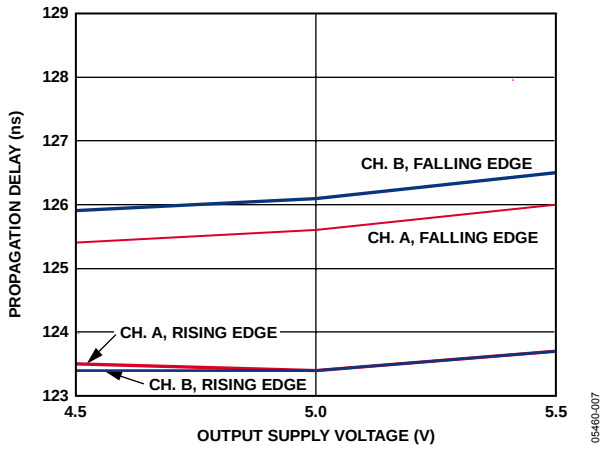


Figure 7. Typical Propagation Delay Variation with Input Supply Voltage (Output Supply Voltage = 15.0 V)

APPLICATION NOTES

COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM,\,linear} = (\Delta V/\Delta t)\,t$$

where ΔV/Δt is the slope of the transient shown in Figure 11 and Figure 12.

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

The ADuM1230's ability to operate correctly in the presence of linear transients is characterized by the data in Figure 8. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM1230 can tolerate without an operational error. This data shows a higher level of robustness than what is shown in Table 5 because the transient immunity values obtained in Table 5 use measured data and apply allowances for measurement error and margin.

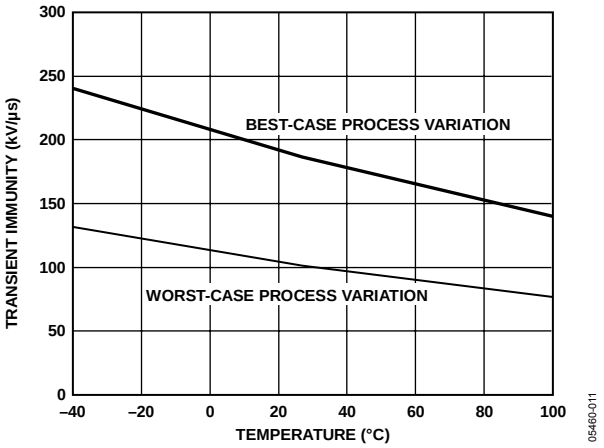


Figure 8. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM,\,sinusoidal} = V_0 \sin(2\pi f t)$$

where:

V_0 is the magnitude of the sinusoidal.

f is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f\,V_0$$

The ADuM1230's ability to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 9 and Figure 10. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f\,V_0$) that the ADuM1230 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 5 because measurements to obtain such values have not been possible.

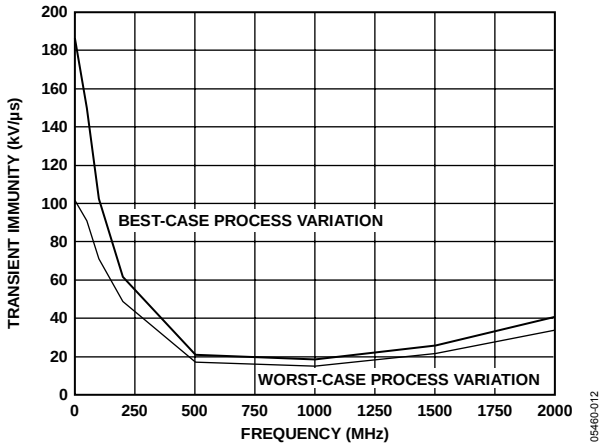


Figure 9. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature

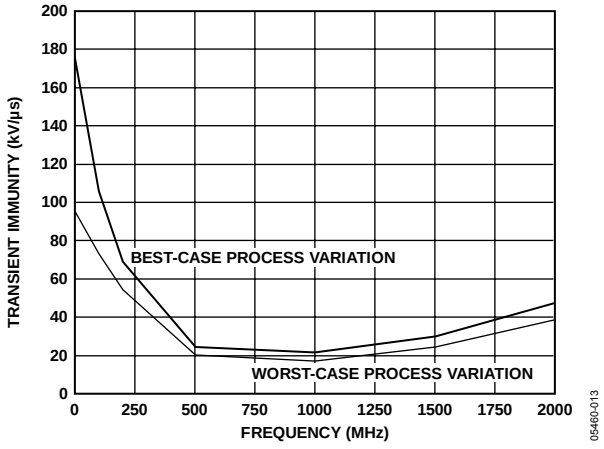


Figure 10. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

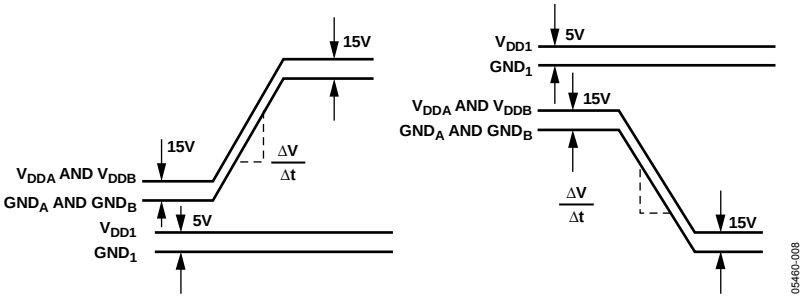


Figure 11. Common-Mode Transient Immunity Waveforms—Input to Output

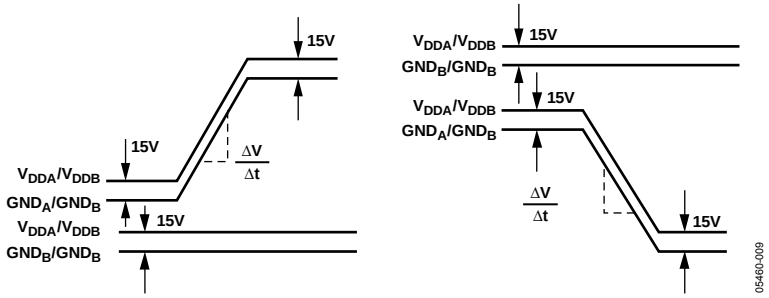


Figure 12. Common-Mode Transient Immunity Waveforms—Between Outputs

Figure 13. Transient Immunity Waveforms—Output Supplies

TYPICAL APPLICATION USAGE

The ADuM1230 is intended for driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these situations, users can choose either a gate driver with a stronger output stage or the buffer configuration with the ADuM1230, as shown in Figure 14. In many cases, the buffer configuration is the less expensive of the two options and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to fit the application's needs.

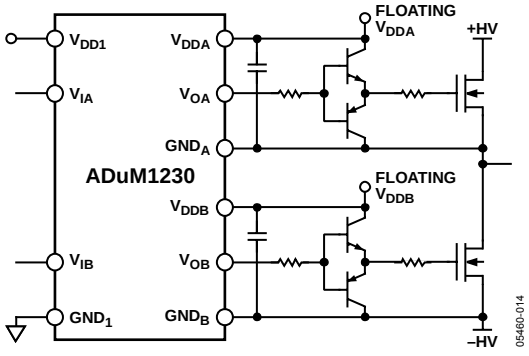
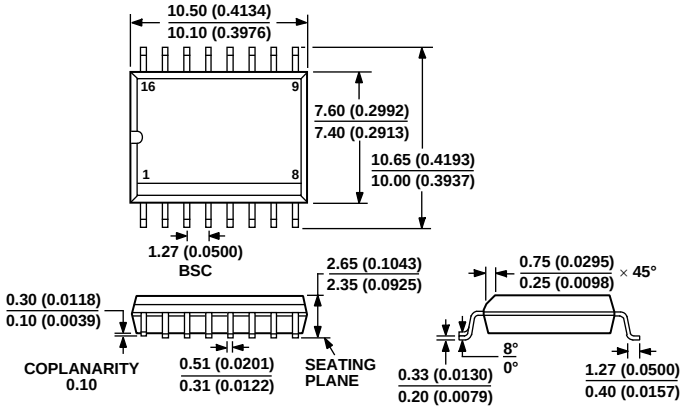


Figure 14.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 15. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM1230BRWZ[1]	2	0.1	15	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM1230BRWZ-RL[1]	2	0.1	15	−40°C to +105°C	16-Lead SOIC_W, 13-inch Tape and Reel Option (1, 000 Units)	RW-16

[1] Z = Pb-free part.

NOTES

NOTES

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