# TLE7189QK

3-Phase Bridge Driver IC

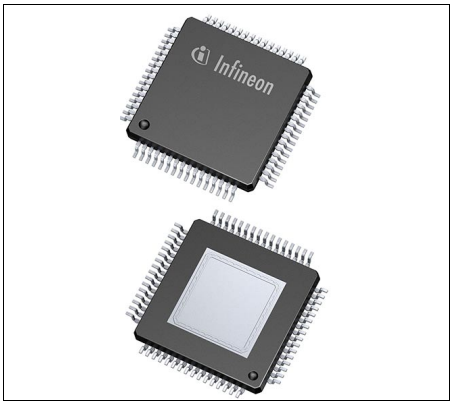
## Data Sheet

Rev. 2.2, 2016-01-28

Automotive Power

# Table of Contents

# 1 Overview




**PG-LQFP-64**

### Features

- Compatible to very low ohmic normal level input N-channel MOSFETs
- PWM frequency up to 30kHz
- Fulfils specification down to 5.5V supply voltage
- Short circuit protection with adjustable detection level
- Three integrated current sense amplifiers
- 0 to 100% duty cycle
- Low EMC sensitivity and emission
- Control inputs with TTL characteristics
- Separate input for each MOSFET
- Separate source connection for each MOSFET
- Integrated minimum dead time
- Shoot through protection
- Disable function and sleep mode
- Detailed diagnosis
- Over temperature warning
- LQFP-64 package with exposed pad for excellent cooling
- Green Product (RoHS compliant)
- AEC (Automotive Electronics Council) qualified

### SIL supporting features:

- VCC check: Over- and under voltage check of 5V µC supply
- Test functions for short circuit detection and VCC check
- High voltage rated inputs

### Description

The TLE7189QK is a driver IC dedicated to control the 6 to 12 external MOSFETs forming the converter for high current 3 phase motor drives in the automotive sector. It incorporates features like short circuit detection, diagnosis and high output performance and combines it with typical automotive specific requirements like full functionality even at low battery voltages. Its 3 high side and 3 low side output stages are powerful enough to drive MOSFETs with 400nC gate charge with approx. 150ns fall and rise times.

| Type | Package | Marking |
|---|---|---|
| TLE7189QK | PG-LQFP-64 | TLE7189QK |

# 2 Block Diagram

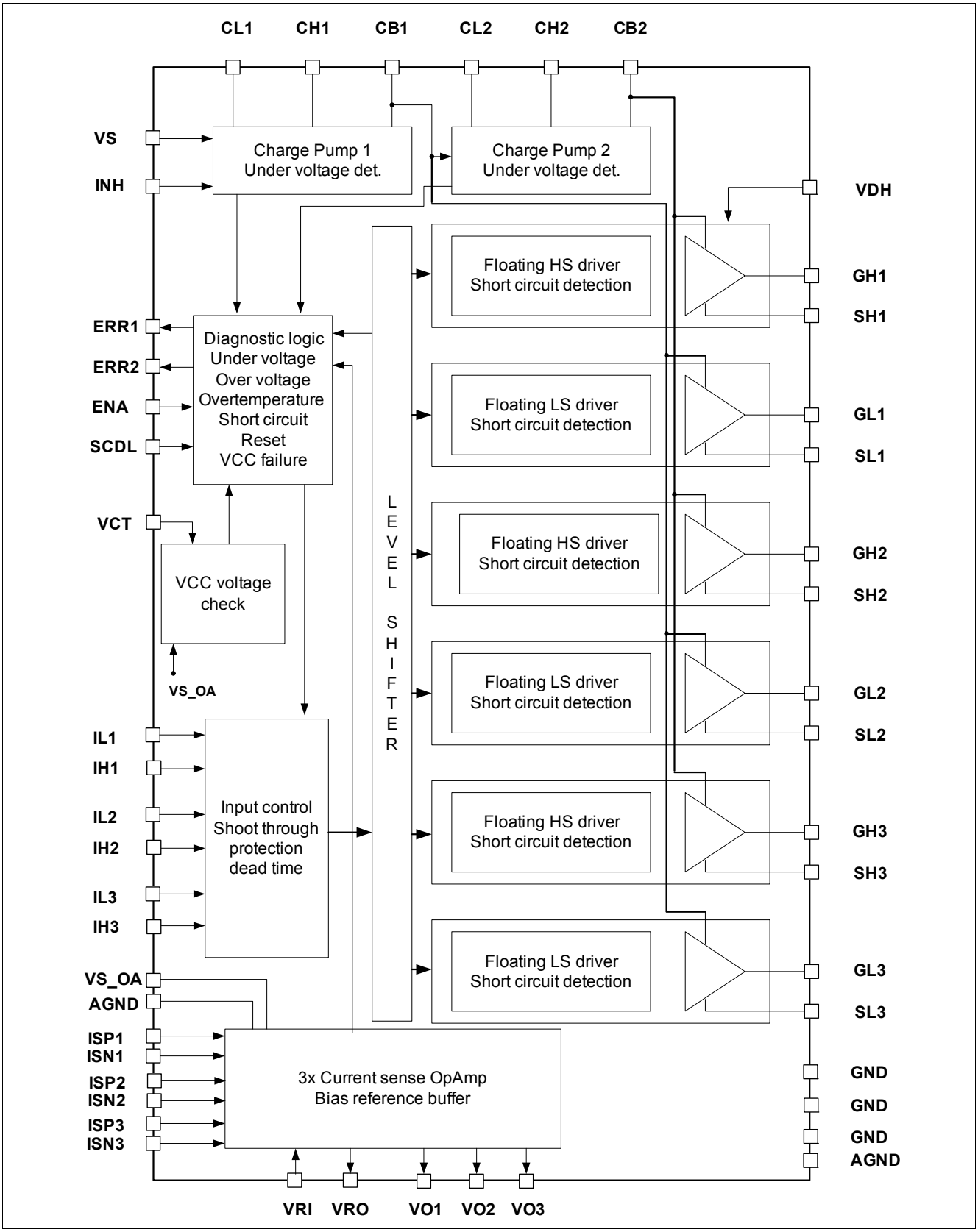



**Figure 1 Block Diagram**

# 3 Pin Configuration

## 3.1 Pin Assignment TLE7189QK

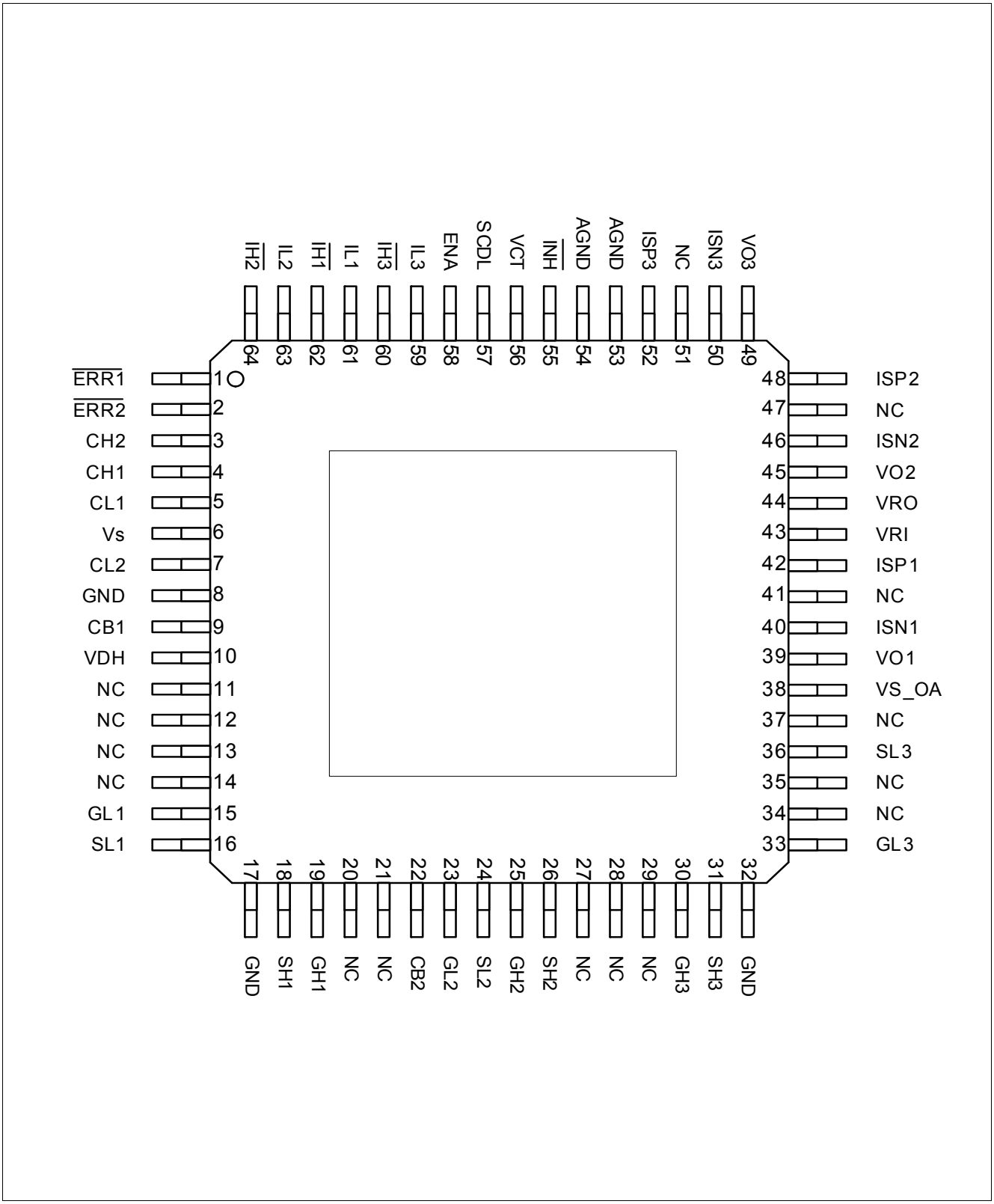



**Figure 2 Pin Configuration**

## 3.2 Pin Definitions and Functions.

| Pin | Symbol | Function |
|---|---|---|
| 1 | ERR1 | Error signal 1 |
| 2 | ERR2 | Error signal 2 |
| 3 | CH2 | + terminal for pump capacitor of charge pump 2 |
| 4 | CH1 | + terminal for pump capacitor of charge pump 1 |
| 5 | CL1 | - terminal for pump capacitor of charge pump 1 |
| 6 | VS | Voltage supply |
| 7 | CL2 | - terminal for pump capacitor of charge pump 2 |
| 8 | GND | Logic and power ground |
| 9 | CB1 | Buffer capacitor for charge pump 1 |
| 10 | VDH | Connection to drain of high side switches for short circuit detection |
| 11 | NC | Not connected |
| 12 | NC | Not connected |
| 13 | NC | Not connected |
| 14 | NC | Not connected |
| 15 | GL1 | Output to gate low side switch 1 |
| 16 | SL1 | Connection to source low side switch 1 |
| 17 | GND | Logic and power ground |
| 18 | SH1 | Connection to source high side switch 1 |
| 19 | GH1 | Output to gate high side switch 1 |
| 20 | NC | Not connected |
| 21 | NC | Not connected |
| 22 | CB2 | Buffer capacitor for charge pump 2 |
| 23 | GL2 | Output to gate low side switch 2 |
| 24 | SL2 | Connection to source low side switch 2 |
| 25 | GH2 | Output to gate high side switch 2 |
| 26 | SH2 | Connection to source high side switch 2 |
| 27 | NC | Not connected |
| 28 | NC | Not connected |
| 29 | NC | Not connected |
| 30 | GH3 | Output to gate high side switch 3 |
| 31 | SH3 | Connection to source high side switch 3 |
| 32 | GND | Logic and power ground |
| 33 | GL3 | Output to gate low side switch 3 |
| 34 | NC | Not connected |
| 35 | NC | Not connected |
| 36 | SL3 | Connection to source low side switch 3 |
| 37 | NC | Not connected |
| 38 | VS_OA | Voltage supply I-DC Link OpAmps and voltage reference buffer / input for VCC check |
| 39 | VO1 | Output of OpAmp 1 for shunt signal amplification |
| 40 | ISN1 | - Input of OpAmp 1 for shunt signal amplification |

| Pin | Symbol | Function |
|---|---|---|
| 41 | NC | Not connected |
| 42 | ISP1 | + Input of OpAmp 1 for shunt signal amplification |
| 43 | VRI | Input of bias reference amplifier |
| 44 | VRO | Output of bias reference amplifier |
| 45 | VO2 | Output of OpAmp 2 for shunt signal amplification |
| 46 | ISN2 | - Input of OpAmp 2 for shunt signal amplification |
| 47 | NC | Not connected |
| 48 | ISP2 | + Input of OpAmp 2 for shunt signal amplification |
| 49 | VO3 | Output of OpAmp 3 for shunt signal amplification |
| 50 | ISN3 | - Input of OpAmp 3 for shunt signal amplification |
| 51 | NC | Not connected |
| 52 | ISP3 | + Input of OpAmp 3 for shunt signal amplification |
| 53 | AGND | Analog ground especially for the current sense OpAmps |
| 54 | AGND | Analog ground especially for the current sense OpAmps |
| 55 | INH | Inhibit pin (active low) |
| 56 | VCT | Input pin for VCC check test |
| 57 | SCDL | Input pin to adjust short circuit detection level |
| 58 | ENA | Enable pin (active high) |
| 59 | IL3 | Input for low side switch 3 (active high) |
| 60 | IH3 | Input for high side switch 3 (active low) |
| 61 | IL1 | Input for low side switch 1 (active high) |
| 62 | IH1 | Input for high side switch 1 (active low) |
| 63 | IL2 | Input for low side switch 2 (active high) |
| 64 | IH2 | Input for high side switch 2 (active low) |
| Cooling Tab | GND | Should be connected to GND |

All GND pins and Cooling Tab should be interconnected.

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Absolute Maximum Ratings [1)]**

-40 °C ≤ Tj ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **Voltages** | | | | | | |
| 4.1.1 | Supply voltage | $V_{S1}$ | -4.0 | 45 | V | with 10Ω and 1µF |
| 4.1.2 | Supply voltage | $V_{S2}$ | -0.3 | 45 | V | – |
| 4.1.3 | Supply voltage | $V_{S3}$ | -0.3 | 47 | V | $t_p$<200ms |
| 4.1.4 | Voltage range at IHx, ILx, ENA, VCT | $V_{DP1}$ | -0.3 | 18 | V | – |
| 4.1.5 | Voltage range at ERRx, VOx, VRI, VRO, SCDL | $V_{DP2}$ | -0.3 | 6.0 | V | – |
| 4.1.6 | Voltage range at ERRx, VRI, SCDL | $V_{DP3}$ | -0.3 | 18 | V | with 10kΩ[2)] |
| 4.1.7 | Voltage range at VOx | $V_{VO}$ | -0.3 | 18.0 | V | with 1kΩ[2)] |
| 4.1.8 | Voltage range at INH | $V_{INH}$ | -0.3 | 18.0 | V | – |
| 4.1.9 | Voltage range at VS_OA | $V_{VS\_OA}$ | -0.3 | 18.0 | V | – |
| 4.1.10 | Voltage range at SLx | $V_{SL}$ | -7 | 7 | V | – |
| 4.1.11 | Voltage range at SHx | $V_{SH}$ | -7 | 45 | V | – |
| 4.1.12 | Voltage range at GLx | $V_{GL}$ | -7 | 18 | V | – |
| 4.1.13 | Voltage range at GHx | $V_{GH}$ | -7 | 55 | V | – |
| 4.1.14 | Voltage difference Gxx-Sxx | $V_{GS}$ | -0.3 | 15 | V | – |
| 4.1.15 | Voltage range at VDH | $V_{VDH1}$ | -0.3 | 55 | V | – |
| 4.1.16 | Voltage range at VDH | $V_{VDH2}$ | -7.0 | 55 | V | $R_{VDH}$=100Ω; 200ms; 10x |
| 4.1.17 | Voltage range at VDH | $V_{VDH3}$ | -9.0 | 55 | V | $R_{VDH}$=100Ω; 1ms; 10x |
| 4.1.18 | Voltage range at VDH | $V_{VDH4}$ | -0.3 | 20 | V | $V_{INH}$=low |
| 4.1.19 | Voltage range at VDH | $V_{VDH5}$ | -0.3 | 28 | V | $V_{INH}$=low; 5min; 3x |
| 4.1.20 | Voltage range at VDH | $V_{VDH6}$ | -0.3 | 35 | V | $V_{INH}$=low; 400ms; 10x |
| 4.1.21 | Voltage range at VDH | $V_{VDH7}$ | -5.0 | 28 | V | $V_{INH}$=low; $R_{VDH}$=100Ω; 25°C; 1min; 10x |
| 4.1.22 | Voltage range at VDH | $V_{VDH8}$ | -7.0 | 28 | V | $V_{INH}$=low; $R_{VDH}$=100Ω; 200ms; 10x |
| 4.1.23 | Voltage range at VDH | $V_{VDH9}$ | -9.0 | 28 | V | $V_{INH}$=low; $R_{VDH}$=100Ω; 1ms; 10x |

**Absolute Maximum Ratings** (cont'd)[1)]

-40 °C ≤ Tj ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| 4.1.24 | Voltage range at CL1 | $V_{CL1}$ | -0.3 | 25 | V | – |
| 4.1.25 | Voltage range at CH1, CB1 | $V_{CH1}$ | -0.3 | 25 | V | – |
| 4.1.26 | Voltage difference CH1-CL1 | $V_{CP1}$ | -0.3 | 25 | V | – |
| 4.1.27 | Voltage range at CL2 | $V_{CL2}$ | -0.3 | 25 | V | – |
| 4.1.28 | Voltage range at CH2, CB2 | $V_{CH2}$ | -0.3 | 55 | V | – |
| 4.1.29 | Voltage range at CB2 | $V_{CB2}$ | -0.3 | 60 | V | $t_P$<1µs; $f$=50kHz |
| 4.1.30 | Voltage difference CH2-CL2 | $V_{CP2}$ | -0.3 | 25 | V | – |
| 4.1.31 | DC voltage difference between VDH and VS[3)] | $V_{VDHVS}$ | -2 | +2 | V | – |
| 4.1.32 | Voltage range at ISPx, ISNx | $V_{ISI}$ | -5 | 5 | V | – |
| 4.1.33 | Output current range at VOx | $I_{VOx}$ | -10 | 10 | mA | – |
| **External components** | | | | | | |
| 4.1.34 | Gate resistor | $R_G$ | 2 | – | Ω | – |
| 4.1.35 | Min. Voltage rating of CB2 capacitor | $V_{CCB2a}$ | -20 | 20 | V | – |
| 4.1.36 | Min. Voltage rating of CB2 capacitor | $V_{CCB2b}$ | -31 | +31 | V | $V_S$ > 20V; $V_{INH}$=low |
| **Temperatures** | | | | | | |
| 4.1.37 | Junction temperature | $T_J$ | -40 | 150 | °C | – |
| 4.1.38 | Storage temperature | $T_{stg}$ | -55 | 150 | °C | – |
| 4.1.39 | Lead soldering temperature (1/16'' from body) | $T_{sol}$ | – | 260 | °C | – |
| 4.1.40 | Peak reflow soldering temperature[4)] | $T_{ref}$ | – | 260 | °C | – |
| **Thermal Resistance** | | | | | | |
| 4.1.41 | Junction to case | $R_{thJC}$ | – | 5 | K/W | – |
| **ESD Susceptibility** | | | | | | |
| 4.1.42 | ESD Resistivity[5)] | $V_{ESD}$ | -2 | 2 | kV | |
| 4.1.43 | ESD Resistivity (charge device model)[6)] | $V_{ESD}$ | – | 750 | V | |

1) Not subject to production test, specified by design.
2) after 50h the chip must be replaced; resistor in series
3) High frequent transient ringing above 1MHz exceeding the +/-2V is allowed
4) Reflow profile IPC/JEDEC J-STD-020C
5) ESD susceptibility HBM according to EIA/JESD 22-A 114B
6) ESD susceptibility CDM according to EIA/JESD 22-C 101

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| 4.2.1 | Supply voltage[1)] | $V_{S1}$ | 5.5 | 20 | V | DC |
| 4.2.2 | Supply voltage[1)] | $V_{S2}$ | 5.5 | 28 | | $T_A$=25°C; $t$<1min |
| 4.2.3 | Duty cycle[2)] | $D$ | 0 | 100 | % | – |
| 4.2.4 | PWM frequency | $f_{PWM}$ | 0 | 25 | kHz | Total gate charge 400nC |
| 4.2.5 | Quiescent current[3)] | $I_Q$ | – | 30 | µA | $V_S$ ,$V_{VDH}$<20 V |
| 4.2.6 | Quiescent current into VDH | $I_{Q\_VDH}$ | – | 30 | µA | $V_{VDH}$<20V; $V_S$ pin open |
| 4.2.7 | Supply current at Vs | $I_{Vs}$ | <br>–<br>– | <br>110<br>110<br>90<br>90 | mA | $f_{PWM}$=20kHz $Q_{gate}$=170nC:<br>$V_S$ = 5.5V<br>$V_S$ = 14V<br>$V_S$= 18V<br>$V_S$ = 20V |
| 4.2.8 | Supply current at Vs (device disabled by ENA) | $I_{Vs(o)}$ | – | 60<br>40 | mA | $V_S$=5.5V... 20V; $V_{SHx}$=0V<br>$V_S$=20V... 28V; $V_{SHx}$=0V |
| 4.2.9 | Supply current at VS_OA | $I_{Vs\_OA}$ | – | 30 | mA | $V_{VS\_OA}$=4.8 ... 5.2V |
| 4.2.10 | Current flowing into VDH pin (device not in sleep mode) | $I_{VDH1}$ | – | 1.5 | mA | $V_S$=5.5V... 20V; $V_{SHx}$=0V |
| 4.2.11 | Current flowing into VDH pin (device not in sleep mode) | $I_{VDH2}$ | 150 | 650 | µA | $V_S$=5.5V... 20V; $V_S$=$V_{VDH}$=$V_{SHx}$; $V_{IHx}$=low |
| 4.2.12 | Voltage difference CB2-VDH | $V_{CB2VDH}$ | -0.3 | 20 | V | Operation mode |
| 4.2.13 | Junction temperature | $T_J$ | -40 | 150 | °C | |

1) For proper start up minimum Vs=6.5V is required

2) Duty cycle is referred to the high side input command (IHx); The duty cycles can be driven continuously and fully operational

3) total current consumption from power net (Vs and VDH)

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

*Note: If the voltage difference between CB2 and SHx is smaller than 2V during normal operation, there is a risk that the high side output can switch on and off without a corresponding input signal. As soon as this supply voltage recovers and the input signal changes, the output stage is automatically aligned to the input again.*

## 4.3 Default State of Inputs

**Table 1 Default State of Inputs**

| Characteristic | State | Remark |
|---|---|---|
| Default state of ILx (if ILx left open -pull down) | Low | Low side MOSFETs off |
| Default state of IHx (if IHx left open - pull up) | High | High side MOSFETs off |
| Default state of ENA (if ENA left open - pull down) | Low | Device/outputs disabled |
| Default state of VCT (if VCT left open - pull up) | High | Device/outputs disabled |
| Default state of INH (if INH left open - pull down) | Low | Sleep mode, $I_Q$ < 30 µA |
| Default state of SCDL (if SCDL left open - internal voltage divider) | Typ. 1.4V | – |
| Default State of sense amplifier output $V_{OX}$ (ISPx=ISNx=0V) | Zero ampere equivalent | – |
| Status of the Device and the Outputs when ENA=INH=high & VCT=low[1)] | Device active and outputs functional | 5.5....28V; No VCC check failure |

1) No special start up procedure is required

*Note: The load condition "C=22nF; $R_{Load}$=1Ω" in the paragraph "Electrical characteristics / Dynamic characteristic" means that $R_{Load}$ is connected between the output Gxx and the positive terminal of the C. The negative terminal of the C is connected to GND and the corresponding Sxx. The voltage is measured at the positive terminal of the C.*

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

# 5 Description and Electrical Characteristics

## 5.1 MOSFET Driver

### 5.1.1 Output Stages

The 3 low side and 3 high side powerful push-pull output stages of the TLE7189QK are all floating blocks, each with its own source pin. This allows the direct connection of the output stage to the source of each single MOSFET, allowing a perfect control of each gate-source voltage even when 200A are driven in the bridge with rise and fall times clearly below 1µs.

All 6 output stages have the same output power and thanks to the used charge pump principle they can be switched all up to 30kHz.

Its output stages are powerful enough to drive MOSFETs with 400nC gate charge with approx. 150ns fall and rise times or even to run 12 MOSFETs with 200nC each with fall and rise times of approx. 150ns.

Maximum allowed power dissipation, max. junction temperature and the capabilities of the charge pump limit the use for higher frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 5.2.1**.

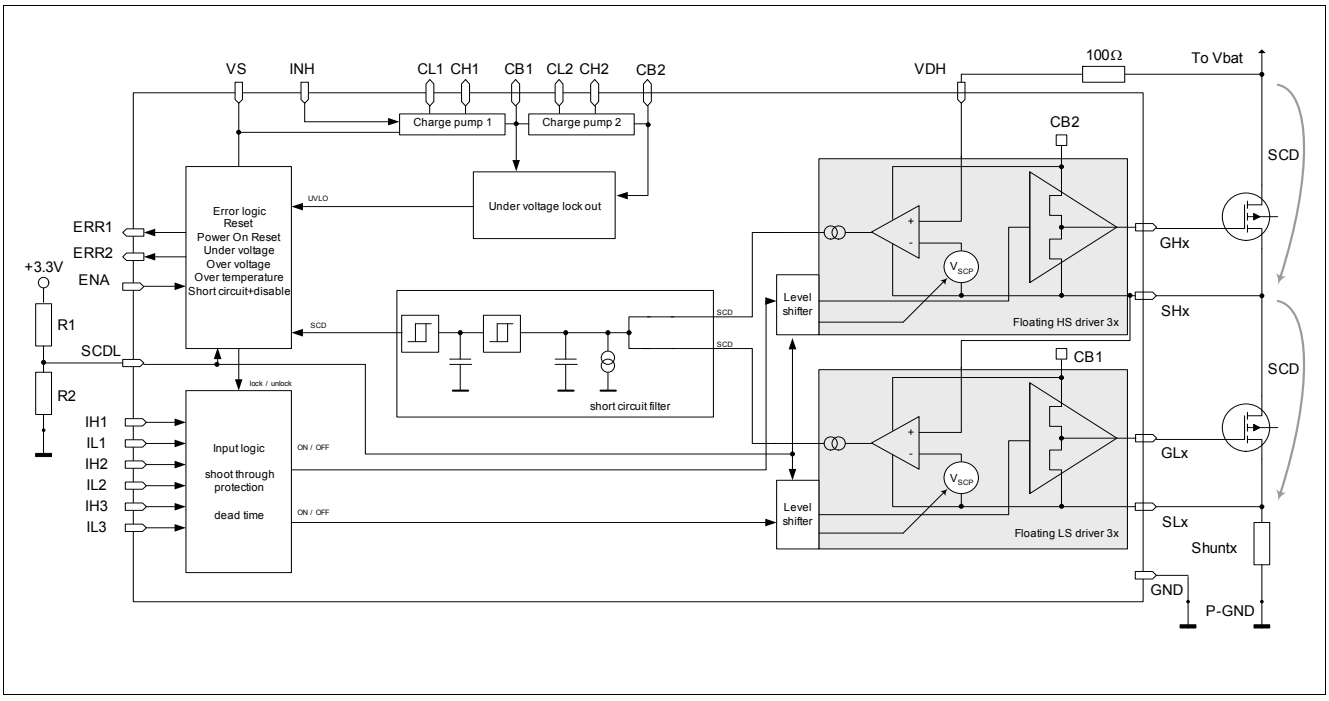



**Figure 3 Block Diagram of Driver Stages including Short Circuit Detection**

### 5.1.2 Operation at Vs<12V - Integrated Charge Pumps

The TLE7189QK provides a feature tailored to the requirements in 12V automotive applications. Often the operation of an application has to be assured even at 9V supply voltage or lower. Normally bridge driver ICs provide in such conditions clearly less than 9V to the gate of the external MOSFETs, increasing their $R_{DSon}$ and the associated power dissipation.

The TLE7189QK has two charge pump circuitries for external capacitors.

The operation of the charge pumps is independent upon the pulse pattern of the MOSFETs.

The output of the charge pumps are regulated. The first charge pump doubles the supply voltage as long as it is below 8V. At 8V supply voltage and above, charge pump 1 regulates its output to 15V typically. Above 15V supply voltage, the output voltage of charge pump 1 will increase linearly. Yet, the output will not exceed 25V.

Charge pump 2 is regulated as well but it is pumped to the voltage on Vs. Normally VDH and Vs are in the same voltage range. The driver is not designed to have significant different voltages at VDH compared to Vs. This would lead to reduced supply voltages for the high side output stages.

Charge pump 1 supplies the low side MOSFETS and output stages for the low side MOSFETs with sufficient voltage to assure 10V at the MOSFETs´ gate even if the supply voltage is below 10V. Charge pump 2 supplies the output stages for the high side MOSFETs with sufficient voltage to assure 10V at the MOSFETs´ gate. In addition, the charge pump 1 supplies most of the internal circuits of the driver IC, including charge pump 2. Output of charge pump 1 is the buffer capacitor CB1 which is referenced to GND.

Charge pump 2 supplies the high side MOSFETs and the output stages for the high side MOSFETs with sufficient voltage to assure 10V at the high side MOSFET gate. Output of charge pump 2 is buffer capacitor CB2 which is referenced to VDH.

This concept allows to drive all external MOSFETs in the complete duty cycle range of 0 to 100% without taking care about recharging of any bootstrap capacitors.

This simplifies the use in all applications especially in motor drives with block wise commutation.

The charge pumps are only deactivated when the device is put into sleep mode via INH.

The size of the charge pump capacitors (pump capacitors CPx as well as buffer capacitors CBx) can be varied between 1µF and 4.7µF. Yet, larger capacitor values result in higher charge pump voltages and less voltage ripple on the charge pump buffer capacitors CBx (which supply the internal circuits as well as the external MOSFETs, pls. see above). Besides the capacitance values the ESR of the buffer capacitors CBx determines the voltage ripple as well. It is recommended to use buffer capacitors CBx that have small ESR.

Pls. see also **Chapter 5.1.3** for capacitor selection.

### 5.1.3 Sleep Mode

When the INH pin is set to low, the driver will be set to sleep mode. The INH pin switches off the complete supply structure of the device and leads finally to an under voltage shut down of the complete driver. Enabling the device with the INH pin means to switch on the supply structure. The device will run through power on reset during wake up. It is recommended to perform a Reset by ENA after Wake up to remove possible ERR signals; Reset is performed by keeping ENA pin low until the charge pump voltages have ramped up.

Enabling and disabling with the INH pin is not very fast. For fast enable / disable the ENA pin is recommended.

When the TLE7189QK is in INH mode (INH is low) or when the supply voltage is not available on the Vs pin, then the driver IC is not supplied, the charge pumps are inactive and the charge pump capacitors are discharged. Pin CB2 (+ terminal of buffer capacitor 2) will decay to GND. When the battery voltage is still applied to VDH (- terminal of buffer capacitor 2) the buffer capacitor 2 will slowly charged to battery voltage, yet with reversed polarity compared to the polarity during regular operation. Hence, it is important to use a buffer capacitor 2 (CB2) that can withstand both, +25 V during operation mode and $-V_{BAT}$ during INH mode, e.g. a ceramic capacitor. In case of load dump during INH mode, the negative voltage across CB2 will be clamped to -31 V (CB2 referenced to VDH).

## 5.1.4 Electrical Characteristics

### Electrical Characteristics MOSFET drivers - DC Characteristics

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.1.1 | Low level output voltage | $V_{G\_LL}$ | – | – | 0.2 | V | $I_{Load}$=30mA |
| 5.1.2 | High level output voltage | $V_{G\_HL1}$ | 9 | – | 13 | V | $V_S$=8... 20V; $I_{Load}$=-2mA |
| 5.1.3 | High level output voltage, Low Side | $V_{G\_HL2}$ | 7.5 | – | 13 | V | $V_S$=5.5... 8V; $I_{Load}$=-2mA |
| 5.1.4 | High level output voltage, High Side | $V_{G\_HL3}$ | 6.5 | – | 13 | V | $V_S$=5.5... 8V; $I_{Load}$=-2mA |
| 5.1.5 | High level output voltage difference | $dV_{G\_H}$ | – | – | 1.0 | V | $I_{Load}$=-100mA; $V_S$=20V |
| 5.1.6 | Gate drive output voltage | $V_{GS\_D}$ | – | – | 0.2 | V | $V_{ENA}$=low or $V_{VCT}$=high; 5.5V<$V_S$<28V $I_{Load}$=10mA |
| 5.1.7 | Gate drive output voltage<br>Tj=-40°C<br>Tj=25°C<br>Tj=150°C | $V_{GS1}$ | – | – | <br>1.4<br>1.2<br>1.0 | V | UVLO; $V_S$<=5.5V; $I_{Load}$=2mA |
| 5.1.8 | Gate drive output voltage high side<br>Tj=-40°C<br>Tj=25°C<br>Tj=150°C | $V_{GS2}$ | – | – | <br>1.4<br>1.2<br>1.0 | V | Over voltage or $V_S$=open or $V_{INH}$=low; $I_{Load}$=2mA |
| 5.1.9 | Gate drive output voltage low side | $V_{GS3}$ | – | – | 0.2 | V | Over voltage; $I_{Load}$=2mA |
| 5.1.10 | Gate drive output voltage low side[1)] | $V_{GS3}$ | – | 1.7 | – | V | SLx open; $V_S$=open; $V_{INH}$=low; $I_{GLx}$=10µA |
| 5.1.11 | Gate drive output voltage low side[1)] | $V_{GS3}$ | – | 1.1 | – | V | SLx open; $V_S$=open; $V_{INH}$=low; $I_{GLx}$=3µA |
| 5.1.12 | Low level input voltage of Ixx, ENA | $V_{I\_LL}$ | – | – | 1.0 | V | – |
| 5.1.13 | High level input voltage of Ixx, ENA | $V_{I\_HL}$ | 2.0 | – | – | V | – |
| 5.1.14 | Input hysteresis of IHx, ILx, ENA | $dV_{I1}$ | 50 | – | –- | mV | $V_S$=5.5... 8V |
| 5.1.15 | Input hysteresis of IHx, ILx, ENA | $dV_{I2}$ | 100 | 200 | –- | mV | $V_S$=8... 20V |
| 5.1.16 | Low level input voltage of INH | $V_{I\_LL}$ | – | – | 0.75 | V | – |
| 5.1.17 | High level input voltage of INH | $V_{I\_HL}$ | 2.1 | – | – | V | – |
| 5.1.18 | IHx pull up resistor | $R_{IHx}$ | 18 | 30 | 42 | kΩ | $V_{IHx}$<5.5V |
| 5.1.19 | ILx pull down resistor | $R_{ILx}$ | 18 | 30 | 42 | kΩ | $V_{ILx}$<5.5V |
| 5.1.20 | INH, ENA pull down resistor | $R_{INEN}$ | 27 | 45 | 70 | kΩ | $V_{INH}$; $V_{ENA}$<5.5V |
| 5.1.21 | Quiescent current VDH | $I_{QVDH}$ | – | 5 | – | µA | 25°C; $V_{INH}$=low |

### Electrical Characteristics MOSFET drivers - DC Characteristics

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.1.22 | Output bias current SHx | $I_{SHx}$ | -1.6 | -1.0 | -0.3 | mA | $V_S$=5.5...20V; $V_{SHx}$=0...($V_S$+1) |
| 5.1.23 | Output bias current SLx | $I_{SLx}$ | -1.6 | -1.0 | -0.3 | mA | $V_S$=5.5...20V; $V_{SLx}$=0...7V |

### Electrical Characteristics MOSFET drivers - Dynamic Characteristics

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.1.24 | Fixed internal dead time | $t_{DT}$ | 220 | 400 | 600 | ns | – |
| 5.1.25 | Turn on current, peak | $I_{G(on)1}$ | – | 1.5 | – | A | $V_{Gxx}$-$V_{Sxx}$=0V; $V_S$=8...20V; $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.26 | Turn on current, peak | $I_{G(on)2}$ | – | 0.8 | – | A | $V_{Gxx}$-$V_{Sxx}$=0V; $V_S$=5.5...8V; $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.27 | Turn off current, peak | $I_{G(off)}$ | – | 1.5 | – | A | $V_{Gxx}$-$V_{Sxx}$=10V; $V_S$=8...20V; $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.28 | Rise time (20-80%)<br>$T_j$ = -40°C<br>$T_j$ = 25°C<br>$T_j$ = 150°C | $t_{G\_rise}$ | – | <br>150 | <br>400<br>400<br>700 | ns | $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.29 | Fall time (20-80%)<br>$T_j$ = -40°C<br>$T_j$ = 25°C<br>$T_j$ = 150°C | $t_{G\_fall}$ | – | <br>150 | <br>230<br>230<br>500 | ns | $C_{Load}$=22nF; $R_{Load}$=1Ω; |
| 5.1.30 | Input propagation time (low on) | $t_{P(ILN)}$ | 90 | 190 | 290 | ns | $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.31 | Input propagation time (low off) | $t_{P(ILF)}$ | 0 | 100 | 200 | ns | |
| 5.1.32 | Input propagation time (high on) | $t_{P(IHN)}$ | 90 | 190 | 290 | ns | |
| 5.1.33 | Input propagation time (high off) | $t_{P(IHF)}$ | 0 | 100 | 200 | ns | |
| 5.1.34 | Absolute input propagation time difference (all channels turn on) | $t_{P(an)}$ | – | – | 70 | ns | |
| 5.1.35 | Absolute input propagation time difference (all channels turn off) | $t_{P(af)}$ | – | – | 70 | ns | |

### Electrical Characteristics MOSFET drivers - Dynamic Characteristics

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.1.36 | Absolute input propagation time difference (1channel high off - low on) | $t_{P(1hfln)}$ | 40 | – | 180 | ns | $C_{Load}$=22nF; $R_{Load}$=1Ω |
| 5.1.37 | Absolute input propagation time difference (1channel low off - high on) | $t_{P(1lfhn)}$ | 40 | – | 180 | ns | |
| 5.1.38 | Absolute input propagation time difference (all channel high off - low on) | $t_{P(ahfln)}$ | 40 | – | 180 | ns | |
| 5.1.39 | Absolute input propagation time difference (all channel low off - high on) | $t_{P(alfhn)}$ | 40 | – | 180 | ns | |
| 5.1.40 | Wake up time; INH low to high | $t_{INH\_Pen1}$ | – | – | 20 | ms | Driver fully functional; $V_S$=6.5...8V; $V_{ENA}$=low; $C_{CPx}$=$C_{CBx}$=4.7µF |
| 5.1.41 | Wake up time; INH low to high | $t_{INH\_Pen2}$ | – | – | 10 | ms | Driver fully functional; $V_S$=8...20V; $V_{ENA}$=low; $C_{CPx}$=$C_{CBx}$=4,7µF |
| 5.1.42 | Wake up time logic functions; INH low to high | $t_{INH\_log}$ | – | – | 10 | ms | Driver fully functional; $V_S$=6.5...8V; $V_{ENA}$=low; $C_{CPx}$=$C_{CBx}$=4,7µF |
| 5.1.43 | Wake up time logic functions; INH low to high | $t_{INH\_log}$ | – | – | 5 | ms | Driver fully functional; $V_S$=8...20V; $V_{ENA}$=low; $C_{CPx}$=$C_{CBx}$=4,7µF |
| 5.1.44 | INH propagation time to disable the output stages | $t_{INH\_Pdi1}$ | – | – | 10 | µs | $V_S$=5.5...8V |
| 5.1.45 | INH propagation time to disable the output stages | $t_{INH\_Pdi2}$ | – | – | 8 | µs | $V_S$=8...20V |
| 5.1.46 | INH propagation time to disable the entire driver IC | $t_{INH\_Pdi3}$ | – | – | 300 | µs | – |
| 5.1.47 | Supply voltage $V_s$ for Wake up | $V_{VsWU}$ | 6.5 | – | – | V | diagnostic, OpAmp working |
| 5.1.48 | Charge pump frequency | $f_{CP}$ | 38 | 55 | 72 | kHz | – |

## 5.2 Protection and Diagnostic Functions

### 5.2.1 Short Circuit Protection

The TLE7189QK provides a short circuit protection for the external MOSFETs. It is a monitoring of the drain-source voltage of the external MOSFETs. As soon as this voltage is higher than the short circuit detection limit, a capacitor will be charged. The high side and the low side output stage of the same half bridge use the same capacitor (see **Figure 3** ). This capacitor is discharged permanently with a current which is about 2 times smaller than the charging current. This charging and discharging ratio is specified with the help of duty cycle where a short is detected or not detected.

After a delay of about 12µs all external MOSFETs will be switched off until the driver is reset by the ENA pin. The error flag is set.

The drain-source voltage monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding input is set to "on" and the dead time is expired.

The short circuit detection level is adjustable in an analogue manner by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1V drain-source voltage, the SCDL pin must be set to 1V as well. The drain-source voltage limit can be chosen between 0.7 ... 2.5V.

If the SCDL pin is left open, the short circuit detection level will be set internally to a specified value. In case SCDL is connected to GND the detection level is low. If SCDL is connected to 3.3V, the detection level is about 3.2V.

In the TLE7189QK the short circuit detection functionality can be tested by setting the SCDL pin to voltages lower than 0.4V, switching off the low side MOSFETs and switching on one or more high side MOSFETs. In this test, a short circuit will be detected even without current in the external MOSFET (VDH-SHx > $V_{TSCD1}$).

This test function can be used as well to detect an open VDH pin. If VDH is open during this test, no SCD error will be reported.

A setting of 5V at the SCDL pin will disable the short circuit protection function.

### 5.2.2 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs are not "on" at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7189QK is fixed to a minimum value. This function assures a minimum dead time if the input signals coming from the µC are faulty.

The exact dead time of the bridge is usually controlled by the PWM generation unit of the µC.

In addition to this dead time, the TLE7189QK provides a locking mechanism, avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection.

If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored. The conflicting input signals will not generate an error message.

### 5.2.3 Under Voltage Shut Down

The TLE7189QK has an integrated under voltage shut down, to assure that the behavior of the device is predictable in all voltage ranges.

If the voltage of a charge pump buffer capacitors CBx reaches the under voltage shut down level for a minimum specified filter time, the gate-source voltage of all external MOSFETs will be actively pulled to low. In this situation the short circuit detection of this output stage is deactivated to avoid a latching shut down of the driver.

As soon as the charge pump buffer voltage recovers, the output stage condition will be aligned to the input patterns automatically.This allows to continue operation of the motor in case of under voltage shut down without a reset by the µC.

Under voltage shut down will not occur when $V_S$ > 6V, $Q_G$ < 250nC, $f_{PWM}$ < 25kHz, and the charge pump capacitors Cxx = 4.7 µF.

### 5.2.4 Over Voltage Shut Down

The TLE7189QK has an integrated over voltage shut down to avoid destruction of the IC at high supply voltages. The voltage is measured at the Vs and the VDH pin. When one of them or all of them exceed the over voltage shut down level for more than the specified filter time then the external MOSFETs are switched off. In addition, over voltage will shut down the charge pumps and will discharge the charge pump capacitors. This results in an under voltage condition which will be indicated on the ERRx pins. During over voltage shut down the external MOSFETs and the charge pumps remain off until a reset is performed.

### 5.2.5 Over Temperature Warning

If the junction temperature is exceeding typ. 155°C an error signal is given as warning. The driver IC will continue to operate in order not to disturb the application.

The warning is removed automatically when the junction temperature is cooling down.

It is in the responsibility of the user to protect the device against over temperature destruction.

### 5.2.6 VCC Check

To assure a high level of system safety, the TLE7189QK provides an VCC check.

The 5.0V system supply connected to the VS_OA pin is checked by an internally monitoring for over- and under voltage. An internal filter time is integrated to avoid faulty triggering.

The VCC check is active when the signal on the ENA pin is high and inactive when ENA signal is low (=driver IC disabled).

In case of under- or over voltage at VS_OA, the VCC check will disable the driver IC and is latched. To restart the output stages, a reset has to be performed with the ENA pin.

The VCT pin decides about the over voltage and under voltage detection level.

### 5.2.7 ERR Pins

The TLE7189QK has two status pins to provide diagnostic feedback to the µC. The outputs of these pins are 5V push pull stages, they are either High or Low.

**Table 2 Overview of error conditions**

| INH | ENA | ERR1 | ERR2 | Driver conditions |
|---|---|---|---|---|
| High | High | Low | Low | Under voltage or VCC check error |
| High | High | Low | High | Over temperature or over voltage |
| High | High | High | Low | Short circuit detection |
| High | High | High | High | No errors observed |
| High | Low | High | High | No errors will be reported (except OT warning & undervoltage shutdown) |
| Low | X | Low | Low | ERR output tristate - low secured by pull down |

**Table 3 Behavior at different error conditions**

| Error condition | restart behavior | Shuts down... |
|---|---|---|
| Short circuit detection | Latch, reset must be performed at ENA pin | All external Power -MOSFETs |
| Under voltage | Auto restart | All external Power -MOSFETs |
| Over voltage | Latch, reset must be performed at ENA pin | All external Power -MOSFETs |

| Error condition | restart behavior | Shuts down... |
|---|---|---|
| Over temperature warning | Self clearing | Nothing |
| VCC check | Latch, reset must be performed at ENA pin | All external Power -MOSFETs |

*Note: All errors do NOT lead to sleep mode. Sleep mode is only initiated with the INH pin. The latch and restart behavior allows to distinguish between the different error types combined at the ERR signals.*

**Table 4 Priorisation of Errors**

| Priority | Error |
|---|---|
| 1 | VCC check |
| 2 | Short circuit detection |
| 3 | Under voltage detection |
| 4 | Over voltage detection |
| 5 | Over temperature |

**Reset of ERROR registers and Disable**

The TLE7189QK can be reseted with the help of the enable pin ENA. If the ENA pin is pulled to low for a specified minimum time, the error registers are cleared and the external MOSFETs are switched off actively.

During disable only the errors under voltage shut down and over temperature warning are shown. Other errors are not displayed.

## 5.2.8 Electrical Characteristics

**Electrical Characteristics - Protection and diagnostic functions**

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Over temperature** | | | | | | | |
| 5.2.1 | Over temperature warning | $T_{j(OW)}$ | 135 | 155 | 175 | °C | – |
| 5.2.2 | Hysteresis for over temperature warning | $dT_{j(OW)}$ | – | 20 | – | °C | – |
| **Short circuit detection** | | | | | | | |
| 5.2.3 | Filter time of short circuit protection | $t_{SCP(off)}$ | 8 | 12 | 16 | µs | Default |
| 5.2.4 | Maximum duty cycle for no SCD[1)] | $D_{SCDmax}$ | – | – | 30 | % | $f_{PWM}$=100kHz at IHx or ILx and at static applied SC |
| 5.2.5 | minimum duty cycle for periodic SCD[1)] | $D_{SCDmin}$ | 70 | – | – | % | $f_{PWM}$=100 kHz at IHx or ILx and at static applied SC |
| 5.2.6 | Voltage range on VSCD pin to adjust the Vds limit | $V_{SCDLa1}$ | 0.7 | – | 2.5 | V | Short circuit detection is active |
| 5.2.7 | Short circuit detection level | $V_{SCDLa2}$ | 2.64 | – | 3.63 | V | Short circuit detection is active $V_{SCDL}$=3.3V |

**Electrical Characteristics - Protection and diagnostic functions** (cont'd)

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.2.8 | Short circuit disable voltage at VSCD pin | $V_{SCDL(dis)}$ | 4.5 | – | 5.5 | V | Short circuit detection is disabled |
| 5.2.9 | Accuracy of SCD ($V_{SCDL}$ /$V_{DS(off)}$) | $A_{SC(off)1}$ | 0.85 | – | 1.15 | – | $V_{SCDL(off)}$ set to 1... 2.5V |
| 5.2.10 | Accuracy of SCD ($V_{SCDL}$ /$V_{DS(off)}$) | $A_{SC(off)2}$ | 0.7 | – | 1.3 | – | $V_{SCDL(off)}$ set to 0.7... 1V |
| 5.2.11 | SCDL pull up resistor | $R_{SCDU}$ | – | 400 | – | kΩ | Not tested |
| 5.2.12 | SCDL pull down resistor | $R_{SCDD}$ | – | 160 | – | kΩ | Not tested |
| 5.2.13 | SCDL default voltage | $V_{SCDLop}$ | – | 1.4 | – | V | Open pin |
| **Test of short circuit detection** | | | | | | | |
| 5.2.14 | SCDL voltage for SCD test activation | $V_{SCDT}$ | – | – | 0.4 | V | – |
| 5.2.15 | Filter time for SCD test activation | $t_{SCDT}$ | 0.5 | 2.5 | – | µs | – |
| 5.2.16 | VDH-SHx voltage for SCD detection in SCD test mode | $V_{TSCD1}$ | -80 | – | – | mV | |
| 5.2.17 | VDH-SHx voltage with no SCD detection in SCD test mode | $V_{TSCD2}$ | – | – | -350 | mV | |
| **ERR pins** | | | | | | | |
| 5.2.18 | High level output voltage of ERRx | $V_{OHERR}$ | 4.0 | – | 5.2 | V | $I_{Load}$= -0.2mA |
| 5.2.19 | Low level output voltage of ERRx | $V_{OLERR}$ | -0.1 | – | 0.4 | V | $I_{Load}$= 0.2mA |
| 5.2.20 | ERR pull down resistor | $R_{ERR}$ | 2.7 | – | 112 | kΩ | $V_{ERR}$<5.5V; $V_{INH}$=low |
| 5.2.21 | Propagation time difference ERR1 and ERR2 | $t_{PD(ERR)}$ | – | – | 200 | ns | – |
| **Over- and under voltage** | | | | | | | |
| 5.2.22 | Over voltage shut down | $V_{OV(off)}$ | 28 | – | 33 | V | – |
| 5.2.23 | Over voltage shut down at VDH | $V_{OV(off)}$ | 28 | – | 32.7 | V | – |
| 5.2.24 | Over voltage filter time | $t_{OV}$ | 30 | – | 60 | µs | – |
| 5.2.25 | Under voltage shut down CB1 | $V_{UV1}$ | 7.4 | 8.2 | 9.0 | V | CB1 to GND |
| 5.2.26 | Under voltage shut down CB2 | $V_{UV2}$ | 4.6 | – | 6.8 | V | CB2 to VDH |
| 5.2.27 | Hysteresis of under voltage shut down on CB1 and CB2 | $V_{HUV1,2}$ | – | 1.0 | – | V | – |
| 5.2.28 | Under voltage filter time on CB1 and CB2 | $t_{UV}$ | 3.5 | 5 | 7 | µs | – |
| **Enable and reset** | | | | | | | |
| 5.2.29 | Reset time to clear ERR registers | $t_{Res1}$ | 3.0 | – | – | µs | – |
| 5.2.30 | Low time of ENA signal without reset | $t_{Res0}$ | – | – | 1.0 | µs | – |

**Electrical Characteristics - Protection and diagnostic functions** (cont'd)

$V_S$ = 5.5 to 20V, $T_j$ = -40 to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.2.31 | ENA propagation time (for enable / disable) | $t_{PENA}$ | – | – | 4.0 | µs | – |
| 5.2.32 | Return time to normal operation at auto-restart | $t_{AR}$ | – | – | 1.0 | µs | – |
| **VCC Check** | | | | | | | |
| 5.2.33 | Under voltage detection level | $V_{VCU}$ | 4.3 | – | 4.7 | V | $V_{VCT}$=low |
| 5.2.34 | Over voltage detection level | $V_{VCOl}$ | 5.3 | – | 5.8 | V | $V_{VCT}$=low |
| 5.2.35 | Over voltage detection level | $V_{VCOh}$ | 3.3 | – | 4.3 | V | $V_{VCT}$=high |
| 5.2.36 | Over- and under voltage filter time | $t_{VC}$ | 10 | – | 25 | µs | – |
| 5.2.37 | Low level input voltage of VCT | $V_{VCT\_LL}$ | – | – | 1.0 | V | – |
| 5.2.38 | High level input voltage of VCT | $V_{VCT\_HL}$ | 2.0 | – | – | V | – |
| 5.2.39 | VCT pull up resistor | $R_{VCT}$ | 27 | 45 | 70 | kΩ | $V_{VCT}$<5.5V |
| 5.2.40 | Filter time for VCT test | $t_{VCT}$ | 1.3 | 2 | 3.0 | µs | – |

1) Parameters describe the behavior of the internal SCD circuit. Therefore only internal delay times are considered. In application dead-/ delay times determined by application circuit (switching times of MOSFETs, adjusted dead time) have to be considered as well.

## 5.3 Shunt Signal Conditioning

The TLE7189QK incorporates three fast and precise operational amplifiers for conditioning and amplification of the shunt signals sensed in the three phases. Additionally, one reference bias buffer is integrated to provide an adjustable bias reference for the three OpAmps. The voltage divider on the VRI pin should be less than 50 kΩ, the filtering capacitor less than 1.2 µF - if needed at all. The gain of the OpAmps is adjustable by external resistors within a range of 5 to 15.

When $V_{ISP}$ = $V_{ISN}$, VO provides the reference voltage $V_{VRO}$. $V_{VRO}$ is normally half of the regulated voltage provided from an external voltage regulator for the ADC used to read the current sense signal. The additional buffer allows bi-directional current sensing and permits the adaptation of the reference bias to different µC I/O voltages. The reference buffer assures a stable reference voltage even in the high frequency range.

The reference bias buffer is used for all of the OpAmps. The OpAmps of the TLE7189QK demonstrate low offset voltages and very little drift over temperature, thus allowing accurate phase current measurements.

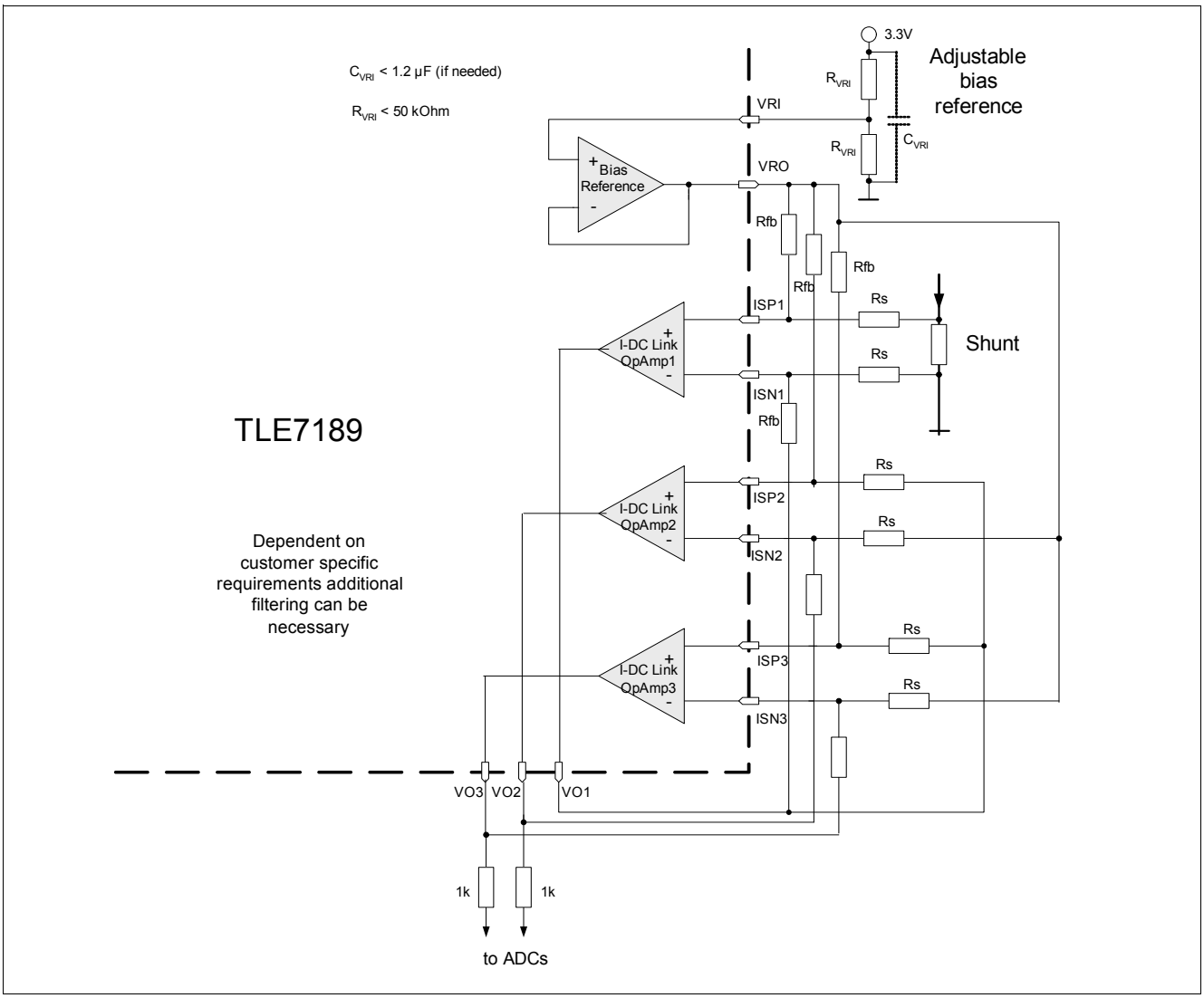



**Figure 4 Shunt Signal Conditioning Block Diagram**

### 5.3.1 Electrical Characteristics

**Electrical Characteristics - Current sense signal conditioning**

$V_S$ = 5.5 to 20V, $V_{VSOA}$ = 5V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.3.1 | Series resistors | $R_{RS}$ | 100 | 500 | 1000 | Ω | – |
| 5.3.2 | Resistor ratio (gain ratio) | $R_{Rfb}/R_{RS1}$ | 5 | – | 20 | – | – |
| 5.3.3 | Resistor ratio (gain ratio) | $R_{Rfb}/R_{RS2}$ | 3 | – | 20 | – | 1kΩ and 200pF at VOx |
| 5.3.4 | Input differential voltage (ISPx - ISNx) | $V_{IDR}$ | -800 | – | 800 | mV | – |
| 5.3.5 | Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND) | $V_{LL1}$ | -800 | – | 2200 | mV | $V_S$=8 ... 20V |
| 5.3.6 | Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND) | $V_{LL2}$ | -800 | – | 1500 | mV | |
| 5.3.7 | Input offset voltage of the I-DC link OpAmp, including drift over temperature range | $V_{IO1}$ | -1.58 | – | 1.28 | mV | $R_{RS}$=500Ω; $V_{CM}$=0V; $V_O$=1.65V; $V_{RI}$=1.65V |
| 5.3.8 | Input offset voltage of reference buffer | $V_{IO2}$ | -3 | – | 2 | mV | – |
| 5.3.9 | VRI input range | $V_{RI}$ | 1.2 | – | 2.6 | V | – |
| 5.3.10 | Input bias current | $I_{IB}$ | -300 | – | -70 | µA | $V_{CM}$=0V; $V_O$=open |
| 5.3.11 | Input bias current of reference buffer | $I_{IBRB}$ | 0.6 | 1.4 | 2.4 | µA | $V_{RI}$=1.65V |
| 5.3.12 | High level output voltage of VOx | $V_{OH}$ | 4.0 | – | 4.5 | V | $V_{RI}$=1.2 ... 2.6V; $I_{OH}$=-3mA; |
| 5.3.13 | Low level output voltage of VOx | $V_{OL}$ | -0.1 | – | 0.2 | V | $V_{RI}$=1.2 ... 2.6V; $I_{OH}$=3mA |
| 5.3.14 | Output voltage of VOx | $V_{OR}$ | 1.623 | 1.65 | 1.668 | V | $V_{IN(SS)}$=0V; Gain=15; $V_{RI}$=1.65V |
| 5.3.15 | Output short circuit current | $I_{SC}$ | 5 | – | – | mA | – |
| 5.3.16 | Differential input resistance[1)] | $R_{RI}$ | 100 | – | – | kΩ | – |
| 5.3.17 | Common mode input capacitance[1)] | $I_{SC}$ | – | – | 10 | pF | 10kHz |
| 5.3.18 | Common mode rejection ratio at DC<br>CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM)) | $CMRR$ | 80 | – | – | db | – |
| 5.3.19 | Common mode suppression[2)] with CMS = 20*Log(Vout_CM/Vin_CM)<br>Freq =100kHz<br>Freq = 1MHz<br>Freq = 10MHz | $CMS$ | – | <br>62<br>43<br>33 | – | db | $V_{IN}$=360mV* sin(2*π*freq*t); $R_{RS}$=500Ω; $R_{Rfb}$=7500Ω; $V_{VRI}$=1.65, 2.5V |

**Electrical Characteristics - Current sense signal conditioning** (cont'd)

$V_S$ = 5.5 to 20V, $V_{VSOA}$ = 5V, $T_j$ = -40 to +150 °C, $f_{PWM}$ < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.3.20 | Slew rate | $I_{SC}$ | – | 10 | – | V/µs | Gain>= 5; $R_{Load}$=1.0kΩ; $C_{Load}$=500pF |
| 5.3.21 | Large signal open loop voltage gain (DC) | $A_{OL}$ | 80 | 100 | – | dB | – |
| 5.3.22 | Unity gain bandwidth | $GBW$ | 12 | 22 | – | MHz | $R_{Load}$=1kΩ; $C_{Load}$=100pF |
| 5.3.23 | Phase margin[1)] | $\Phi_M$ | – | 50 | – | ° | Gain>= 5; $R_{Load}$=1kΩ; $C_{Load}$=100pF |
| 5.3.24 | Gain margin[1)] | $A_M$ | – | 12 | – | db | $R_{Load}$=1kΩ; $C_{Load}$=100pF |
| 5.3.25 | Bandwidth | $BW_G$ | 1.6 | – | – | MHz | Gain=15; $R_{Load}$=1kΩ; $C_{Load}$=500pF; $R_s$=500Ω |
| 5.3.26 | Output settle time to 98% | $t_{set}$ | – | 1 | 1.8 | µs | Gain=15; $R_{Load}$=1kΩ; $C_{Load}$=500pF; 0.2<$V_{VO}$< 4.0V; $R_{RS}$=500Ω |
| 5.3.27 | Output rise time 10% to 90% | $t_{Irise}$ | – | – | 1 | µs | |
| 5.3.28 | Output fall time 90% to 10% | $t_{Ifall}$ | – | – | 1 | µs | |

1) Not subject to production test; specified by design

2) Without considering any offsets such as input offset voltage, internal miss match and assuming no tolerance error in external resistors.

# 6 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as electro-hydraulic or electric power steering. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

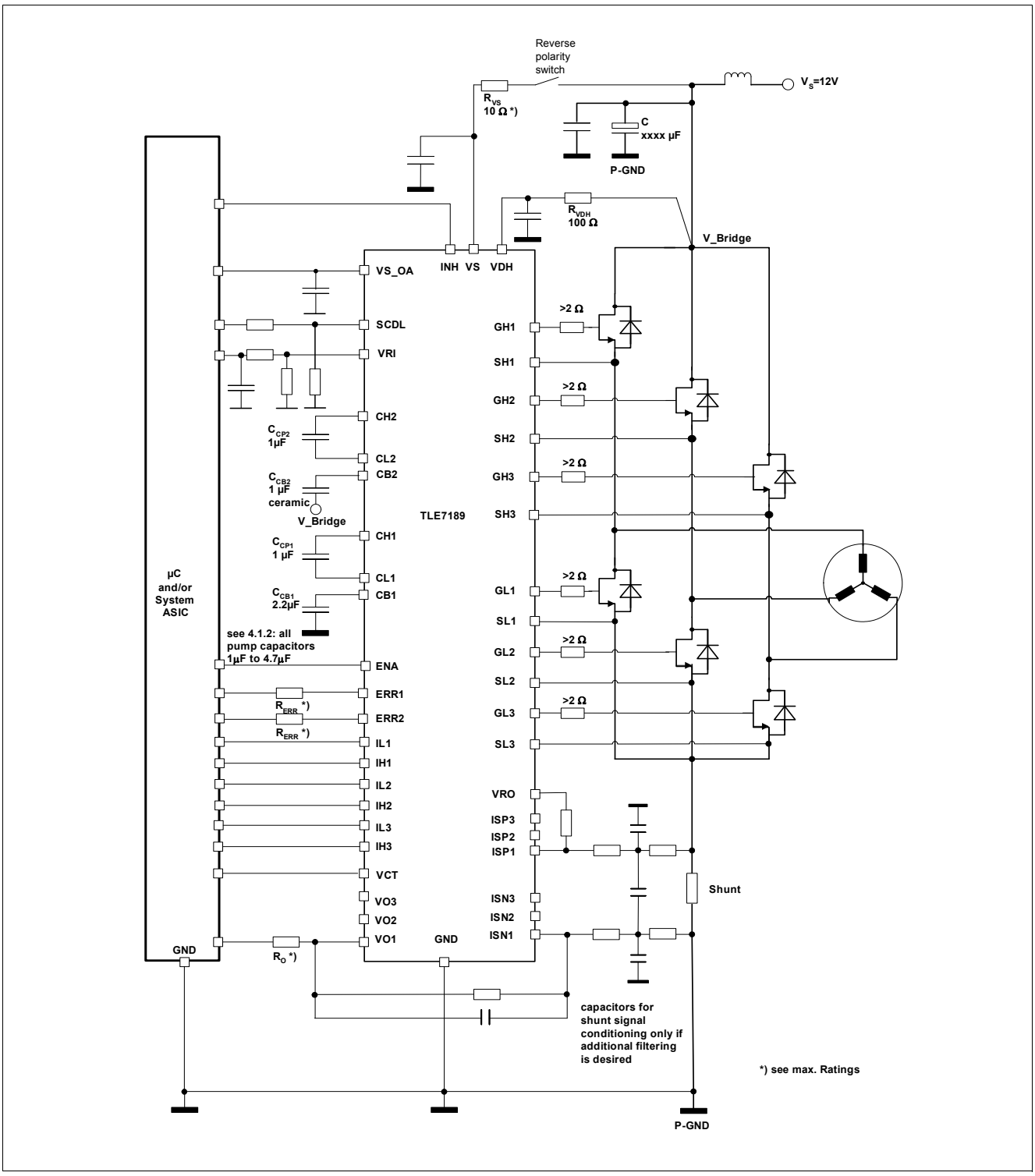



**Figure 5 Application Circuit - TLE7189QK**

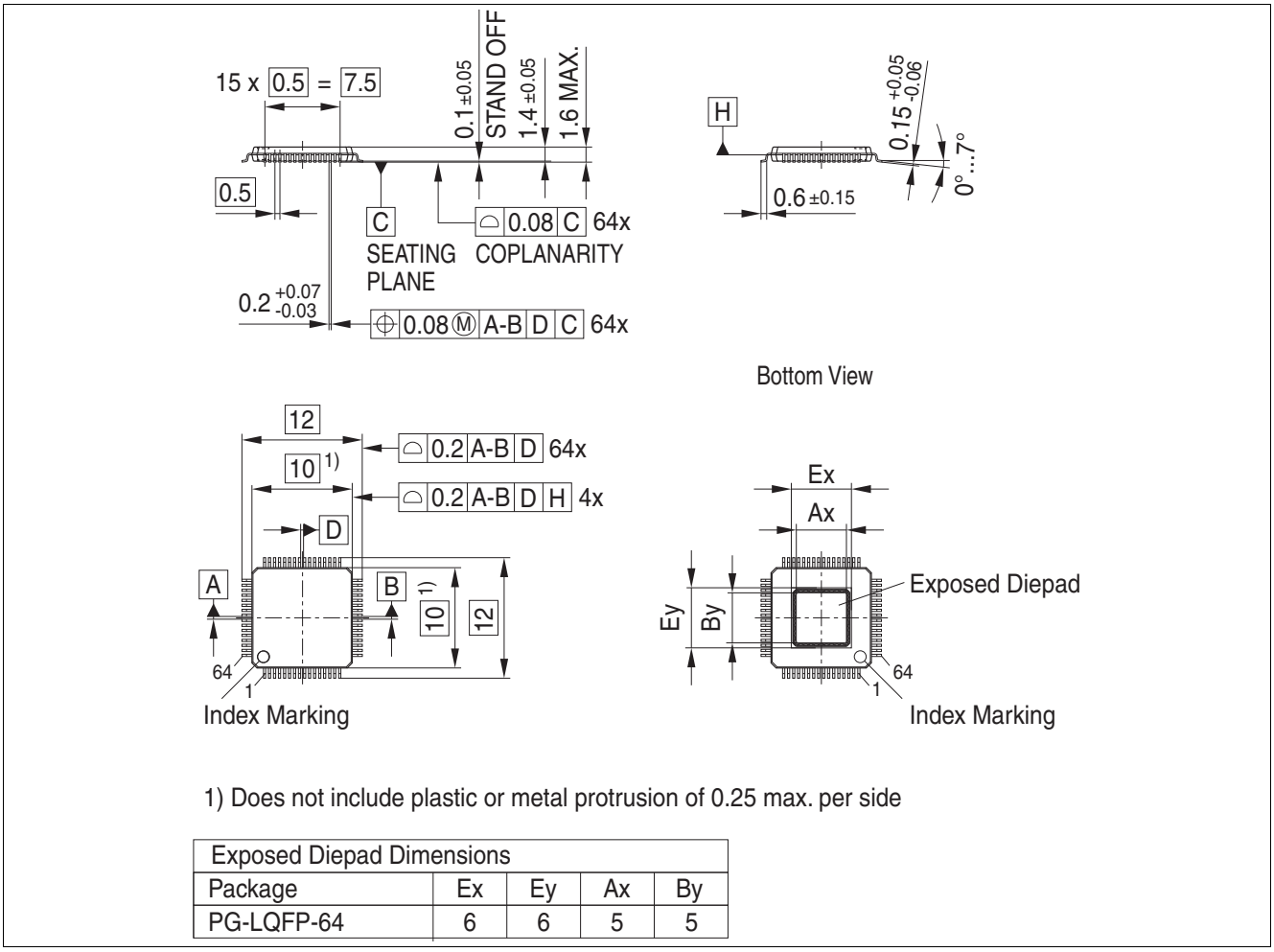
*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

## 6.1 Layout Guide Lines

Please refer also to the simplified application example.

- Three separated bulk capacitors $C_B$ should be used - one per half bridge
- Three separated ceramic capacitors $C_C$ should be used - one per half bridge
- Each of the 3 bulk capacitors $C_B$ and each of the 3 ceramic capacitors $C_C$ should be assigned to one of the half bridges and should be placed very close to it
- The components within one half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor $C_B$ and ceramic capacitor $C_C$ ($C_B$ and $C_C$ are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The three half bridges can be separated; yet, when there is one common GND referenced shunt resistor for the three half bridges the sources of the three low side MOSFETs should be close to each other and close to the common shunt resistor
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high side MOSFETs to sense the voltage present on drain high side
- CB2 is the buffer capacitor of charge pump 2; its negative terminal should be routed to the common point of the drains of the high side MOSFETs as well - this connection should be low inductive / resistive
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- the exposed pad on the backside of the LQFP is recommended to connect to GND

# 7 Package Outlines




| Exposed Diepad Dimensions | | | | |
|---|---|---|---|---|
| Package | Ex | Ey | Ax | By |
| PG-LQFP-64 | 6 | 6 | 5 | 5 |

**Figure 6 PG-LQFP-64**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

# 8 Revision History

| Version | Date | Changes |
|---|---|---|
| V2.2 | 2016-01-28 | package adjustments |
| V2.1 | 2012-11-28 | marking typo fix, cover update |
| V2.0 | 2009-07 | – |

**Edition 2016-01-28**

**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**



### Legal Disclaimer

PRO-SIL™ is a Registered Trademark of Infineon Technologies AG. The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency. SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.

SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.